

Dual N-Channel 30-V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY			
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
Channel-1	30	0.022 at V _{GS} = 10 V	6.3
		0.030 at V _{GS} = 4.5 V	5.4
Channel-2		0.0155 at V _{GS} = 10 V	9.5
		0.0205 at V _{GS} = 4.5 V	8.2

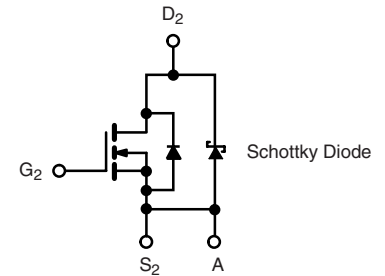
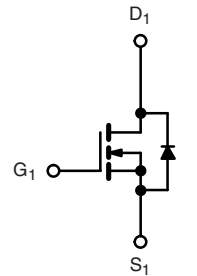
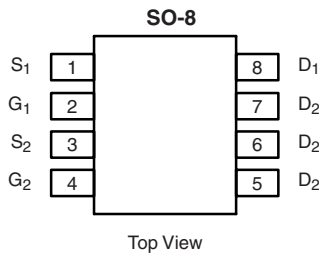
SCHOTTKY PRODUCT SUMMARY		
V _{DS} (V)	V _{SD} (V) Diode Forward Voltage	I _F (A)
30	0.50 V at 1.0 A	2.0

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- LITTLE FOOT® Plus
- Compliant to RoHS directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available



Ordering Information: Si4818DY-T1-E3 (Lead (Pb)-free)
Si4818DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted							
Parameter	Symbol	Channel-1		Channel-2		Unit	
		10 s	Steady State	10 s	Steady State		
Drain-Source Voltage	V _{DS}	30				V	
Gate-Source Voltage	V _{GS}	20					
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	6.3	5.3	9.5	7.0	A
		T _A = 70 °C	5.4	4.2	7.6	5.6	
Pulsed Drain Current	I _{DM}	30		40		W	
Continuous Source Current (Diode Conduction) ^a	I _S	1.3	0.9	2.2	1.15		
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	1.4	1.0	2.4	1.25	W
		T _A = 70 °C	0.9	0.64	1.5	0.80	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150				°C	

THERMAL RESISTANCE RATINGS									
Parameter	Symbol	Channel-1		Channel-2		Schottky		Unit	
		Typ.	Max.	Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 s	72	90	43	53	48	60	°C/W
		Steady State	100	125	82	100	80	100	
Maximum Junction-to-Foot (Drain)	R _{thJC}	Steady State	51	63	25	30	28	35	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

MOSFET SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	Ch-1 Ch-2	0.8 1.0		V	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = 20\text{ V}$	Ch-1 Ch-2		100 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$	Ch-1 Ch-2		1 100	μA	
		$V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 85\text{ }^\circ\text{C}$	Ch-1 Ch-2		15 2000		
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}$, $V_{GS} = 10\text{ V}$	Ch-1 Ch-2	20 30		A	
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 6.3\text{ A}$	Ch-1		0.018	0.022	Ω
		$V_{GS} = 10\text{ V}$, $I_D = 9.5\text{ A}$	Ch-2		0.0125	0.0155	
		$V_{GS} = 4.5\text{ V}$, $I_D = 5.4\text{ A}$	Ch-1		0.024	0.030	
		$V_{GS} = 4.5\text{ V}$, $I_D = 8.2\text{ A}$	Ch-2		0.0165	0.0205	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 6.3\text{ A}$	Ch-1		17	S	
		$V_{DS} = 15\text{ V}$, $I_D = 9.5\text{ A}$	Ch-2		28		
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.3\text{ A}$, $V_{GS} = 0\text{ V}$	Ch-1		0.7	1.1	V
		$I_S = 1\text{ A}$, $V_{GS} = 0\text{ V}$	Ch-2		0.47	0.5	
Dynamic^a							
Total Gate Charge	Q_g	Channel-1 $V_{DS} = 15\text{ V}$, $V_{GS} = 5\text{ V}$, $I_D = 6.3\text{ A}$	Ch-1 Ch-2		8.0 15	12 23	nC
Gate-Source Charge	Q_{gs}		Ch-1 Ch-2		1.75 5.3		
Gate-Drain Charge	Q_{gd}	Channel-2 $V_{DS} = 15\text{ V}$, $V_{GS} = 5\text{ V}$, $I_D = -9.5\text{ A}$	Ch-1 Ch-2		3.2 4.6		
Gate Resistance	R_g		Ch-1 Ch-2	1.5 0.5		6.1 2.6	Ω
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}$, $R_L = 15\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 6\text{ }\Omega$	Ch-1 Ch-2		10 15	20 30	ns
Rise Time	t_r		Ch-1 Ch-2		5 5	10 10	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}$, $R_L = 15\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 6\text{ }\Omega$	Ch-1 Ch-2		26 44	50 80	
Fall Time	t_f		Ch-1 Ch-2		8 12	16 24	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	Ch-1		30	60	
		$I_F = 2.2\text{ A}$, $di/dt = 100\text{ }\mu\text{A}/\mu\text{s}$	Ch-2		32	70	

Notes:

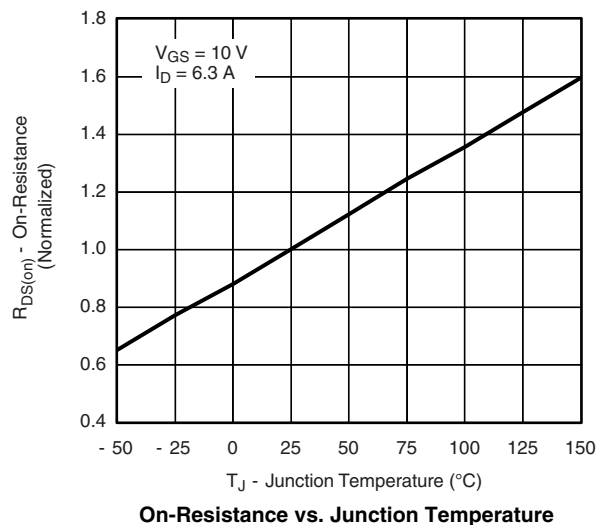
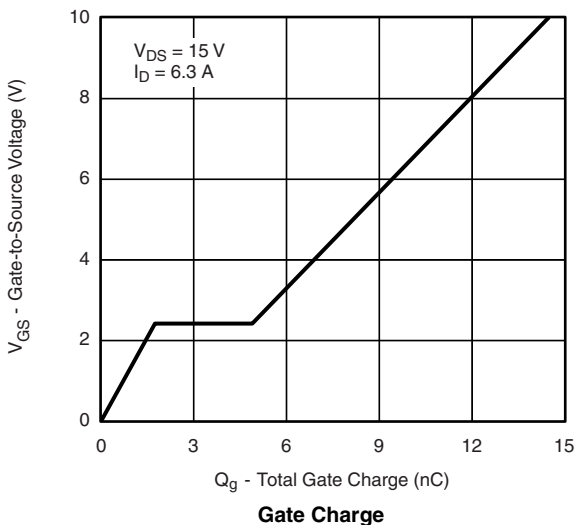
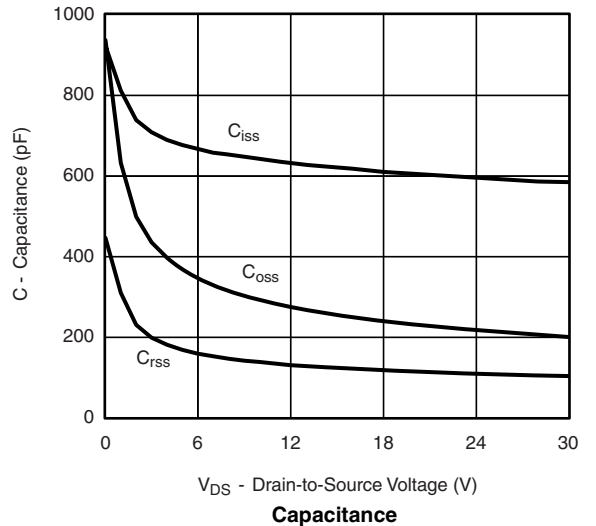
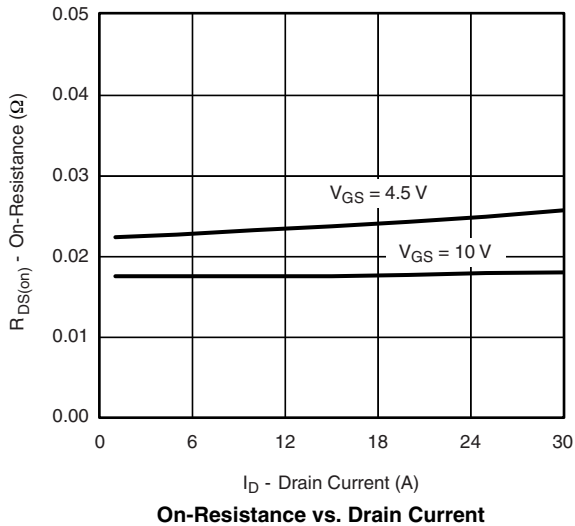
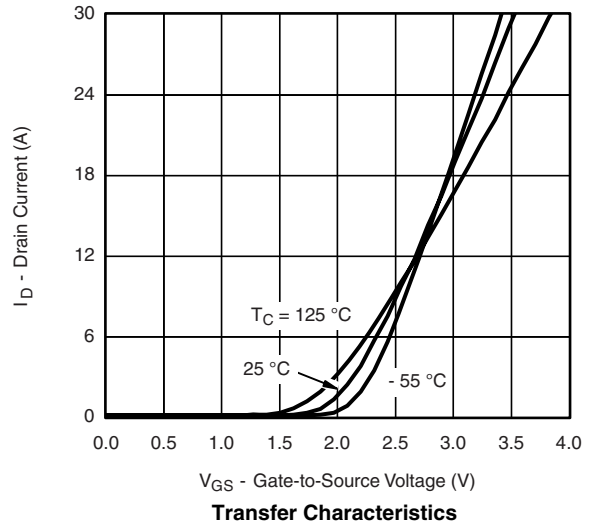
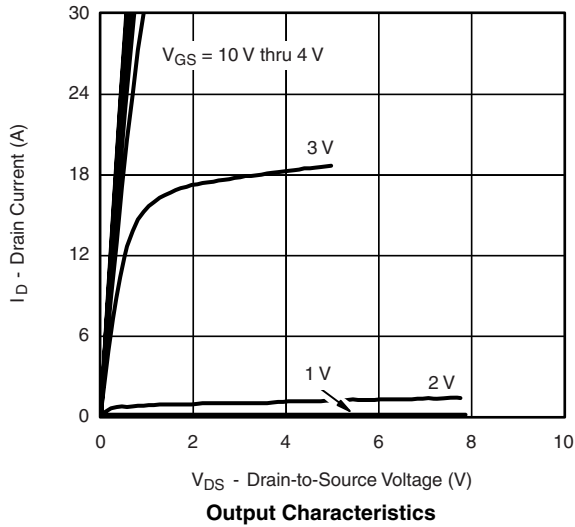
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

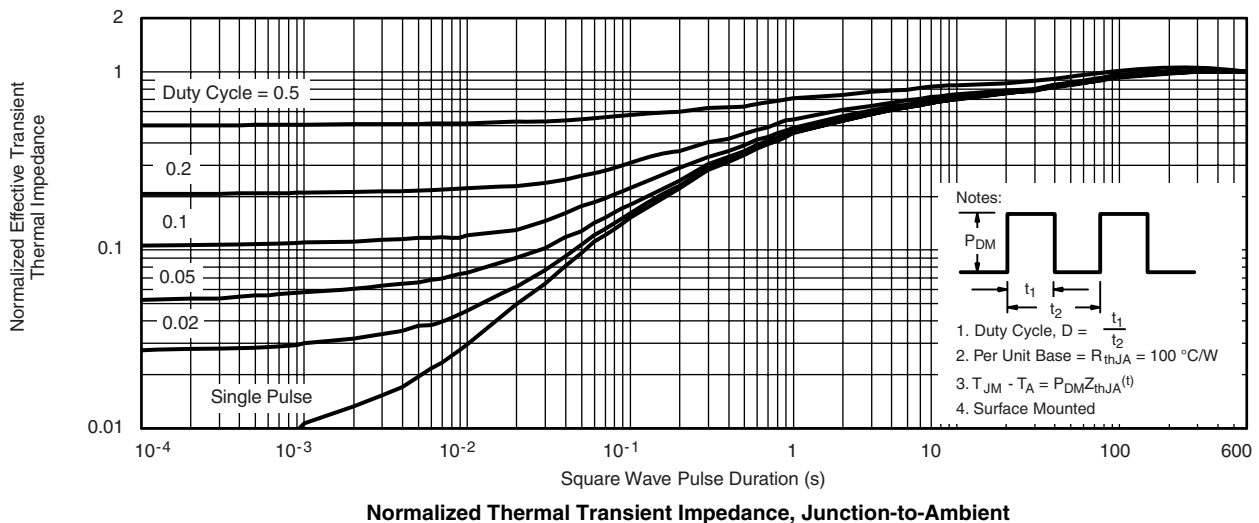
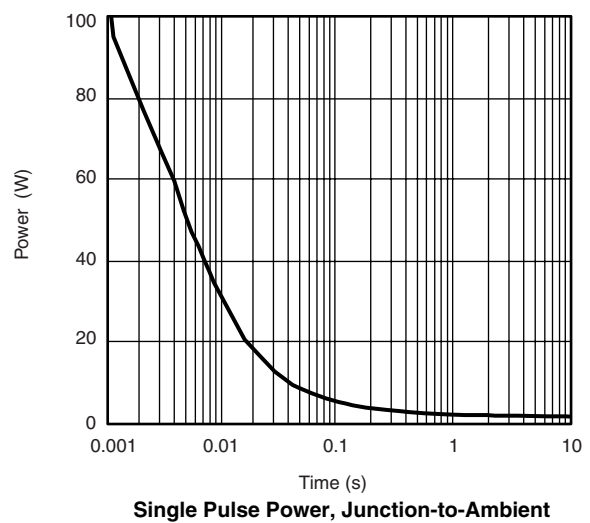
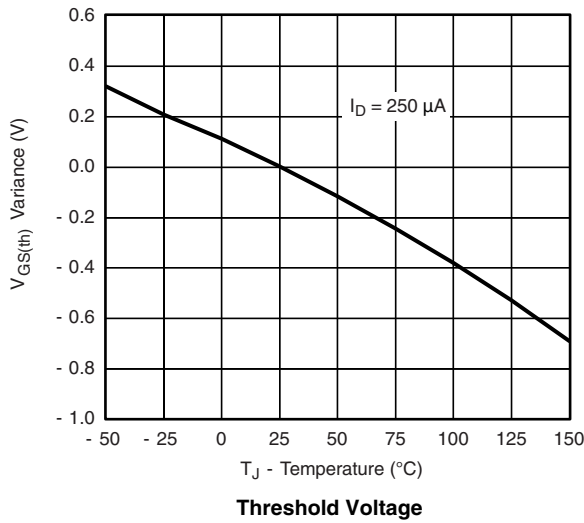
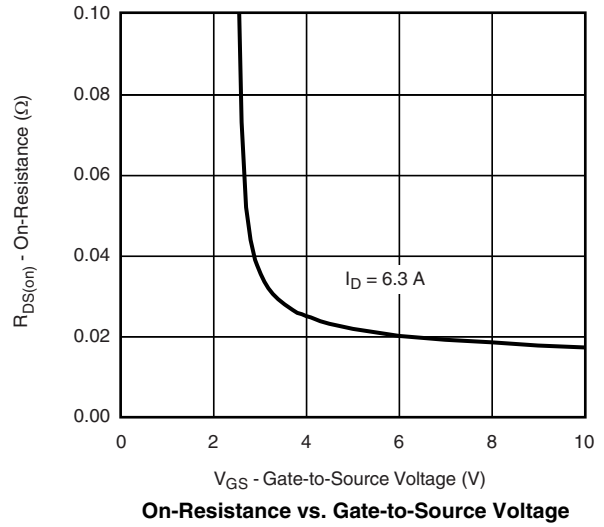
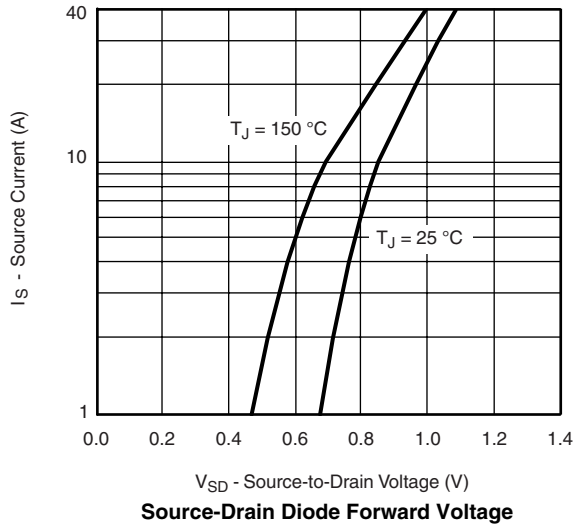
SCHOTTKY SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Forward Voltage Drop	V_F	$I_F = 1.0\text{ A}$		0.47	0.50	V
		$I_F = 1.0\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		0.36	0.42	
Maximum Reverse Leakage Current	I_{rm}	$V_R = 30\text{ V}$		0.004	0.100	mA
		$V_R = 30\text{ V}$, $T_J = 100\text{ }^\circ\text{C}$		0.7	10	
		$V_R = -30\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$		3.0	20	
Junction Capacitance	C_T	$V_R = 10\text{ V}$		50		pF

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

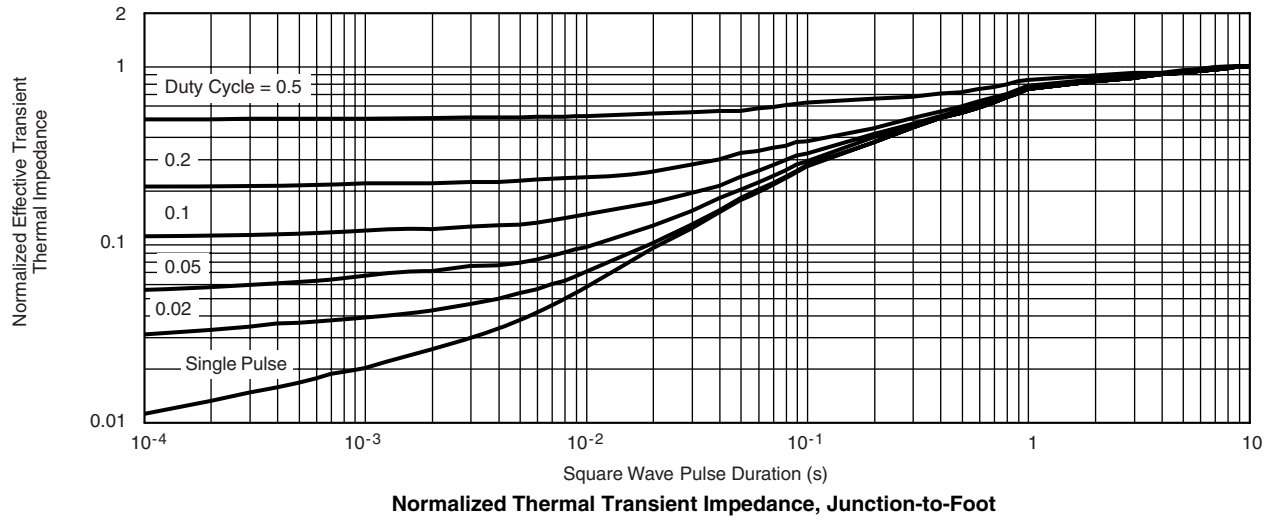
CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



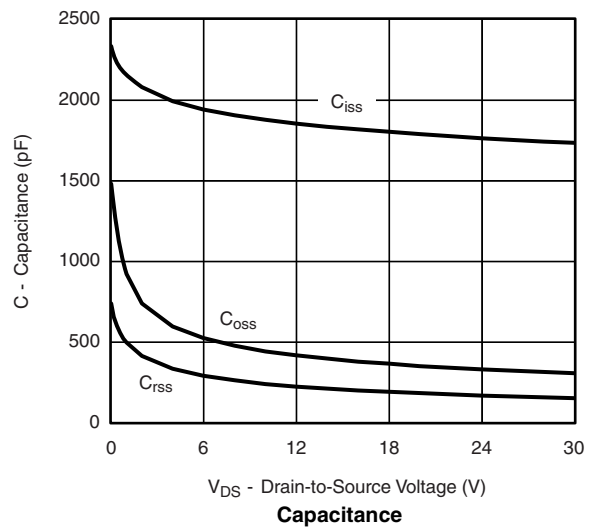
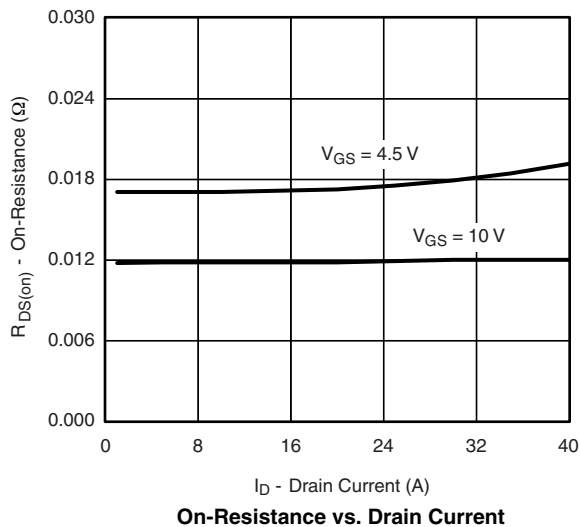
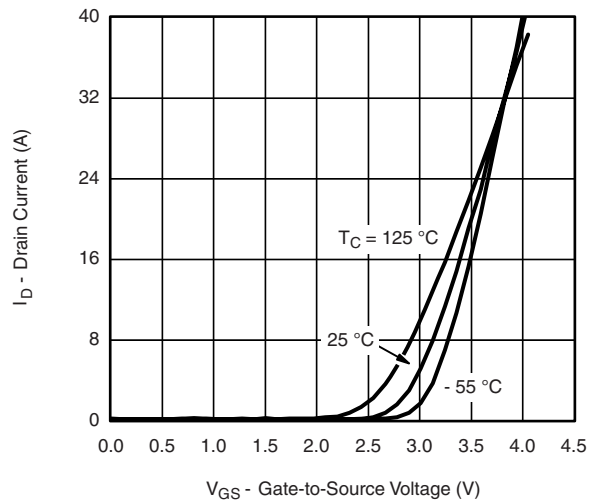
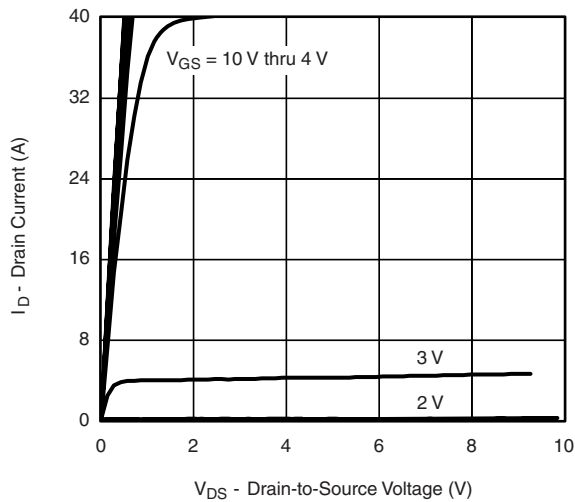
CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



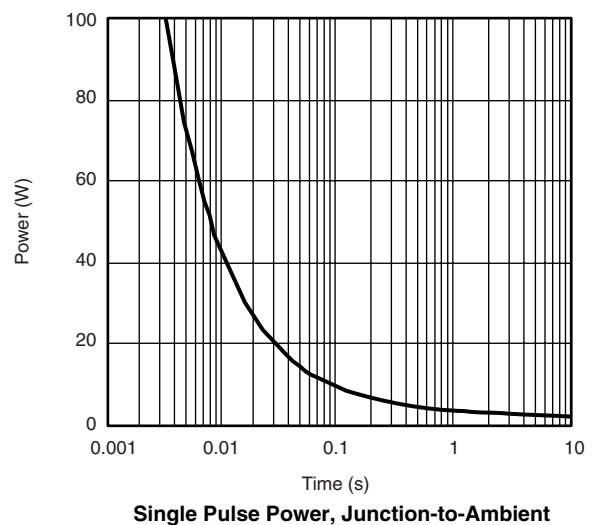
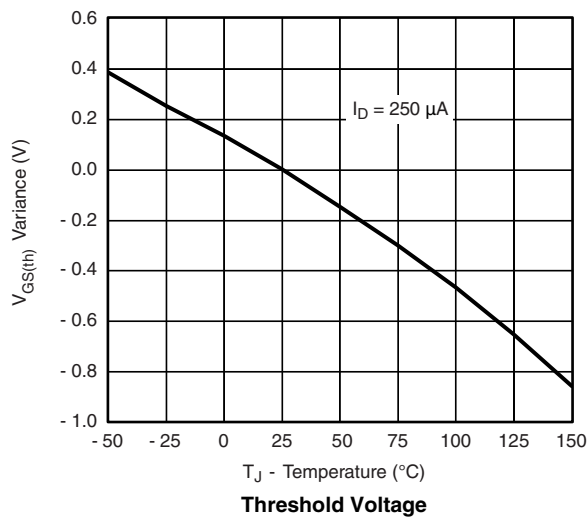
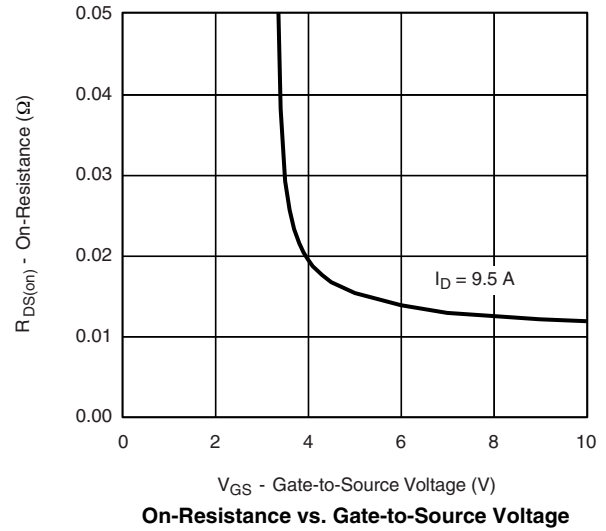
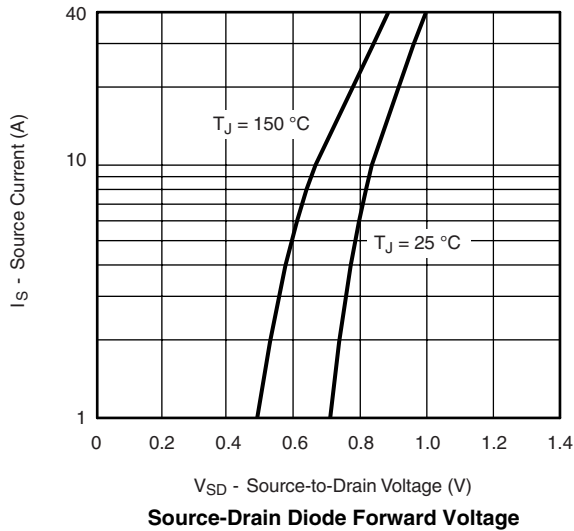
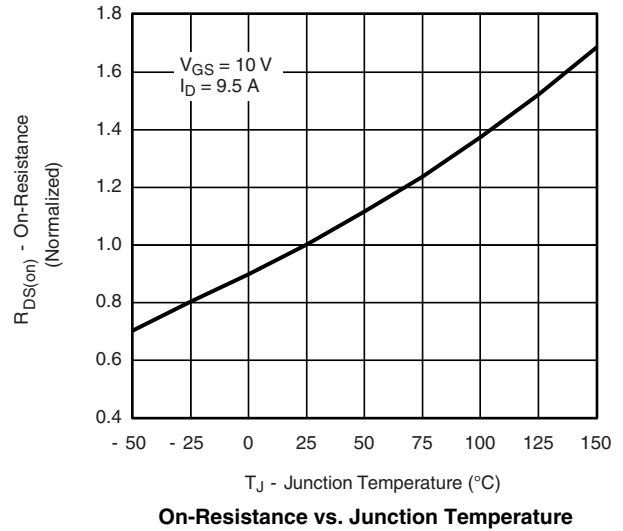
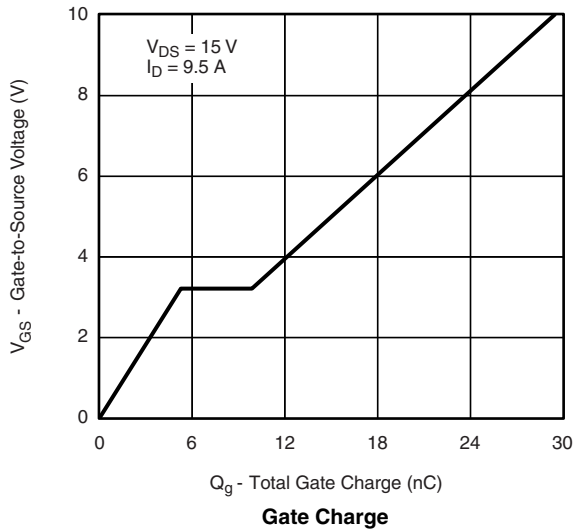
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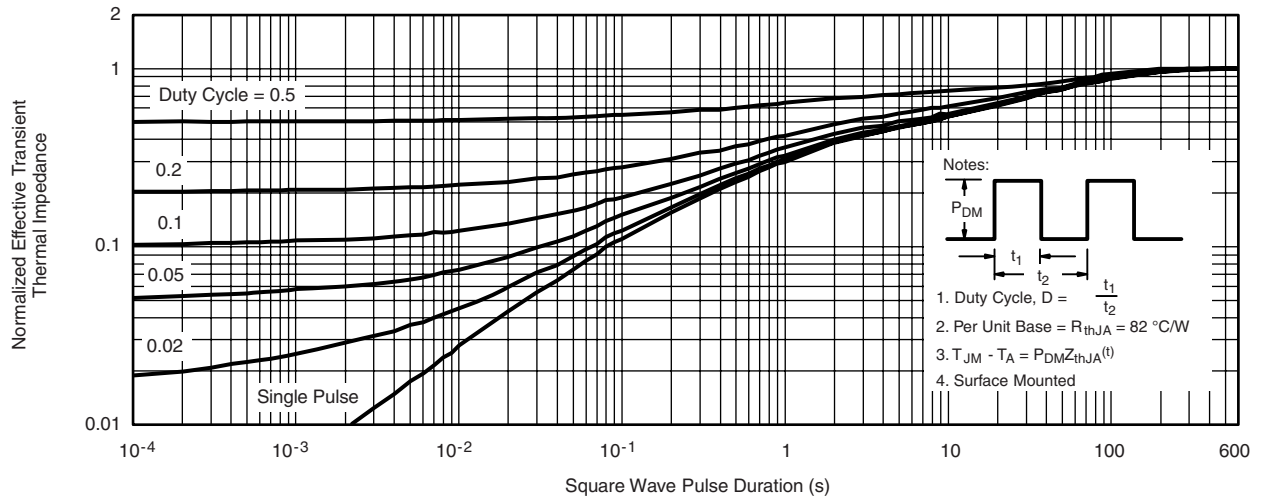
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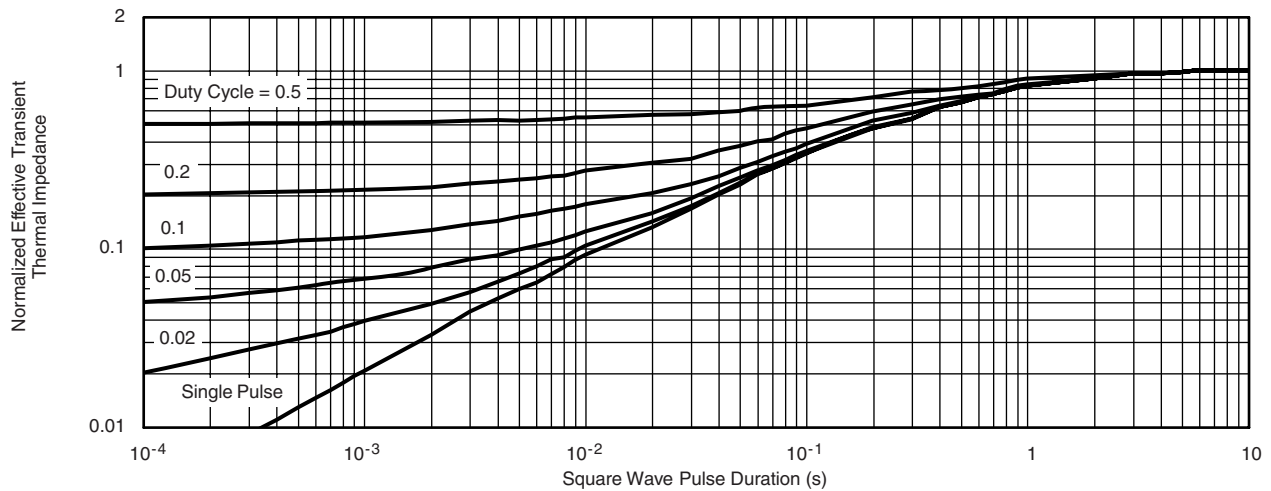
CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

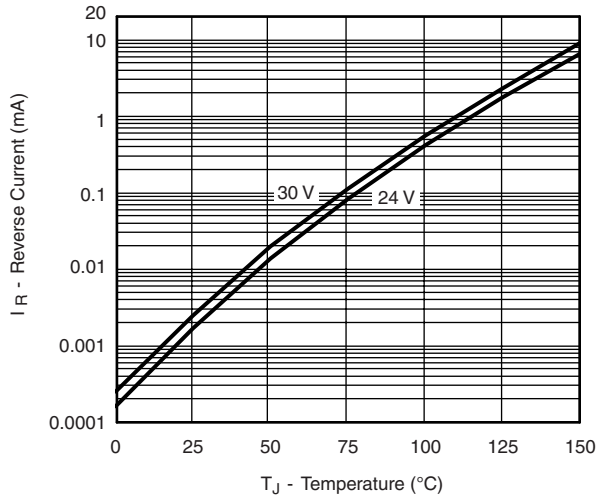


Normalized Thermal Transient Impedance, Junction-to-Ambient

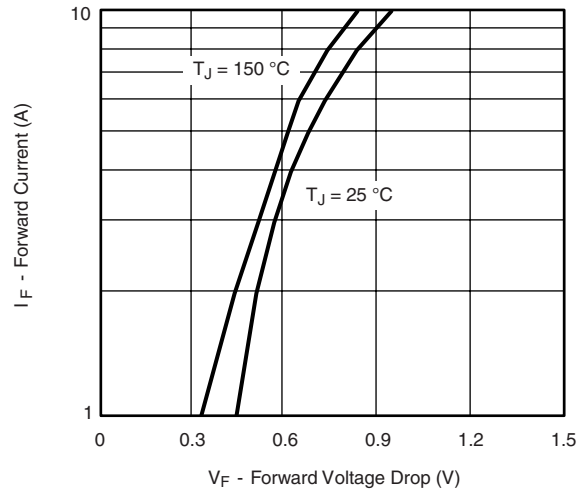


Normalized Thermal Transient Impedance, Junction-to-Foot

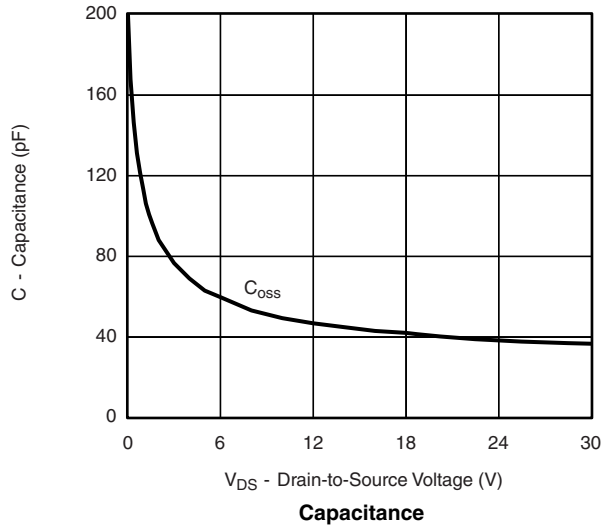
SCHOTTKY TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Reverse Current vs. Junction Temperature



Forward Voltage Drop



Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71122.



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