

## Dual N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY				
	V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
Channel 1	30	0.0145 at V <sub>GS</sub> = 10 V	10.8	8.3
		0.0195 at V <sub>GS</sub> = 4.5 V	9.3	
Channel 2	30	0.0265 at V <sub>GS</sub> = 10 V	7.2	4
		0.036 at V <sub>GS</sub> = 4.5 V	6.2	

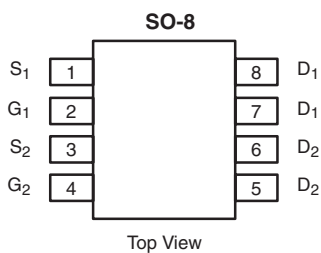
### FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested

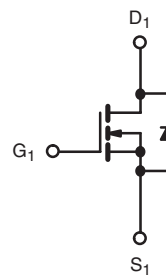


### APPLICATIONS

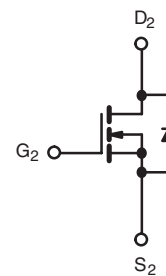
- Logic DC/DC for Notebook PC



Ordering Information: Si4972DY-T1-E3 (Lead (Pb)-free)  
Si4972DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted				
Parameter	Symbol	Channel 1	Channel 2	Unit
Drain-Source Voltage	V <sub>DS</sub>	30		V
Gate-Source Voltage	V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C	10.8	7.2	A
	T <sub>C</sub> = 70 °C	8.7	5.7	
	T <sub>A</sub> = 25 °C	8.7 <sup>b,c</sup>	6.4 <sup>b,c</sup>	
	T <sub>A</sub> = 70 °C	6.9 <sup>b,c</sup>	5.1 <sup>b,c</sup>	
Pulsed Drain Current (10 μs Pulse Width)	I <sub>DM</sub>	20	20	A
Source-Drain Current Diode Current	T <sub>C</sub> = 25 °C	2.5	2.1	
	T <sub>A</sub> = 25 °C	1.6 <sup>b,c</sup>	1.6 <sup>b,c</sup>	
Pulsed Source-Drain Current	I <sub>SM</sub>	20	20	mJ
Single Pulse Avalanche Current	L = 0.1 mH I <sub>AS</sub>	15	6	
Avalanche Energy	E <sub>AS</sub>	11	1.8	W
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	3.1	2.5	
	T <sub>C</sub> = 70 °C	2.1	1.6	
	T <sub>A</sub> = 25 °C	2.0 <sup>b,c</sup>	2.0 <sup>b,c</sup>	
	T <sub>A</sub> = 70 °C	1.25 <sup>b,c</sup>	1.25 <sup>b,c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Channel 1		Channel 2		Unit
		Typical	Maximum	Typical	Maximum	
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 10 s R <sub>thJA</sub>	52	62.5	55	62.5	°C/W
Maximum Junction-to-Foot (Drain)	Steady R <sub>thJF</sub>	32	40	40	50	

Notes:

- Based on T<sub>C</sub> = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 110 °C/W (Ch 1) and 120 °C/W (Ch 2).

<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted								
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit		
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch 1	30		V		
		$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch 2	30				
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch 1		35	mV/ $^\circ\text{C}$		
		$I_D = 250\text{ }\mu\text{A}$	Ch 2		35			
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch 1		- 6.5			
		$I_D = 250\text{ }\mu\text{A}$	Ch 2		- 6.5			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch 1	1.5	3.0	V		
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch 2	1.5	3.0			
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Ch 1		100	nA		
			Ch 2		100			
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch 1		1	$\mu\text{A}$		
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch 2		1			
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch 1		10			
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch 2		10			
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	Ch 1	10		A		
		$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	Ch 2	10				
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$	Ch 1		0.012	$\Omega$		
		$V_{GS} = 10\text{ V}, I_D = 4.5\text{ A}$	Ch 2		0.022			
		$V_{GS} = 4.5\text{ V}, I_D = 5.6\text{ A}$	Ch 1		0.016		0.0195	
		$V_{GS} = 4.5\text{ V}, I_D = 4\text{ A}$	Ch 2		0.030		0.036	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 6\text{ A}$	Ch 1		27	S		
		$V_{DS} = 15\text{ V}, I_D = 4.5\text{ A}$	Ch 2		20			
<b>Dynamic<sup>a</sup></b>								
Input Capacitance	$C_{iss}$	Channel 1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch 1		1080	pF		
			Ch 2		515			
Output Capacitance	$C_{oss}$		Ch 1		170			
			Ch 2		91			
Reverse Transfer Capacitance	$C_{rss}$		Channel 2 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch 1			72	
				Ch 2			38	
Total Gate Charge	$Q_g$	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 5\text{ A}$		Ch 1		18.5	nC	
		$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 5\text{ A}$		Ch 2		9.6		15
		Channel 1 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$		Ch 1		8.3		13
				Ch 2		4		6
Gate-Source Charge	$Q_{gs}$	Channel 2 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	Ch 1		3.9			
			Ch 2		1.9			
Gate-Drain Charge	$Q_{gd}$		Ch 1		2.7			
			Ch 2		1.3			
Gate Resistance	$R_g$		$f = 1\text{ MHz}$	Ch 1		2.5	$\Omega$	
				Ch 2		2.9		4.4



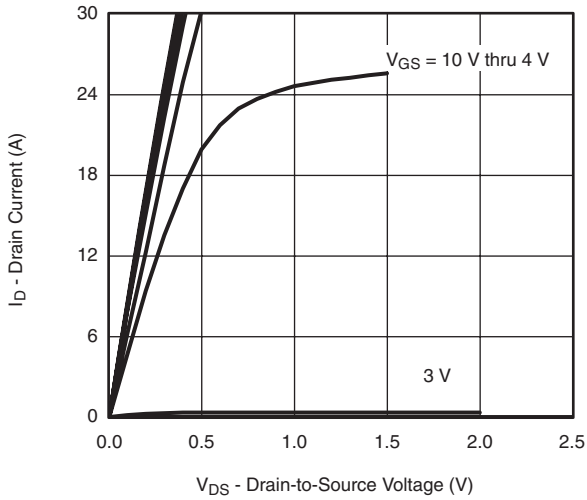
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
<b>Dynamic<sup>a</sup></b>							
Turn-On Delay Time	$t_{d(on)}$	Channel 1 $V_{DD} = 15\text{ V}, R_L = 3\ \Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	Ch 1		12	18	ns
			Ch 2		10	15	
Rise Time	$t_r$		Ch 1		55	83	
			Ch 2		60	90	
Turn-Off Delay Time	$t_{d(off)}$	Channel 2 $V_{DD} = 15\text{ V}, R_L = 3\ \Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	Ch 1		30	45	
			Ch 2		22	33	
Fall Time	$t_f$		Ch 1		7	11	
			Ch 2		6	9	
Turn-On Delay Time	$t_{d(on)}$	Channel 1 $V_{DD} = 15\text{ V}, R_L = 3\ \Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\ \Omega$	Ch 1		120	180	
			Ch 2		108	162	
Rise Time	$t_r$		Ch 1		150	225	
			Ch 2		130	195	
Turn-Off Delay Time	$t_{d(off)}$	Channel 2 $V_{DD} = 15\text{ V}, R_L = 3\ \Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 16\ \Omega$	Ch 1		29	44	
			Ch 2		19	29	
Fall Time	$t_f$		Ch 1		13	20	
			Ch 2		26	39	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	Ch 1		2.5	A	
			Ch 2		2.1		
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$		Ch 1		20		
			Ch 2		20		
Body Diode Voltage	$V_{SD}$	$I_S = 1.6\text{ A}$	Ch 1	0.77	1.2	V	
			Ch 2	0.79	1.2		
Body Diode Reverse Recovery Time	$t_{rr}$	Channel 1 $I_F = 2\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	Ch 1	21	42	ns	
			Ch 2	18	36		
Body Diode Reverse Recovery Charge	$Q_{rr}$		Ch 1	15	30	nC	
			Ch 2	11	22		
Reverse Recovery Fall Time	$t_a$	Channel 2 $I_F = 2\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	Ch 1	13		ns	
			Ch 2	11			
Reverse Recovery Rise Time	$t_b$		Ch 1	8			
			Ch 2	7			

Notes:

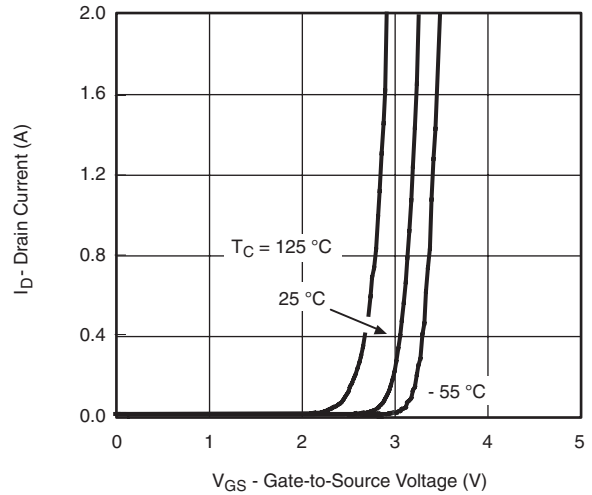
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

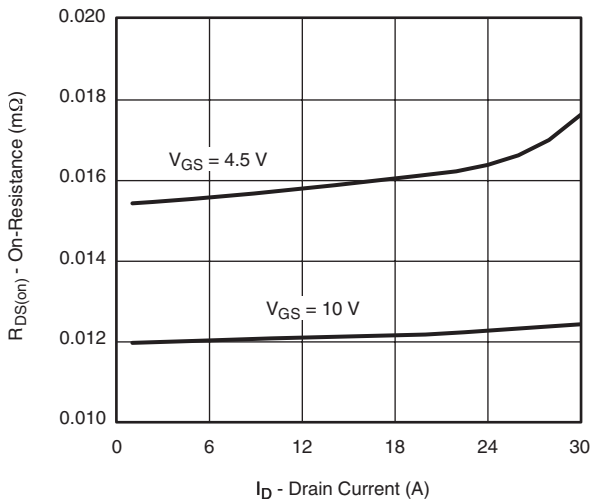
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



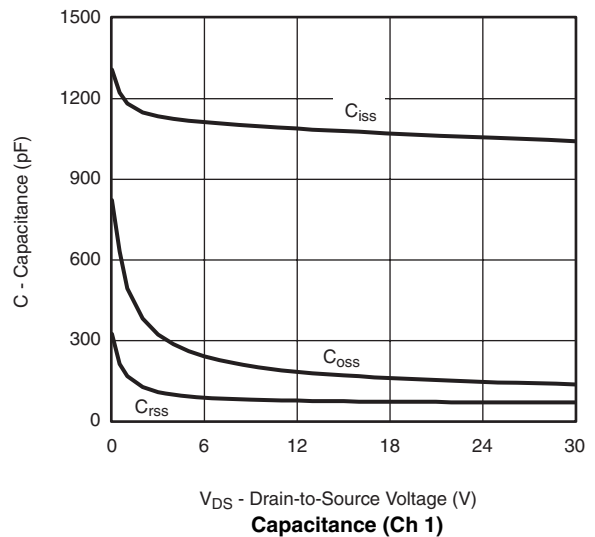
**Output Characteristics (Ch 1)**



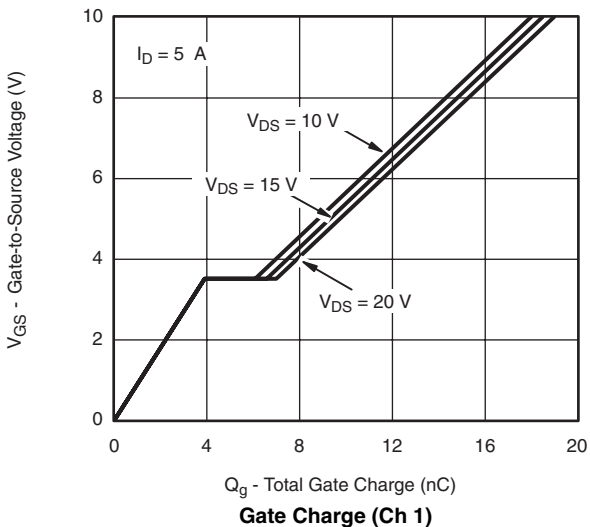
**Transfer Characteristics (Ch 1)**



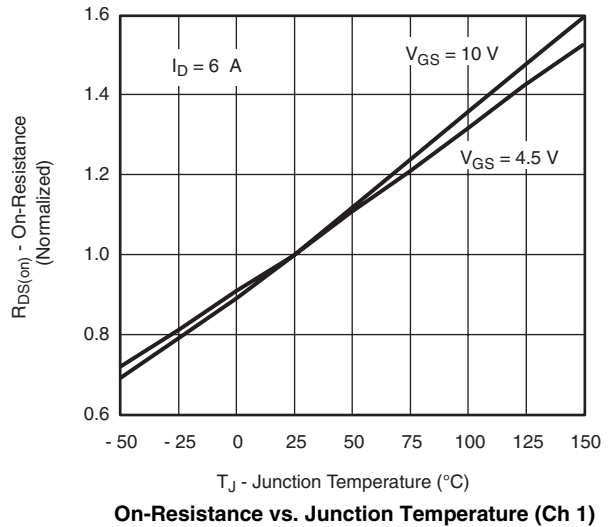
**On-Resistance vs. Drain Current and Gate Voltage (Ch 1)**



**Capacitance (Ch 1)**

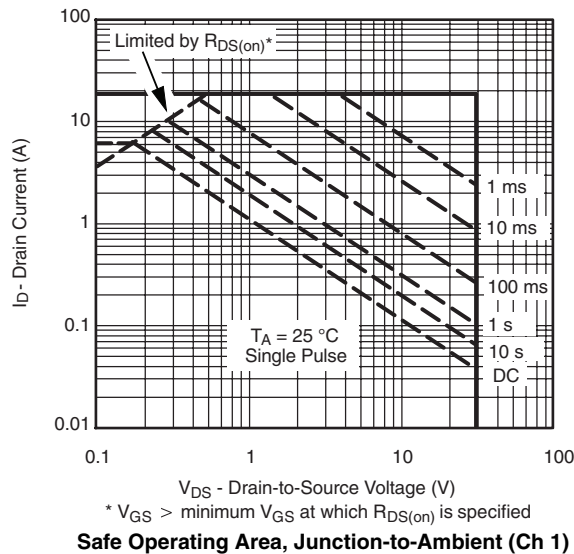
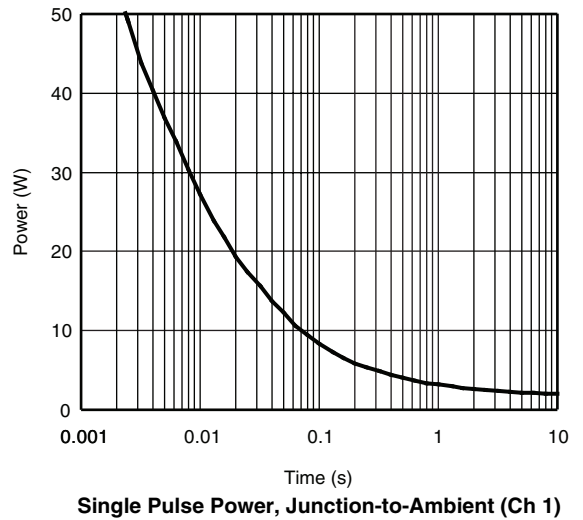
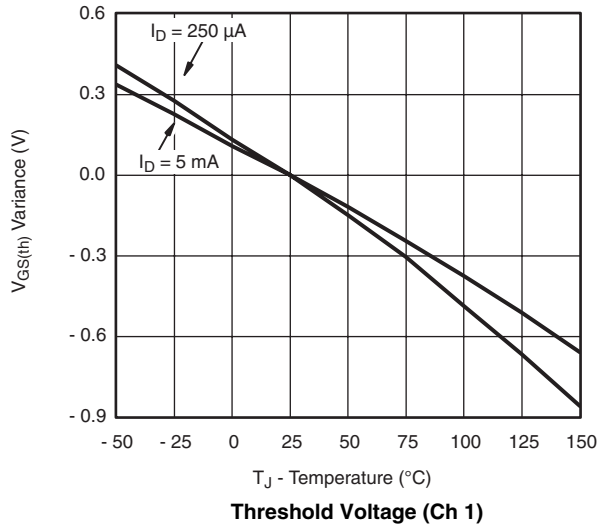
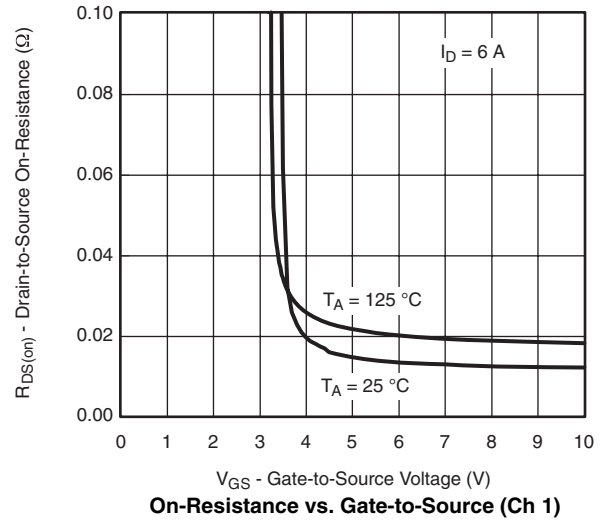
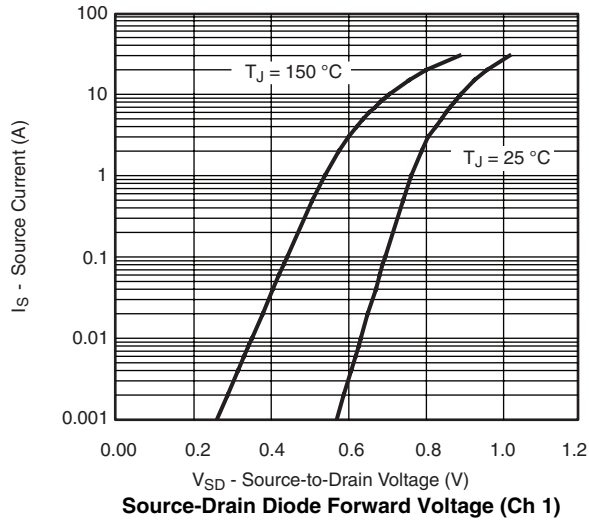


**Gate Charge (Ch 1)**

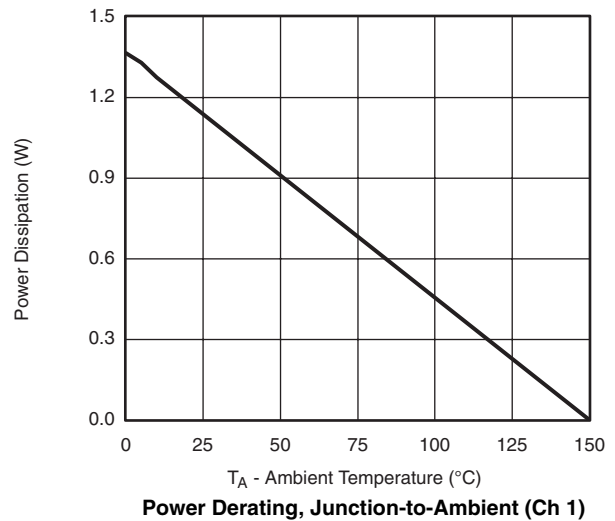
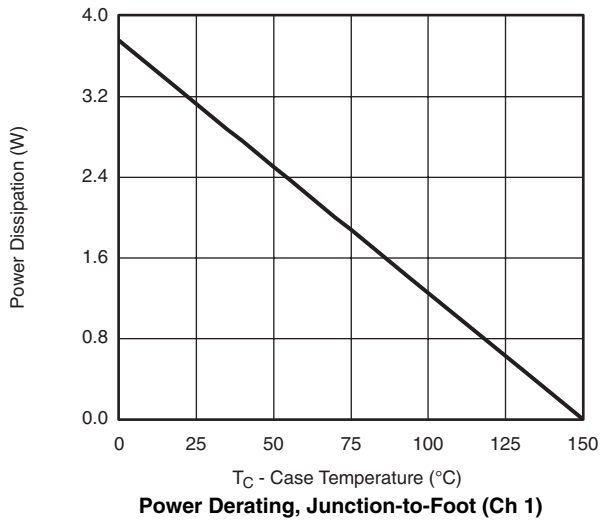
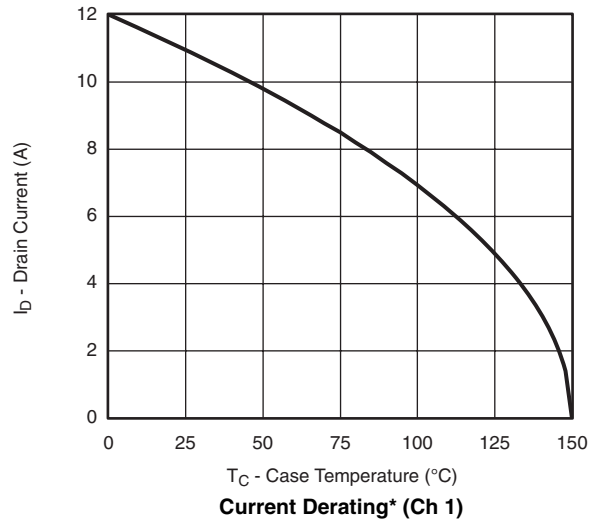


**On-Resistance vs. Junction Temperature (Ch 1)**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

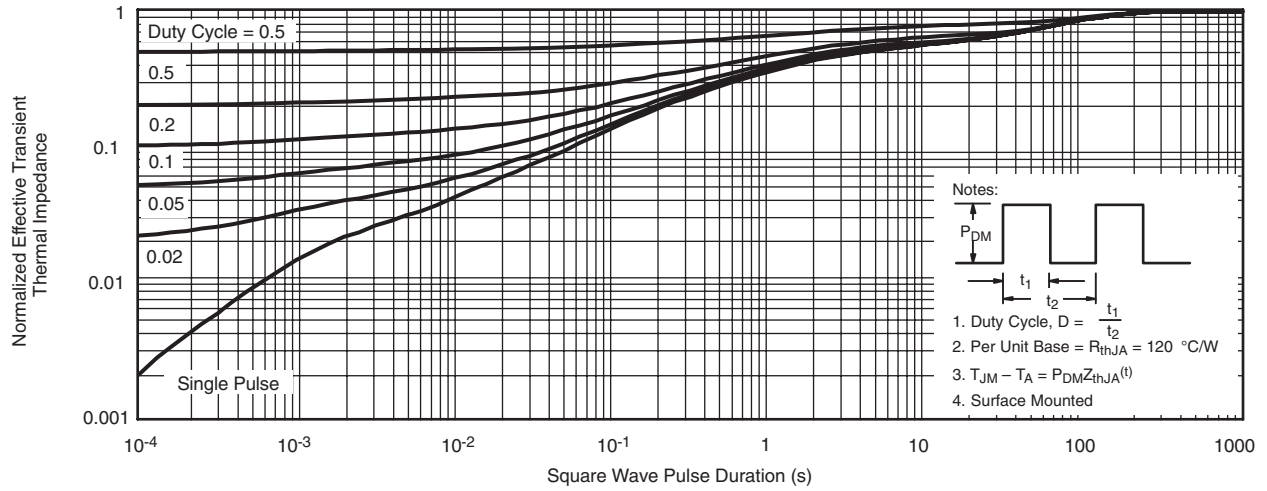


**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

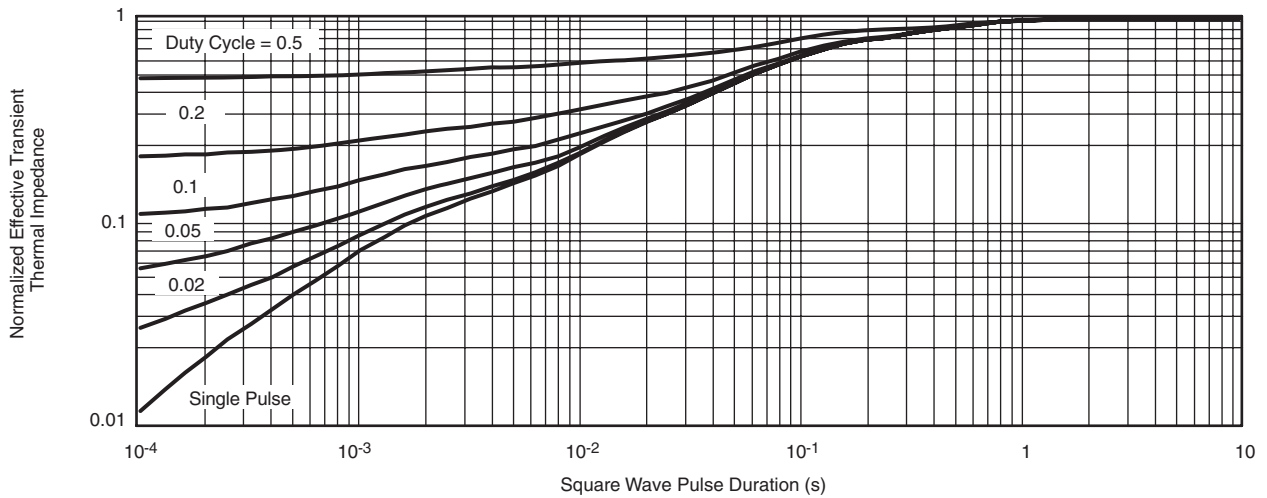


\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

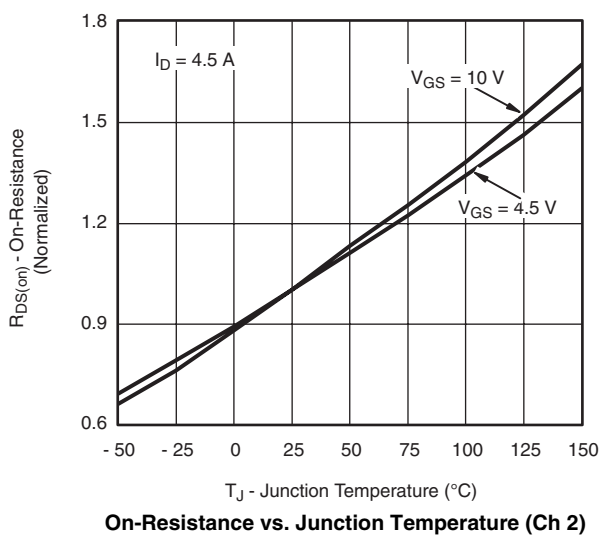
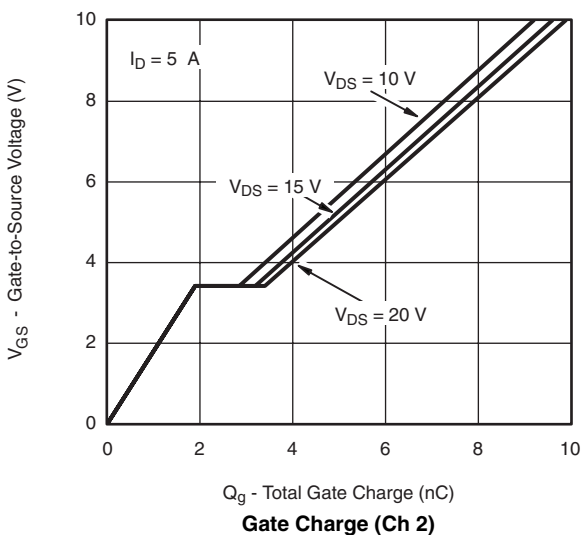
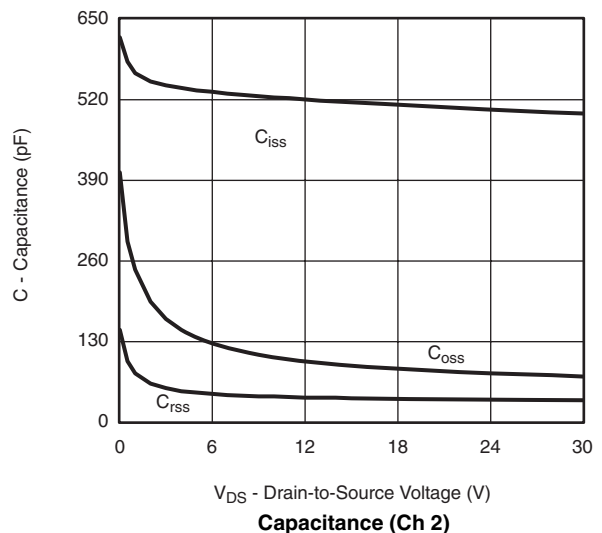
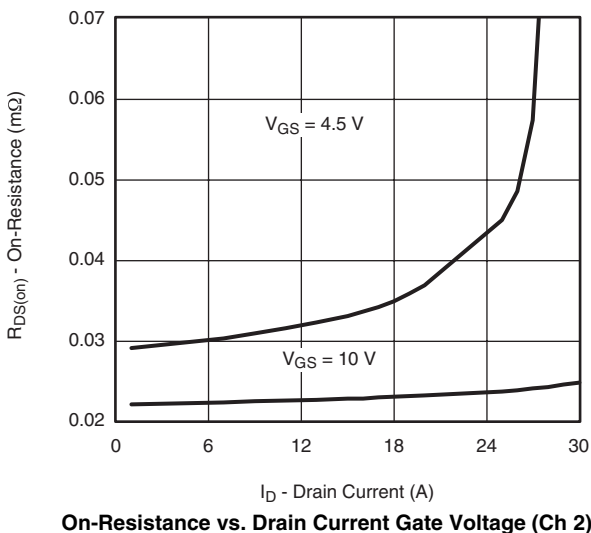
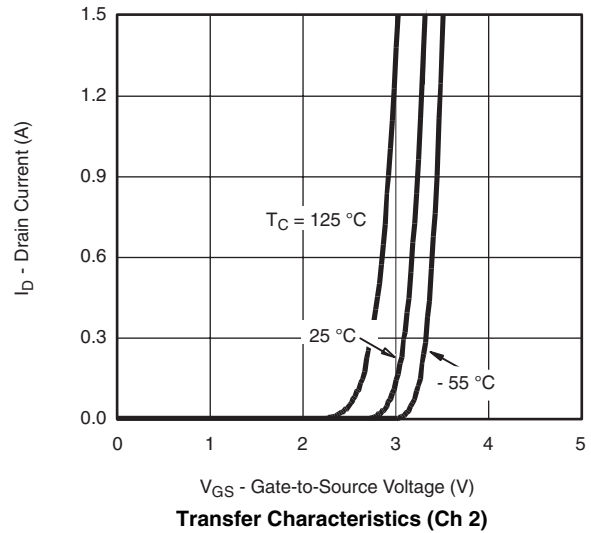
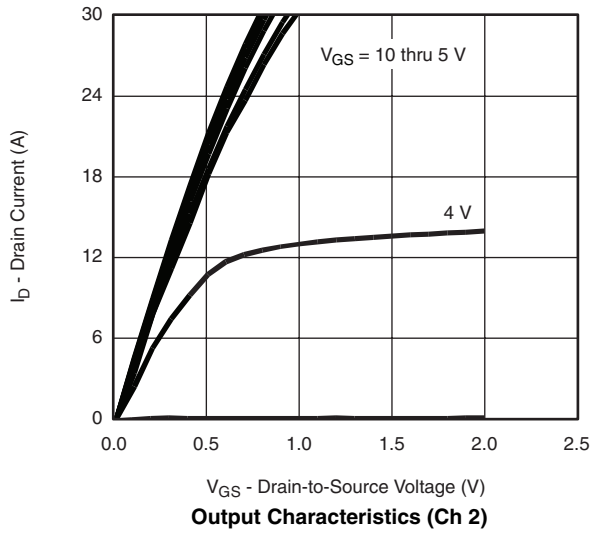


**Normalized Thermal Transient Impedance, Junction-to-Ambient (Ch 1)**



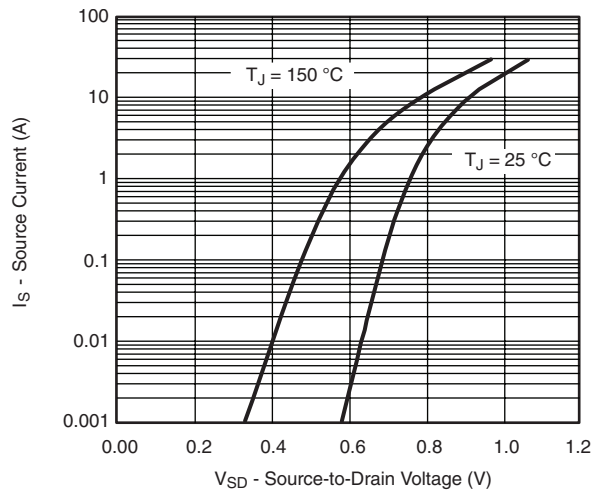
**Normalized Thermal Transient Impedance, Junction-to-Case (Ch 1)**

### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

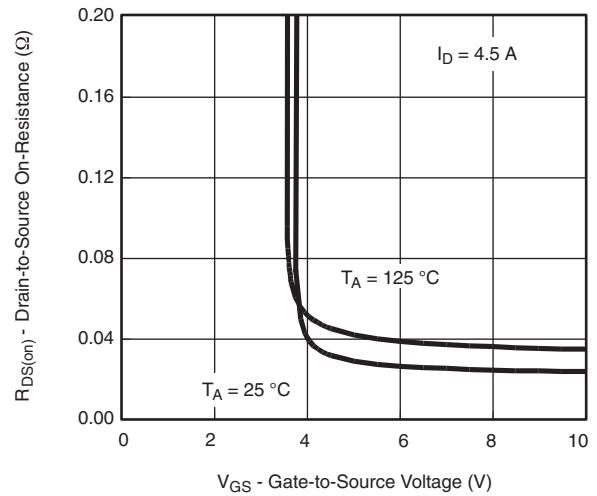




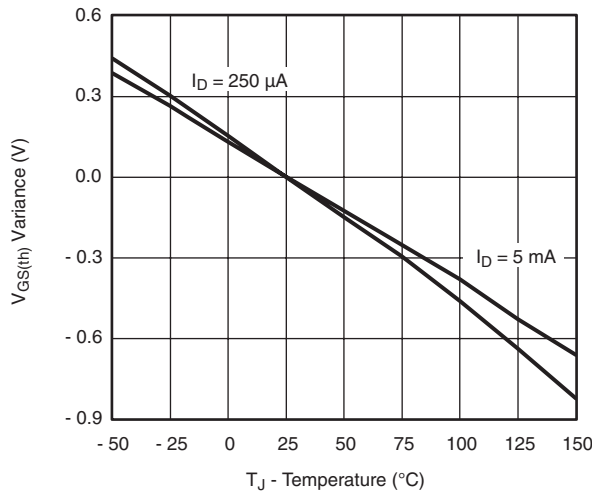
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



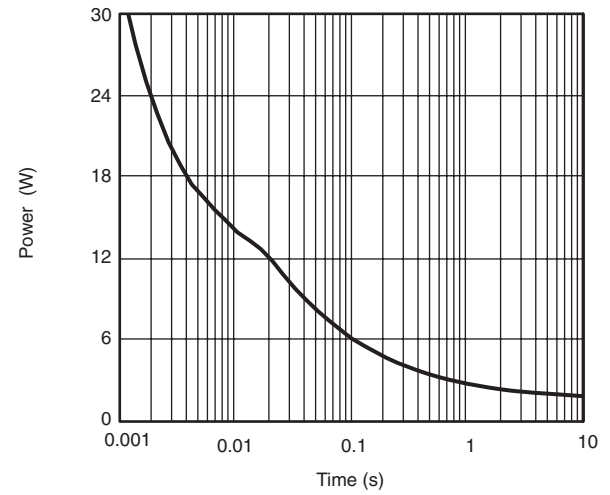
**Source-Drain Diode Forward Voltage (Ch 2)**



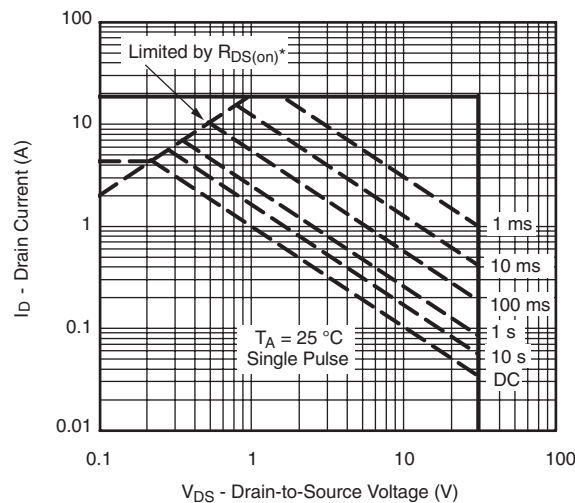
**On-Resistance vs. Gate-to-Source Temperature (Ch 2)**



**Threshold Voltage (Ch 2)**



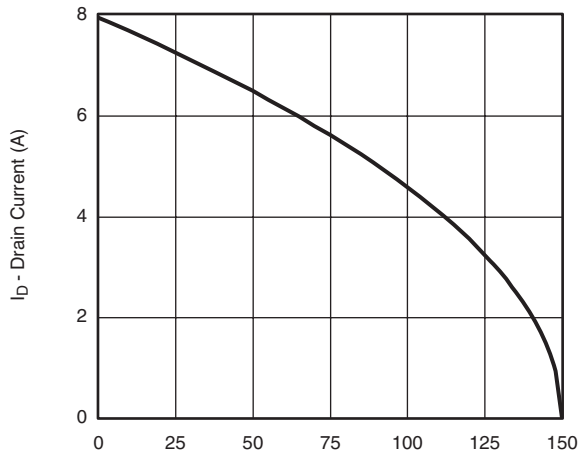
**Single Pulse Power, Junction-to-Ambient (Ch 2)**



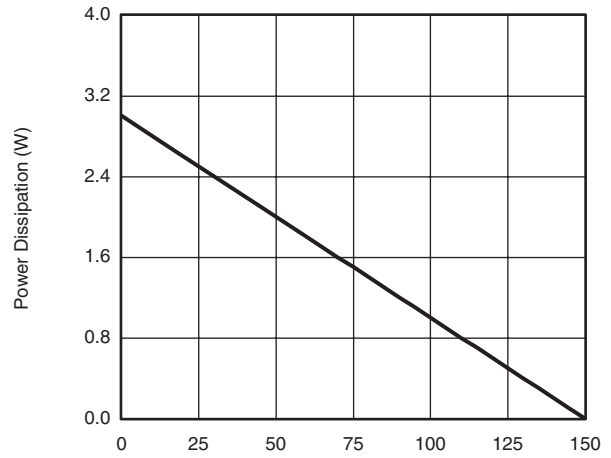
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Ambient (Ch 2)**

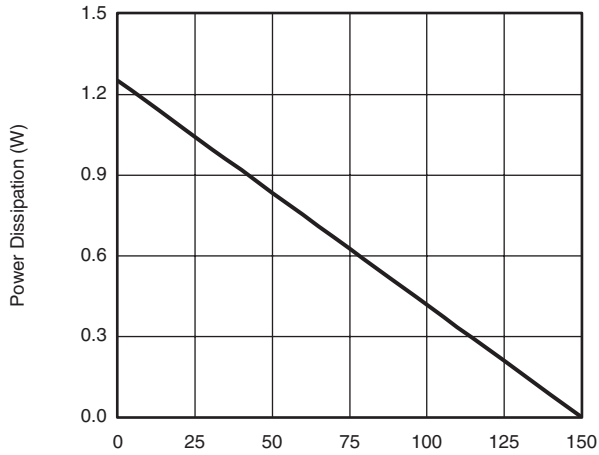
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



$T_C$  - Case Temperature (°C)  
**Current Derating\* (Ch 2)**



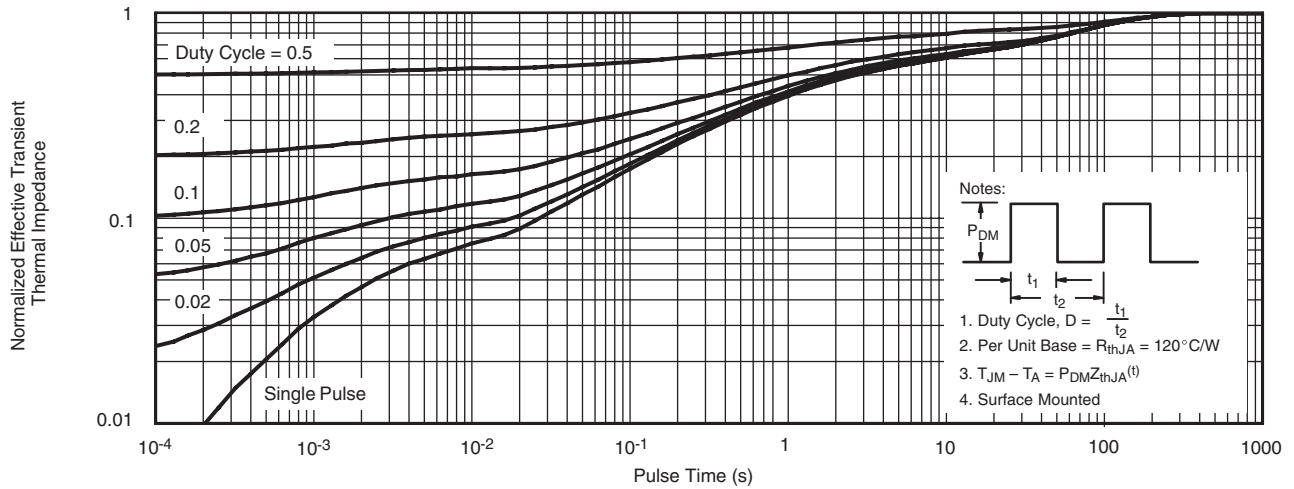
$T_C$  - Case Temperature (°C)  
**Power Derating, Junction-to-Foot (Ch 2)**



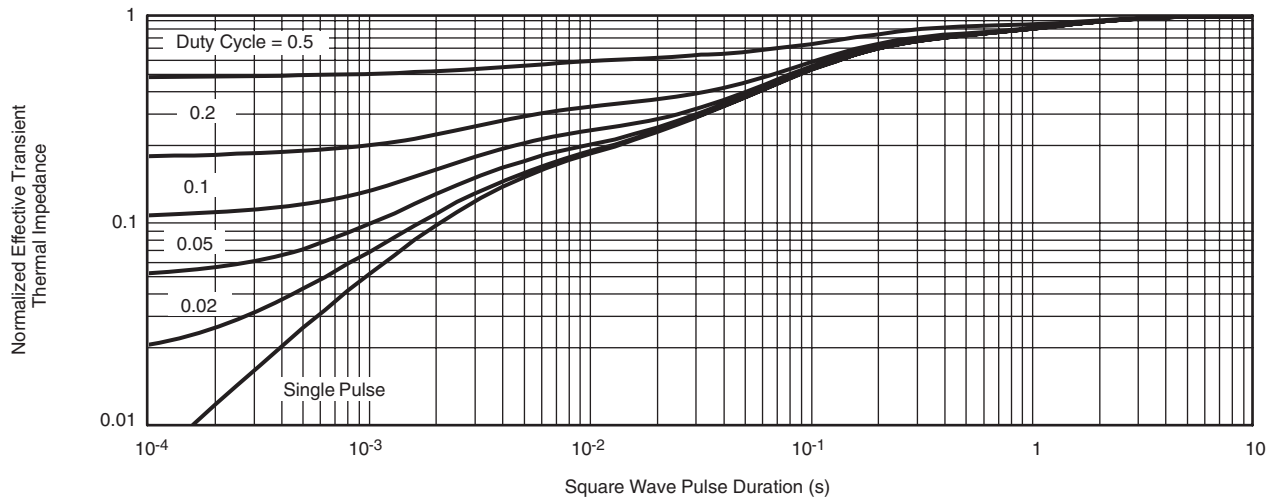
$T_A$  - Ambient Temperature (°C)  
**Power Derating, Junction-to-Ambient (Ch 2)**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Normalized Thermal Transient Impedance, Junction-to-Ambient (Ch 2)**



**Normalized Thermal Transient Impedance, Junction-to-Case (Ch 2)**

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