

N-Channel 2.5-V (G-S) Battery Switch, ESD Protection

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
28	0.033 at $V_{GS} = 4.5$ V	4.6
	0.038 at $V_{GS} = 3.0$ V	4.3
	0.042 at $V_{GS} = 2.5$ V	4.1

FEATURES

- Halogen-free
- Low $R_{DS(on)}$
- V_{GS} Max Rating: 14 V
- Exceeds 2 kV ESD Protection
- 28 V V_{DS} Rated
- Symmetrical Voltage Blocking (Off Voltage)

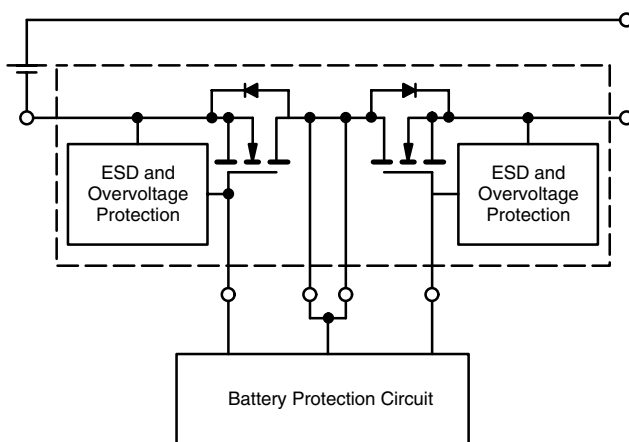

RoHS
COMPLIANT

DESCRIPTION

The Si6924AEDQ is a dual N-Channel MOSFET with ESD protection and gate over-voltage protection circuitry incorporated into the MOSFET. The device is designed for use in Lithium Ion battery pack circuits. The common-drain construction takes advantage of the typical battery pack topology, allowing a further reduction of the device's on-resistance. The 2-stage input protection circuit is a unique design, consisting of two stages of back-to-back zener diodes separated by a resistor. The first stage diode is designed to absorb most of the ESD energy. The second

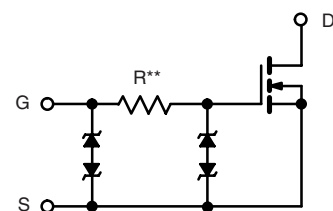
stage diode is designed to protect the gate from any remaining ESD energy and over-voltages above the gates inherent safe operating range. The series resistor used to limit the current through the second stage diode during over voltage conditions has a maximum value which limits the input current to ≤ 10 mA at 14 V and the maximum t_{off} to 12 μ s. The Si6924AEDQ has been optimized as a battery or load switch in Lithium Ion applications with the advantage of both a 2.5 V $R_{DS(on)}$ rating and a safe 14 V gate-to-source maximum rating.

APPLICATION CIRCUITS



*Thermal connection to drain pins is required to achieve specific performance

Figure 1. Typical Use In a Lithium Ion Battery Pack

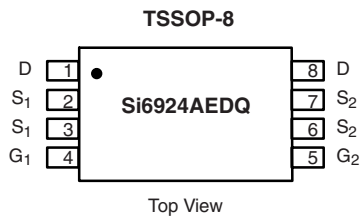


**R typical value is 3.3 k Ω by design.

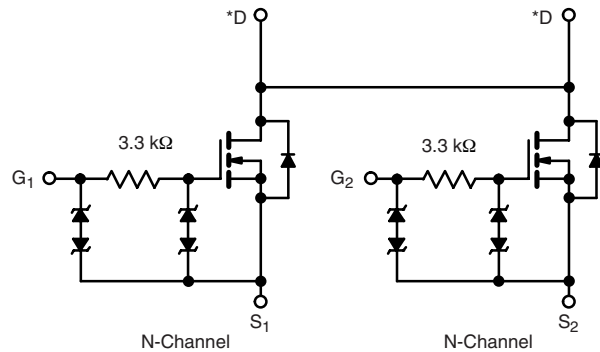
See Typical Characteristics, Gate-Current vs. Gate-Source Voltage, Page 3.

Figure 2. Input ESD and Overvoltage Protection Circuit

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View



N-Channel

N-Channel

Ordering Information: Si6924AEDQ-T1-GE3 (Lead (Pb)-free and Halogen-free)

*Thermal connection to drain pins is required to achieve specific performance.

Figure 3.

Figure 4.

ABSOLUTE MAXIMUM RATINGS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted					
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage, Source-Drain Voltage	V_{DS}	28		V	
Gate-Source Voltage	V_{GS}	± 14			
Continuous Drain-to-Source Current ($T_J = 150\text{ }^\circ\text{C}$) ^a	I_D	$T_A = 25\text{ }^\circ\text{C}$	4.6	4.1	A
		$T_A = 70\text{ }^\circ\text{C}$	3.7	3.2	
Pulsed Drain-to-Source Current	I_{DM}	20			
Pulsed Source Current (Diode Conduction) ^a	I_S	1.2	0.9		
Maximum Power Dissipation ^a	P_D	$T_A = 25\text{ }^\circ\text{C}$	1.3	1.0	W
		$T_A = 70\text{ }^\circ\text{C}$	0.84	0.64	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10\text{ s}$	R_{thJA}	71	95	$^\circ\text{C/W}$
	Steady State		96	125	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	56	70	

Notes:

a. Surface Mounted on FR4 board.



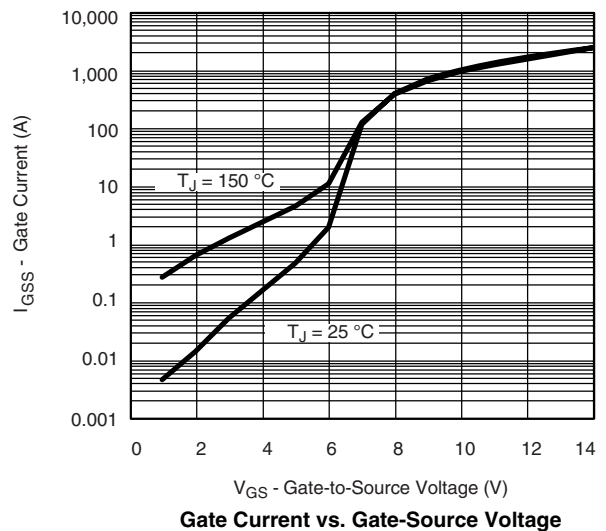
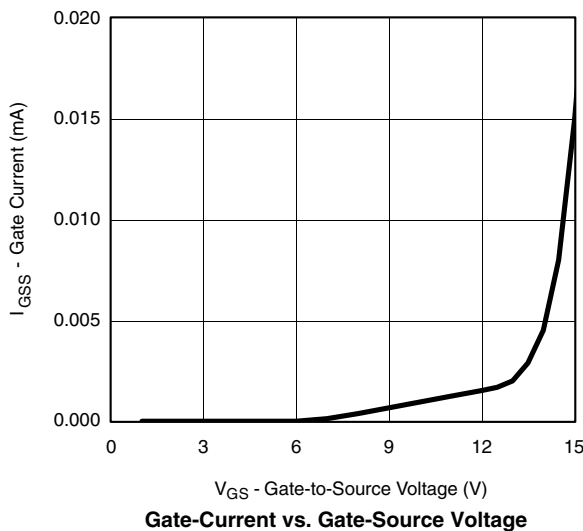
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.6		1.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$			± 1	μA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 14\text{ V}$			± 20	mA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 22.4\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 22.4\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 5\text{ V}$	10			A
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 4.6\text{ A}$		0.022	0.033	Ω
		$V_{GS} = 3.0\text{ V}, I_D = 4.3\text{ A}$		0.025	0.038	
		$V_{GS} = 2.5\text{ V}, I_D = 4.1\text{ A}$		0.029	0.042	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 4.6\text{ A}$		25		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.2\text{ A}, V_{GS} = 0\text{ V}$		0.7	1.1	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 4.6\text{ A}$		6.5	10	nC
Gate-Source Charge	Q_{gs}			1.2		
Gate-Drain Charge	Q_{gd}			1.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 4.5\text{ V}, R_G = 6\text{ }\Omega$		0.95	1.5	μs
Rise Time	t_r			1.4	2.1	
Turn-Off Delay Time	$t_{d(off)}$			7	11	
Fall Time	t_f			3.1	5	

Notes:

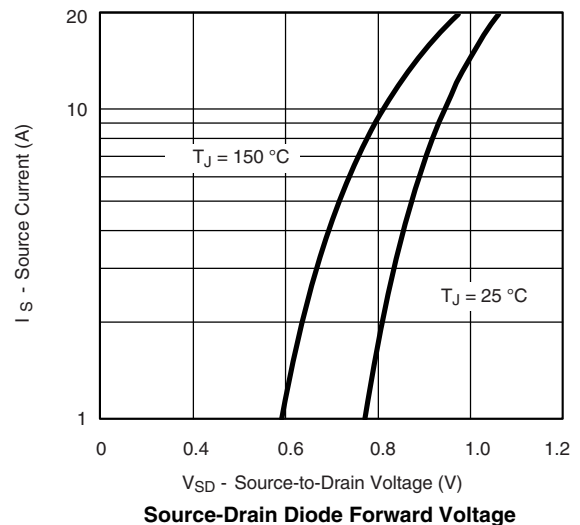
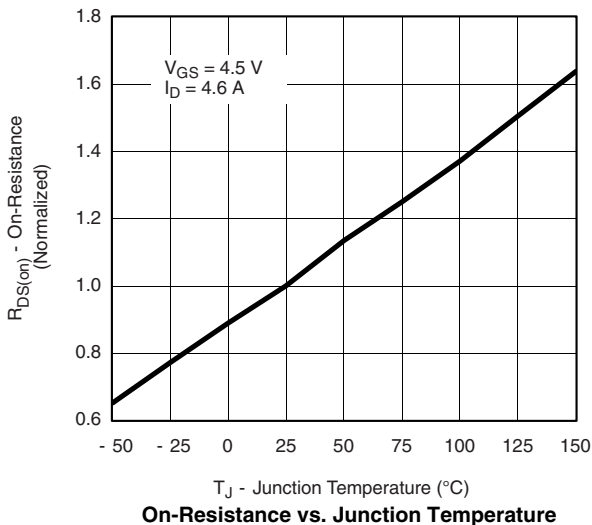
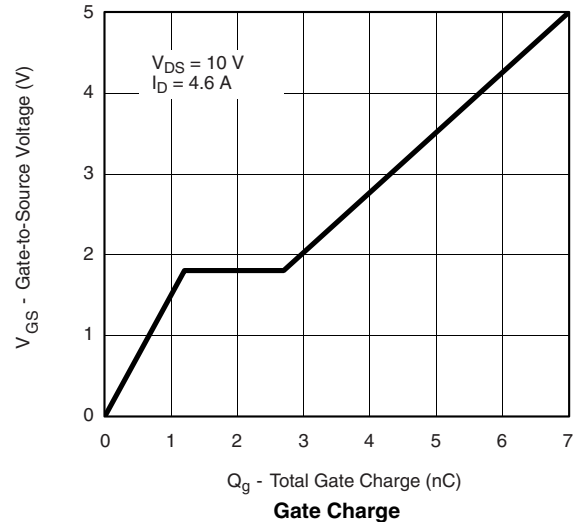
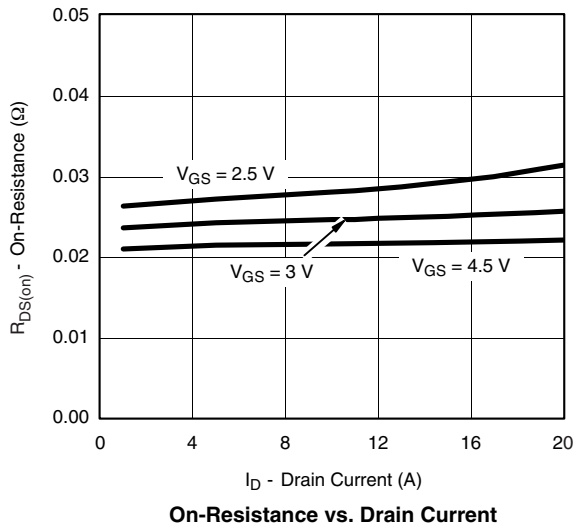
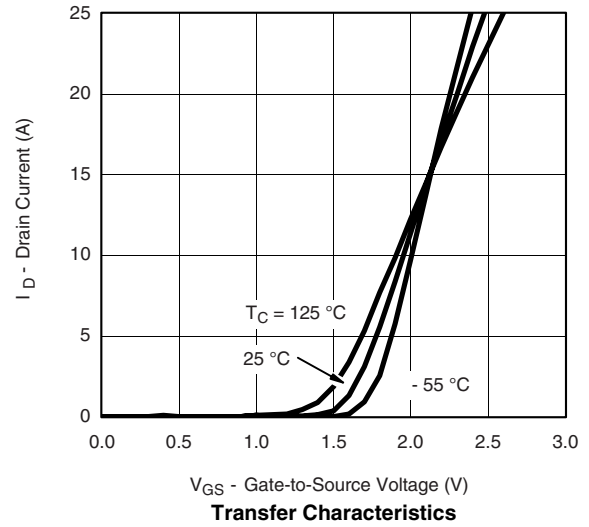
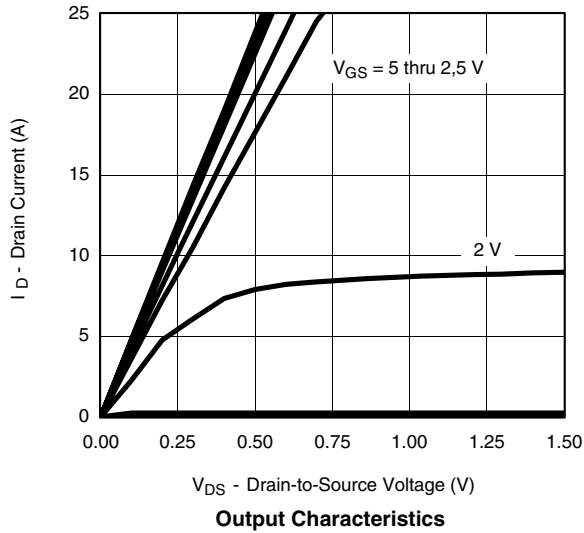
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

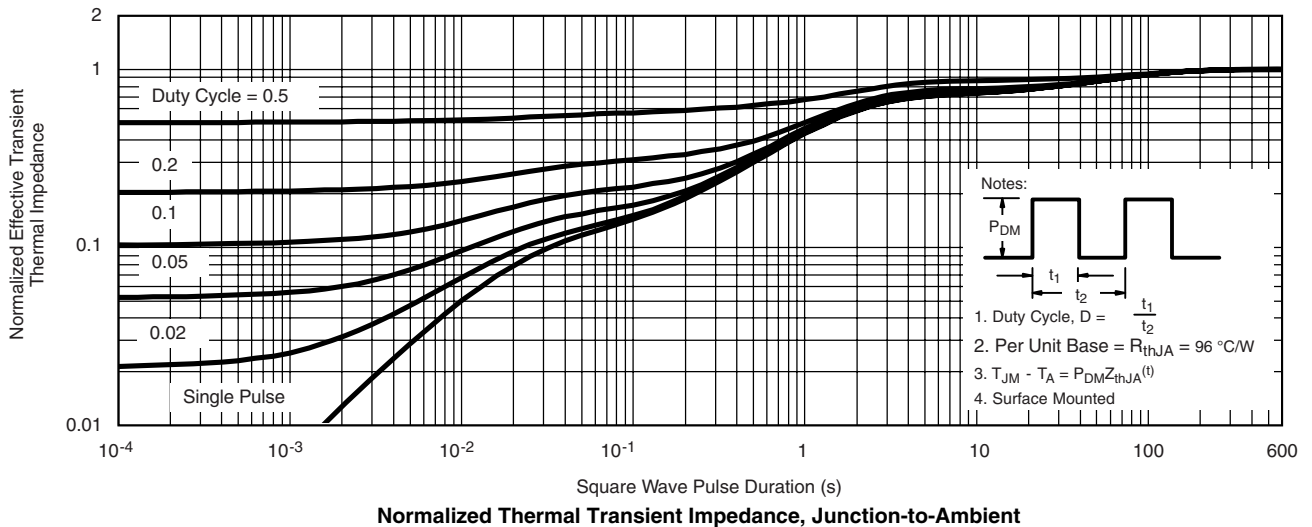
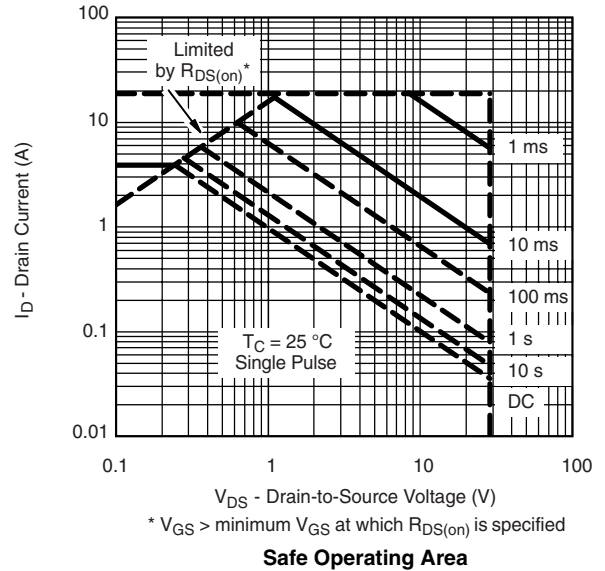
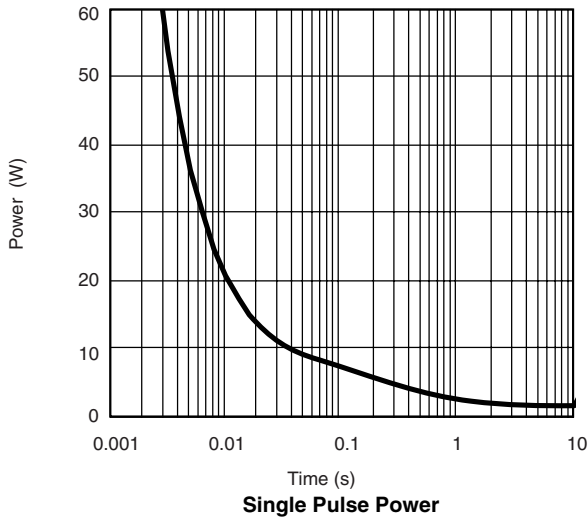
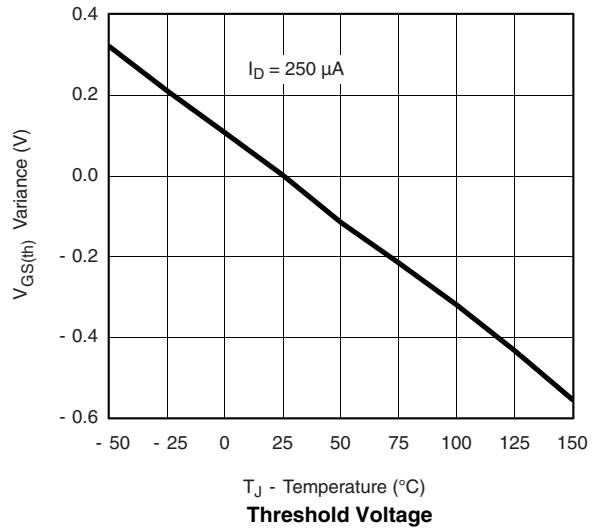
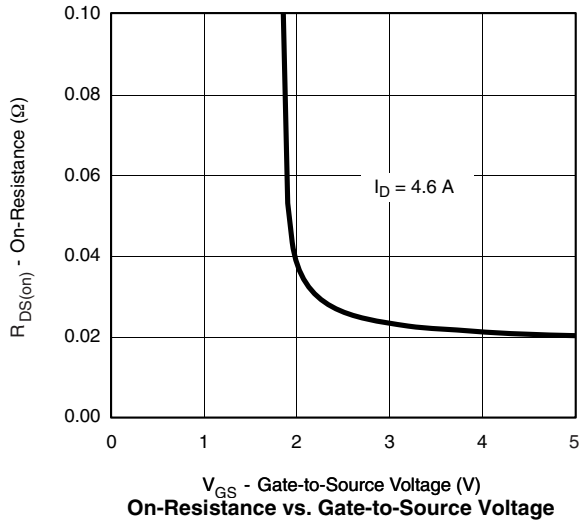
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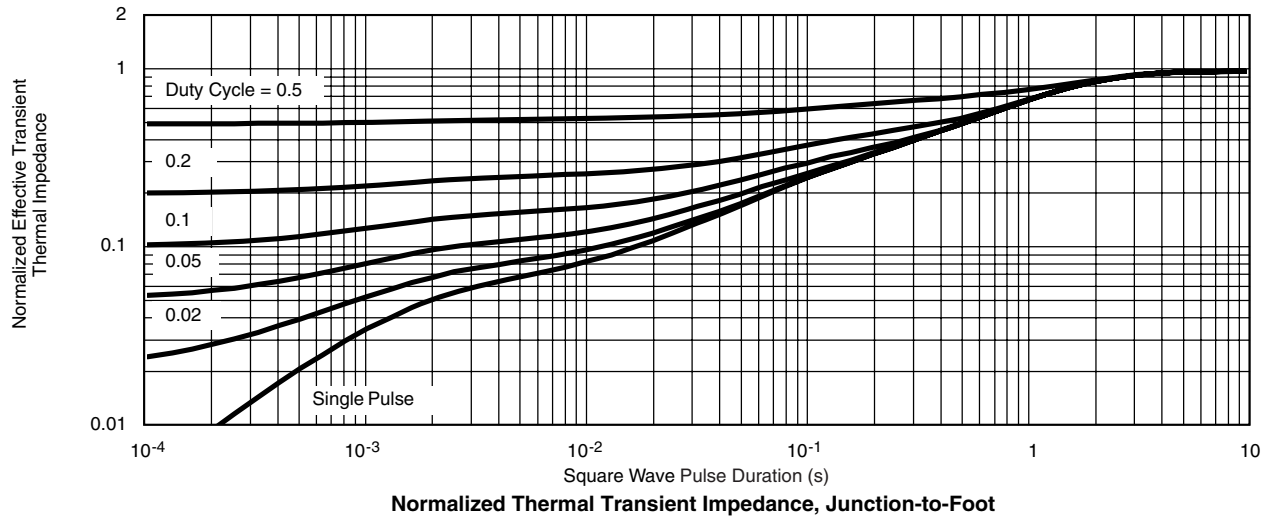
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