

Dual N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
Channel 1	30	0.035 at V _{GS} = 10 V	6 ^a	4.5 nC
		0.042 at V _{GS} = 4.5 V	6 ^a	
Channel 2	30	0.028 at V _{GS} = 10 V	6 ^a	5.5 nC
		0.035 at V _{GS} = 4.5 V	6 ^a	

FEATURES

- Halogen-free Option Available
- TrenchFET[®] Power MOSFETs

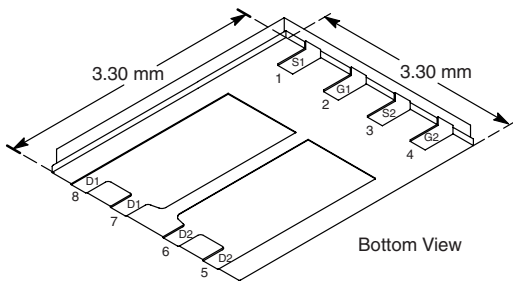


RoHS
COMPLIANT

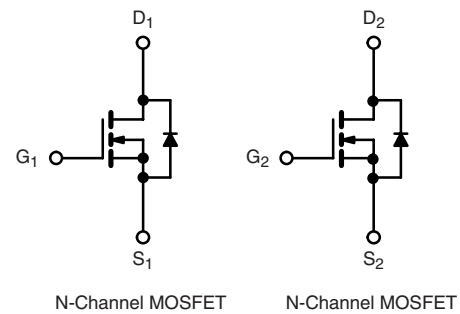
APPLICATIONS

- Notebook PC System Power
- Low Current POL

PowerPAK[®] 1212-8



Ordering Information: Si7224DN-T1-E3 (Lead (Pb)-free)
Si7224DN-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter	Symbol	Channel 1	Channel 2	Unit	
Drain-Source Voltage	V _{DS}	30	30	V	
Gate-Source Voltage	V _{GS}	± 16	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	6 ^a	A	
		T _C = 70 °C	6 ^a		
		T _A = 25 °C	6 ^{a, b, c}		
		T _A = 70 °C	5.2 ^{b, c}		
Pulsed Drain Current	I _{DM}	25	30		
Source Drain Current Diode Current	I _S	T _C = 25 °C	6 ^a		
		T _A = 25 °C	1.7 ^{b, c}		2.2 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	17.8	W	
		T _C = 70 °C	11.4		
		T _A = 25 °C	2.5 ^{b, c}		2.6 ^{b, c}
		T _A = 70 °C	1.6 ^{b, c}		1.7 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260			

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Channel 1		Channel 2		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R _{thJA}	40	50	38	48	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	5.6	7	4.3	5.4	

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 94 °C/W.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted								
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch 1	30		V		
			Ch 2	30				
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch 1		37	mV/ $^\circ\text{C}$		
			Ch 2		32			
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch 1		-5			
			Ch 2		-6			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch 1	1	2.2	V		
			Ch 2	1.5	3			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$	Ch 1		± 100	nA		
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Ch 2		± 100			
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch 1		1	μA		
			Ch 2		1			
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch 1		10			
			Ch 2		10			
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch 1	15		A		
			Ch 2	15				
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 6.5\text{ A}$	Ch 1		0.027	0.035	Ω	
		$V_{GS} = 10\text{ V}, I_D = 7.4\text{ A}$	Ch 2		0.022	0.028		
		$V_{GS} = 4.5\text{ V}, I_D = 5.9\text{ A}$	Ch 1		0.032	0.042		
		$V_{GS} = 4.5\text{ V}, I_D = 6.6\text{ A}$	Ch 2		0.029	0.035		
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 6.5\text{ A}$	Ch 1		22	S		
		$V_{DS} = 15\text{ V}, I_D = 7.4\text{ A}$	Ch 2		21			
Dynamic^a								
Input Capacitance	C_{iss}	Channel 1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch 1		570	pF		
			Ch 2		720			
Output Capacitance	C_{oss}		Channel 2 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch 1			80	
				Ch 2			115	
Reverse Transfer Capacitance	C_{rss}			Ch 1			35	
				Ch 2			50	
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 6.5\text{ A}$		Ch 1		9.5	14.5	nC
		$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 7.4\text{ A}$		Ch 2		12	18	
		Channel 1 $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 6.5\text{ A}$	Ch 1		4.5	7		
			Ch 2		5.5	8.5		
Gate-Source Charge	Q_{gs}	Channel 2 $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 7.4\text{ A}$	Ch 1		1.5			
			Ch 2		2.5			
Gate-Drain Charge	Q_{gd}		Ch 1		1.2			
			Ch 2		1.7			
Gate Resistance	R_g		$f = 1\text{ MHz}$	Ch 1		3.3	Ω	
				Ch 2		2.7		

Notes:

- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Dynamic^a							
Turn-On Delay Time	$t_{d(on)}$	Channel 1 $V_{DD} = 15\text{ V}$, $R_L = 2.9\text{ }\Omega$ $I_D \cong 5.2\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$	Ch 1		12	20	ns
Rise Time	t_r		Ch 2		20	30	
Turn-Off Delay Time	$t_{d(off)}$	Channel 2 $V_{DD} = 15\text{ V}$, $R_L = 2.6\text{ }\Omega$ $I_D \cong 5.9\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$	Ch 1		12	20	
			Ch 2		12	20	
Fall Time	t_f	Channel 1 $V_{DD} = 15\text{ V}$, $R_L = 2.9\text{ }\Omega$ $I_D \cong 5.2\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$	Ch 1		12	20	
			Ch 2		10	15	
Turn-On Delay Time	$t_{d(on)}$	Channel 2 $V_{DD} = 15\text{ V}$, $R_L = 2.6\text{ }\Omega$ $I_D \cong 5.9\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$	Ch 1		5	10	
			Ch 2		10	15	
Rise Time	t_r	Channel 1 $V_{DD} = 15\text{ V}$, $R_L = 2.9\text{ }\Omega$ $I_D \cong 5.2\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$	Ch 1		10	15	
			Ch 2		10	15	
Turn-Off Delay Time	$t_{d(off)}$	Channel 2 $V_{DD} = 15\text{ V}$, $R_L = 2.6\text{ }\Omega$ $I_D \cong 5.9\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$	Ch 1		15	25	
			Ch 2		15	25	
Fall Time	t_f	Channel 1 $V_{DD} = 15\text{ V}$, $R_L = 2.9\text{ }\Omega$ $I_D \cong 5.2\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$	Ch 1		10	15	
			Ch 2		10	15	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	Ch 1			6	A
			Ch 2			6	
Pulse Diode Forward Current ^a	I_{SM}		Ch 1			25	
			Ch 2			30	
Body Diode Voltage	V_{SD}	$I_S = 5.2\text{ A}$, $V_{GS} = 0\text{ V}$ $I_S = 5.9\text{ A}$, $V_{GS} = 0\text{ V}$	Ch 1		0.8	1.2	V
			Ch 2		0.8	1.2	
Body Diode Reverse Recovery Time	t_{rr}	Channel 1 $I_F = 5.2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	Ch 1		15	30	ns
			Ch 2		20	40	
Body Diode Reverse Recovery Charge	Q_{rr}	Channel 2 $I_F = 5.9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	Ch 1		10	20	nC
			Ch 2		12	20	
Reverse Recovery Fall Time	t_a	Channel 1 $I_F = 5.9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	Ch 1		9		ns
			Ch 2		12		
Reverse Recovery Rise Time	t_b	Channel 2 $I_F = 5.9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	Ch 1		6		
			Ch 2		8		

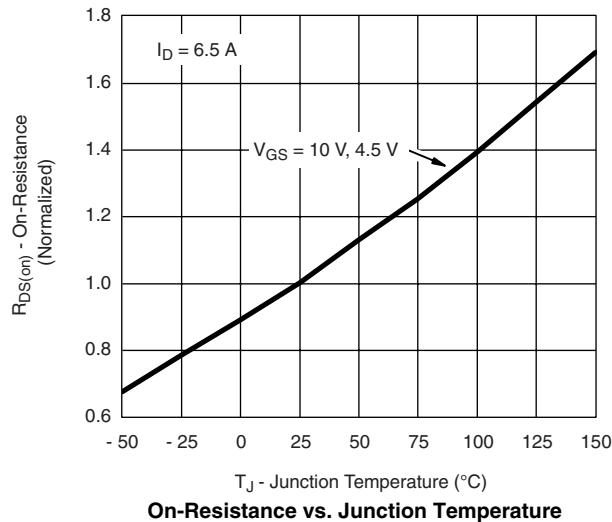
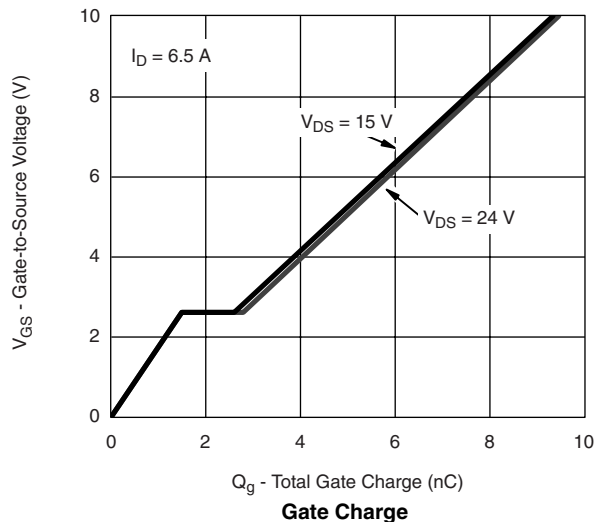
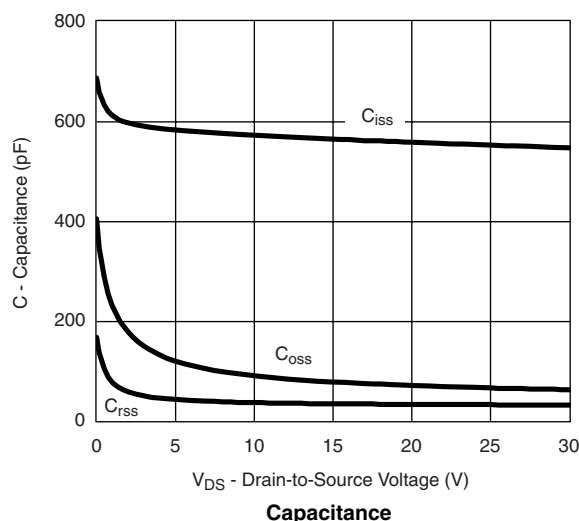
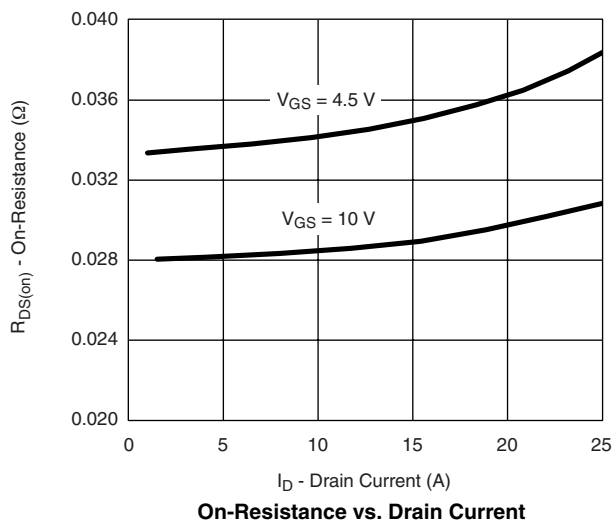
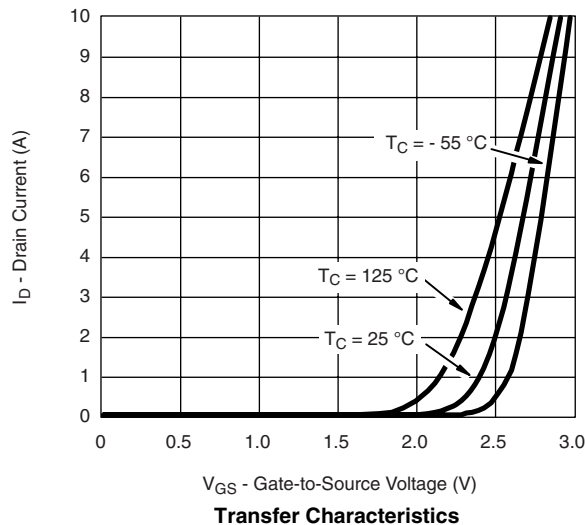
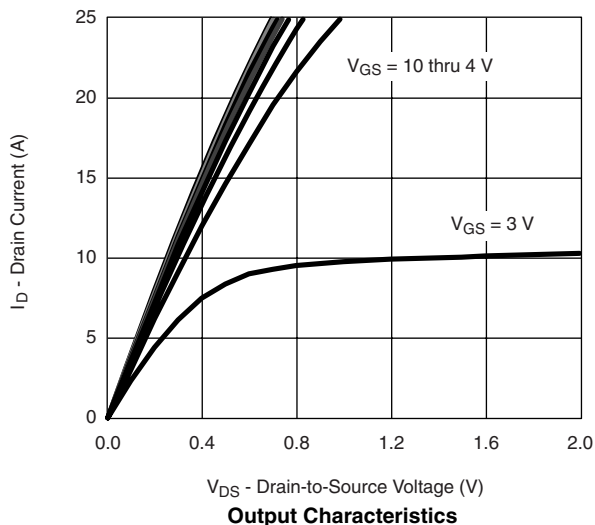
Notes:

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

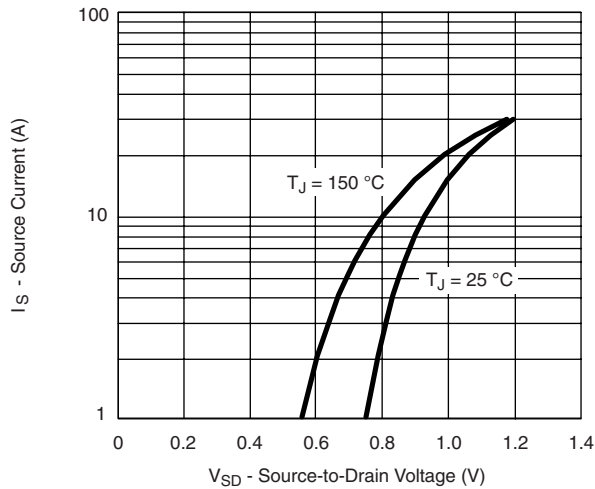


CHANNEL 1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

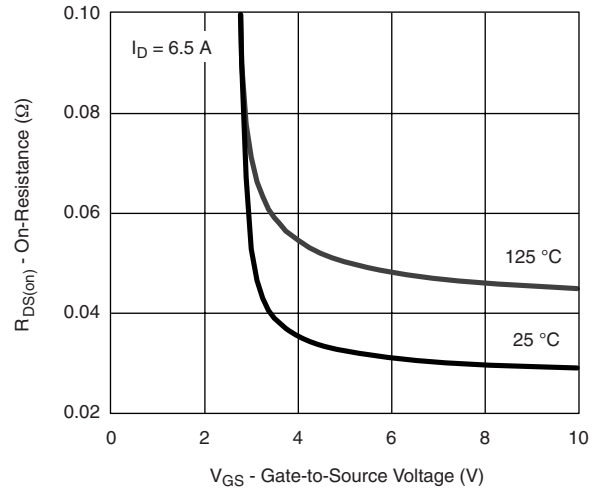




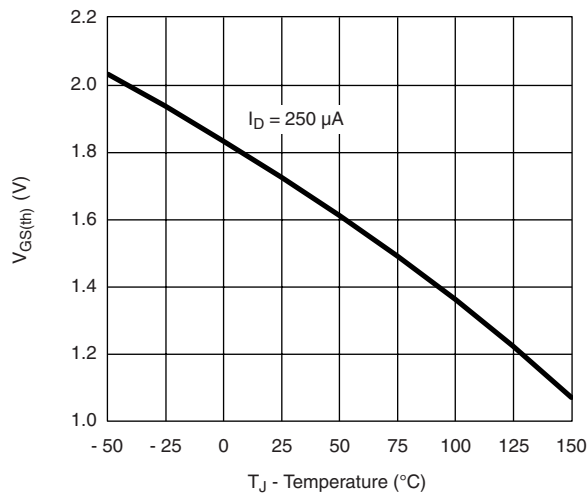
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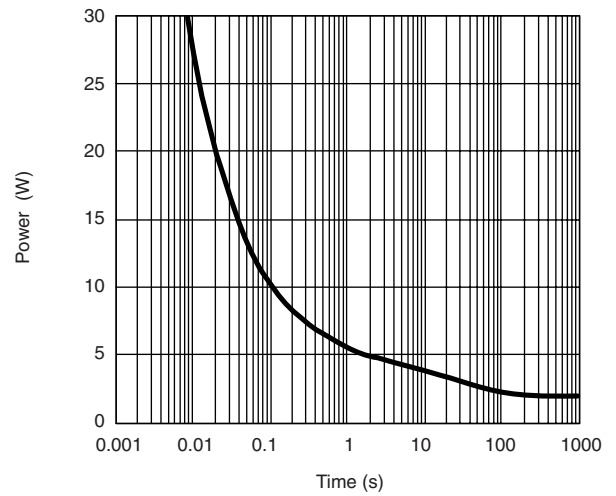
Source-Drain Diode Forward Voltage



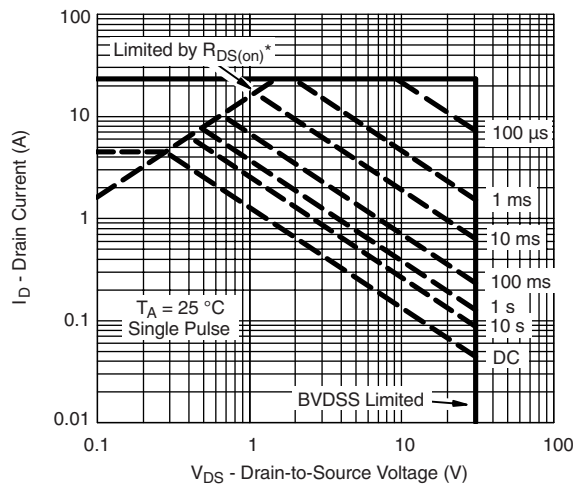
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power

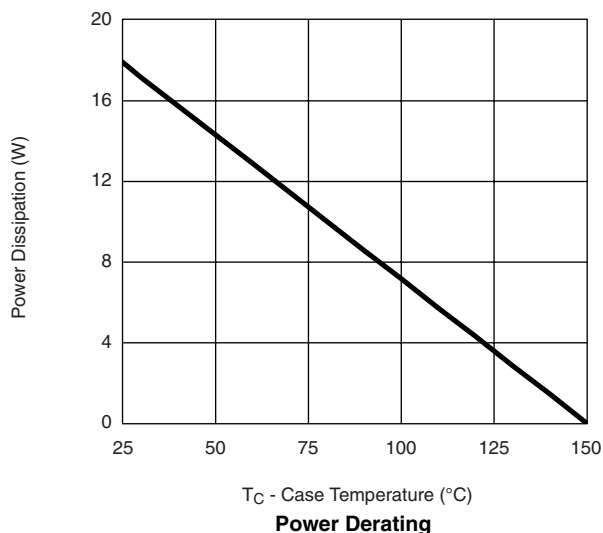
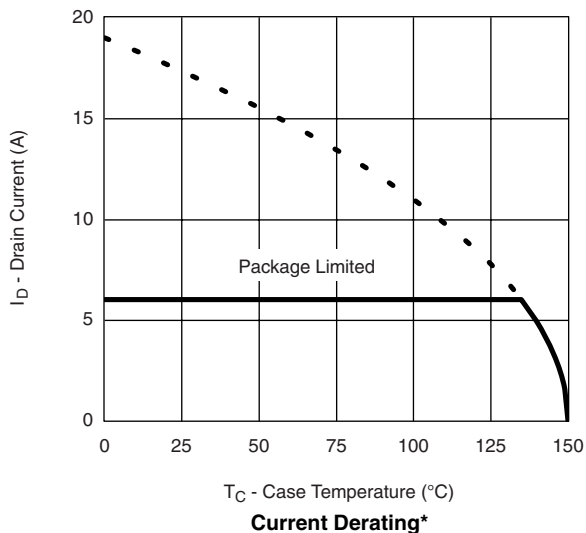


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



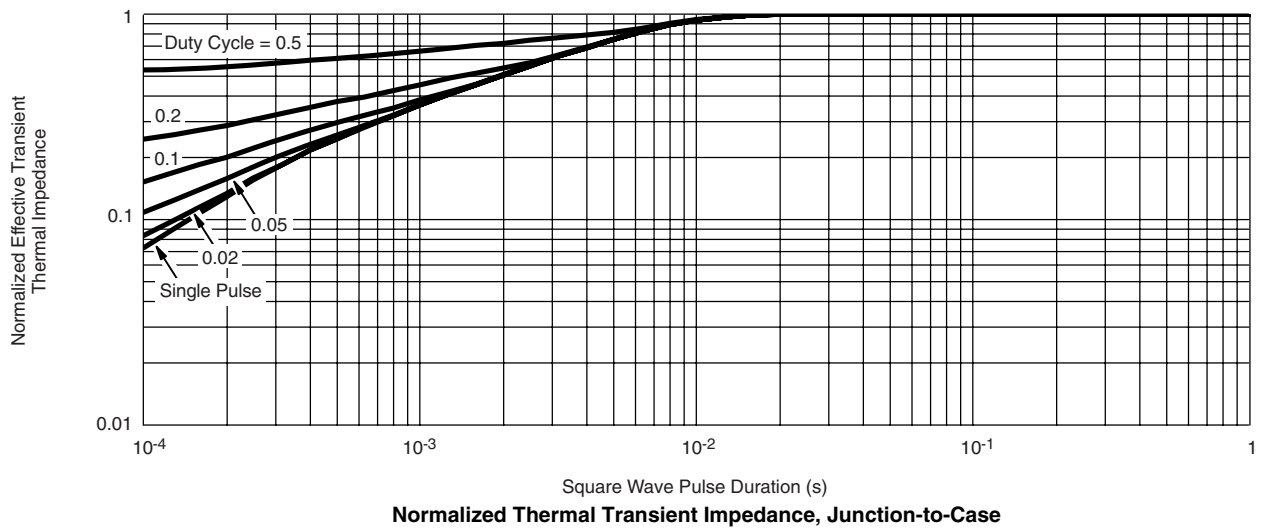
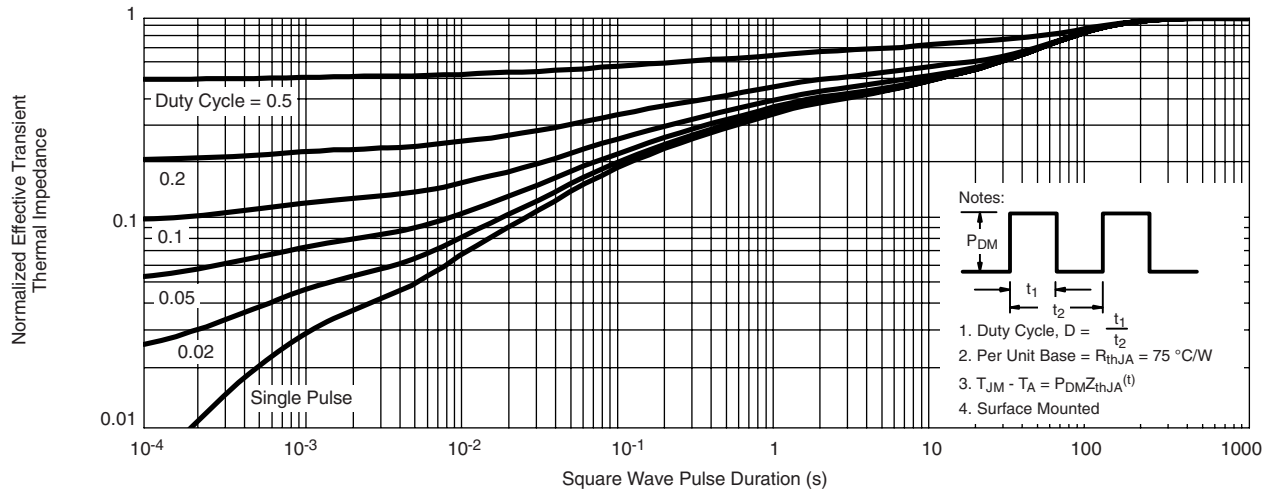
CHANNEL 1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

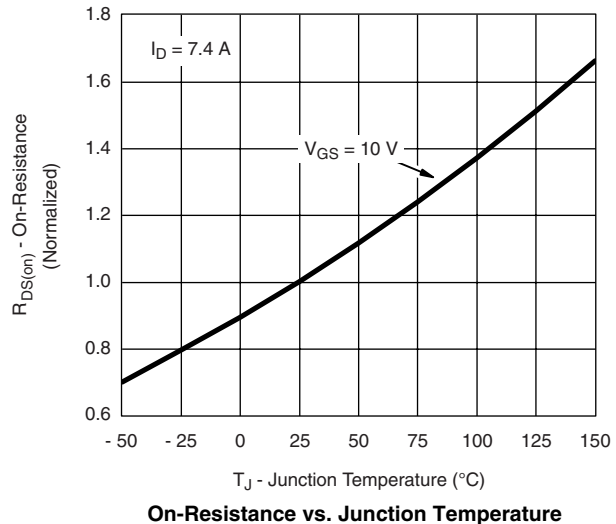
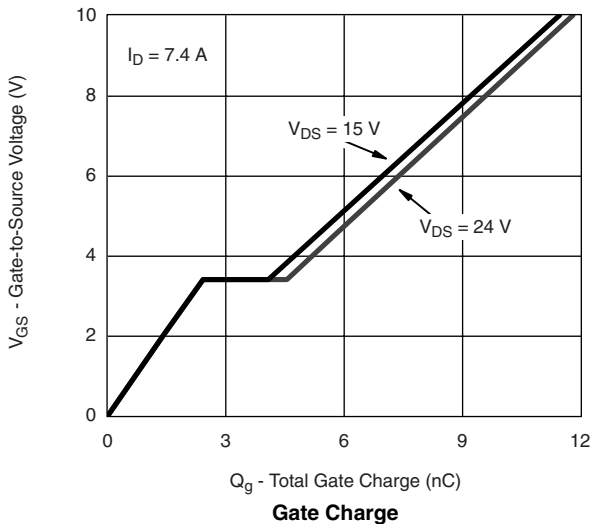
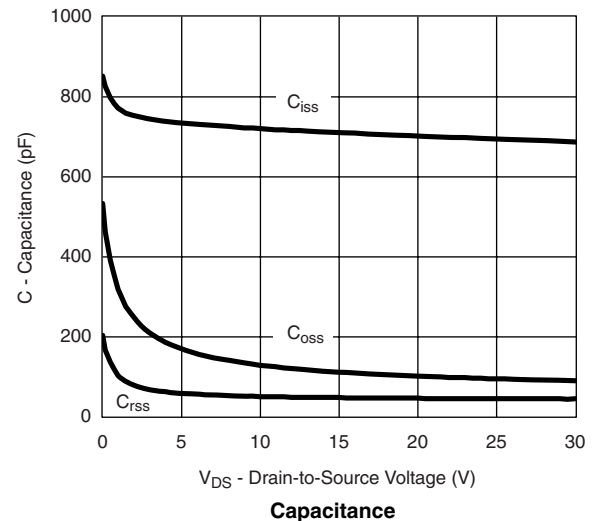
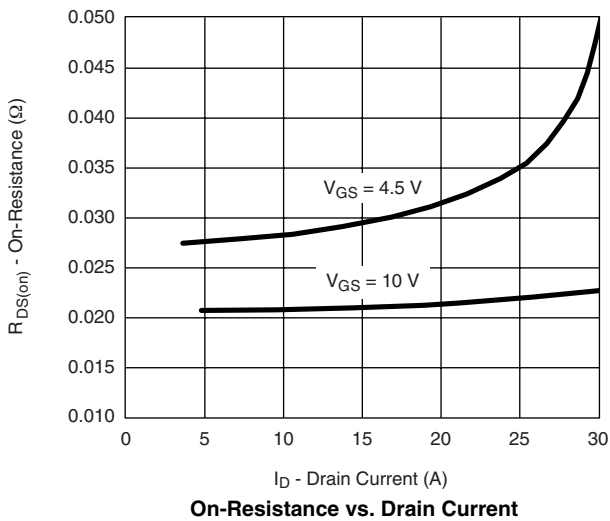
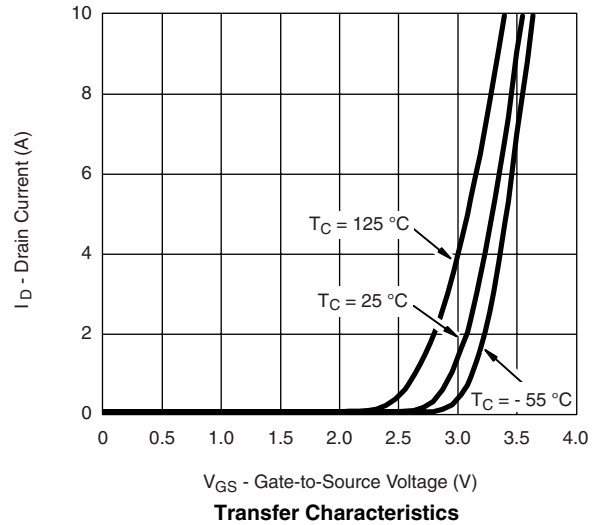
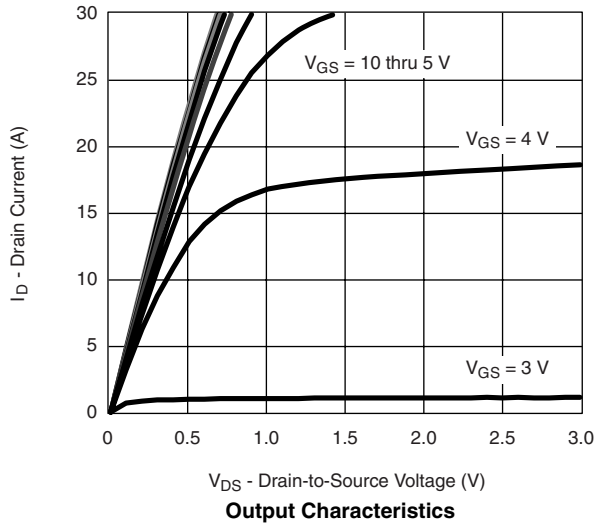


CHANNEL 1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



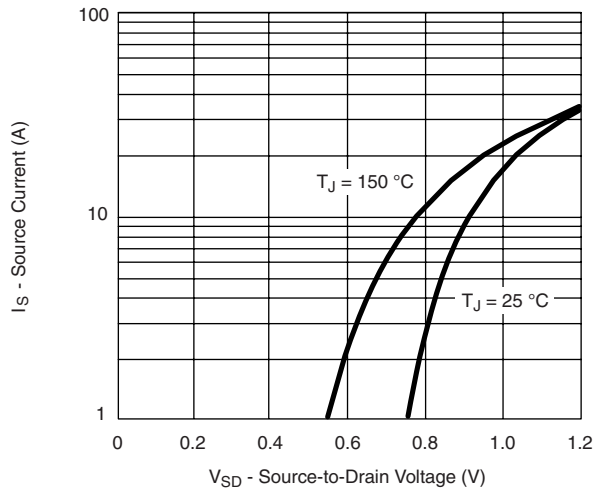


CHANNEL 2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

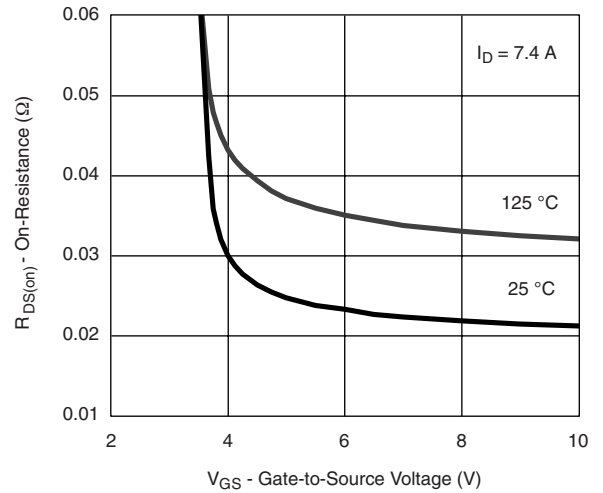




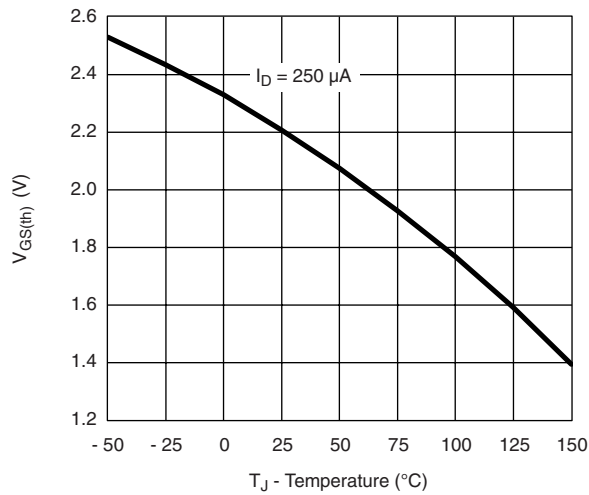
CHANNEL 2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



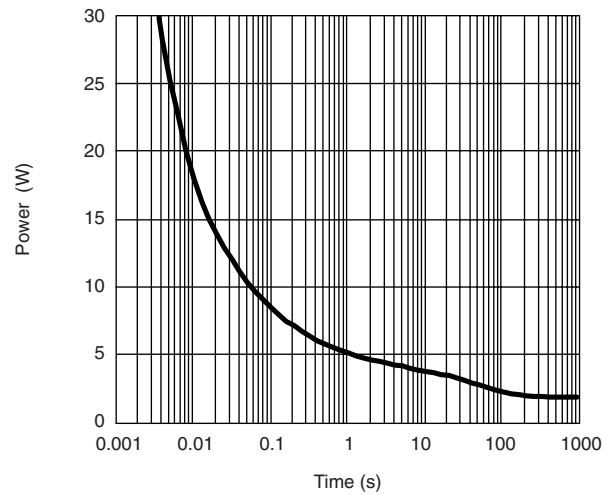
Source-Drain Diode Forward Voltage



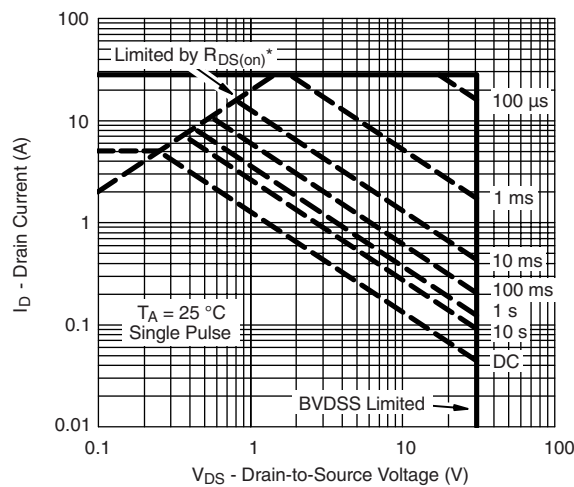
On-Resistance vs. Gate-to-Source



Threshold Voltage



Single Pulse Power

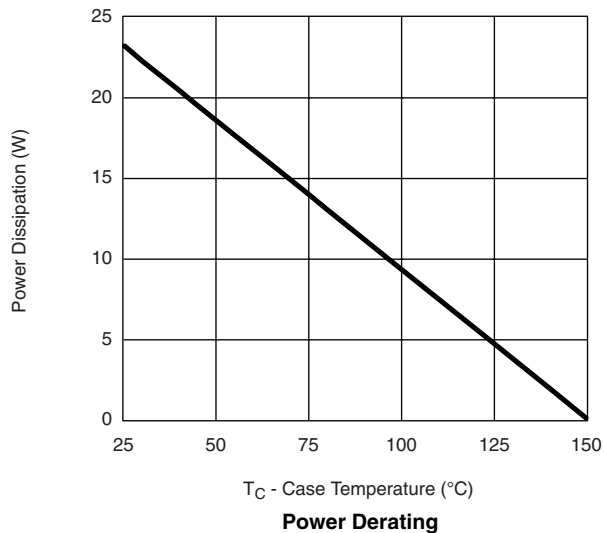
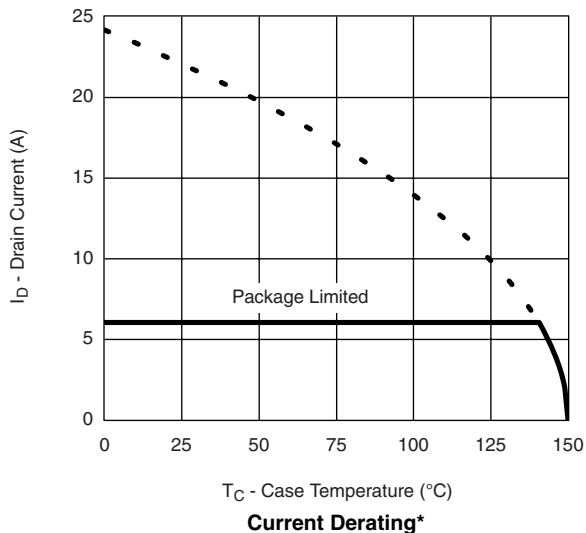


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



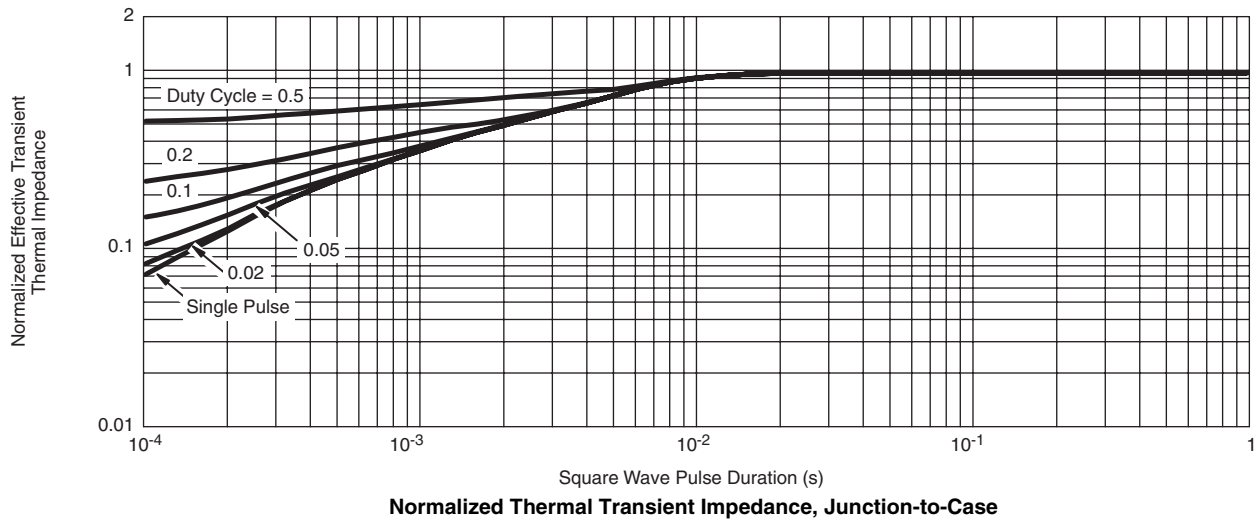
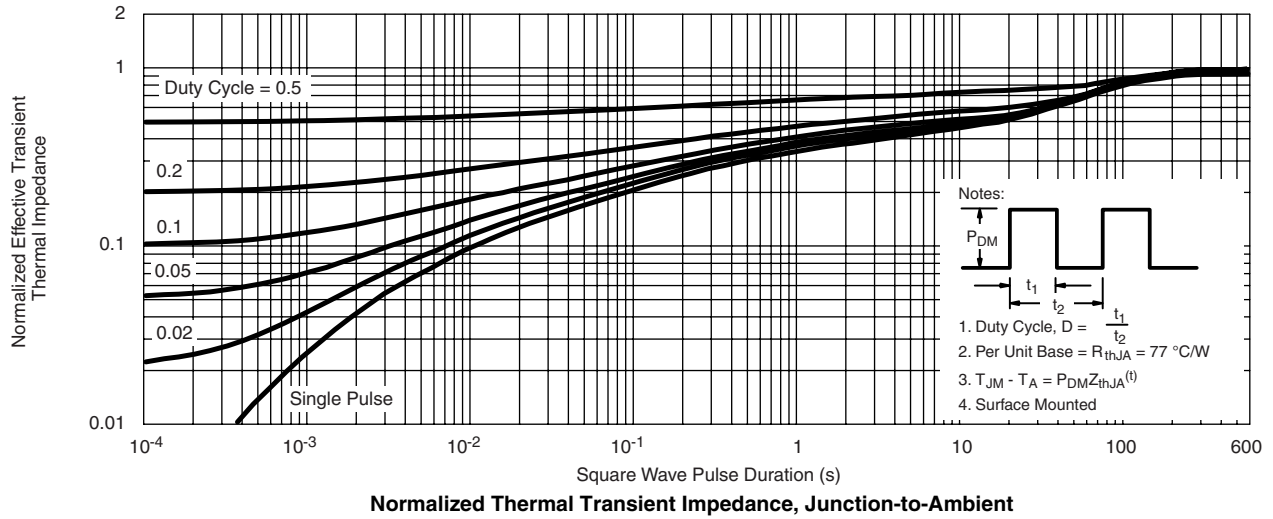
CHANNEL 2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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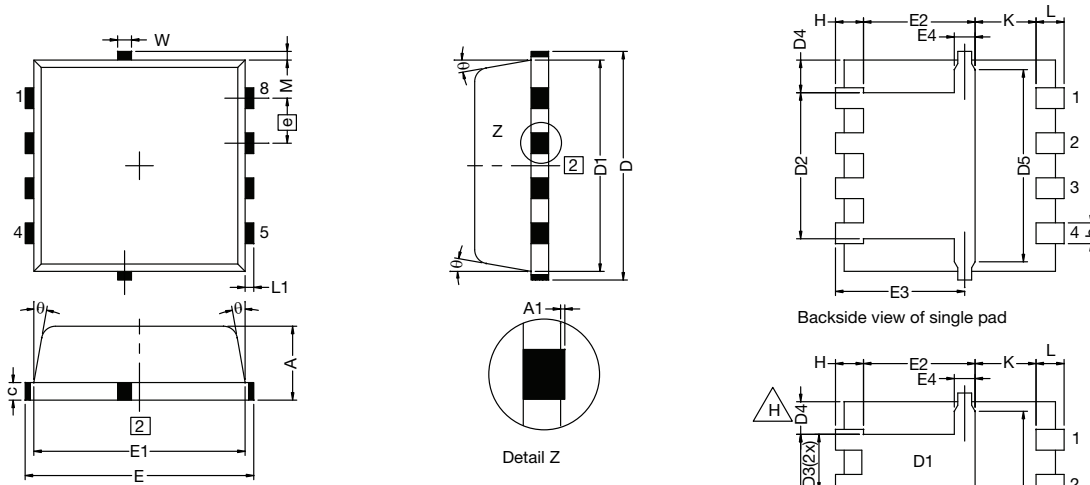
CHANNEL 2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?69500>.



PowerPAK® 1212-8, (Single / Dual)



- Notes**
 1. Inch will govern
 [2] Dimensions exclusive of mold gate burrs
 3. Dimensions exclusive of mold flash and cutting burrs

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 typ.			0.0185 typ		
D5	2.3 typ.			0.090 typ		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.034 typ.			0.013 typ.		
e	0.65 BSC			0.026 BSC		
K	0.86 typ.			0.034 typ.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		

ECN: S16-2667-Rev. M, 09-Jan-17
 DWG: 5882

PowerPAK[®] 1212 Mounting and Thermal Considerations

Johnson Zhao

MOSFETs for switching applications are now available with die on resistances around 1 mΩ and with the capability to handle 85 A. While these die capabilities represent a major advance over what was available just a few years ago, it is important for power MOSFET packaging technology to keep pace. It should be obvious that degradation of a high performance die by the package is undesirable. PowerPAK is a new package technology that addresses these issues. The PowerPAK 1212-8 provides ultra-low thermal impedance in a small package that is ideal for space-constrained applications. In this application note, the PowerPAK 1212-8's construction is described. Following this, mounting information is presented. Finally, thermal and electrical performance is discussed.

THE PowerPAK PACKAGE

The PowerPAK 1212-8 package (Figure 1) is a derivative of PowerPAK SO-8. It utilizes the same packaging technology, maximizing the die area. The bottom of the die attach pad is exposed to provide a direct, low resistance thermal path to the substrate the device is mounted on. The PowerPAK 1212-8 thus translates the benefits of the PowerPAK SO-8 into a smaller package, with the same level of thermal performance. (Please refer to application note "PowerPAK SO-8 Mounting and Thermal Considerations.")

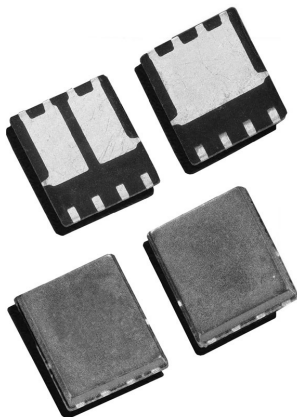


Figure 1. PowerPAK 1212 Devices

The PowerPAK 1212-8 has a footprint area comparable to TSOP-6. It is over 40 % smaller than standard TSSOP-8. Its die capacity is more than twice the size of the standard TSOP-6's. It has thermal performance an order of magnitude better than the SO-8, and 20 times better than TSSOP-8. Its thermal performance is better than all current SMT packages in the market. It will take the advantage of any PC board heat sink capability. Bringing the junction temperature down also increases the die efficiency by around 20 % compared with TSSOP-8. For applications where bigger packages are typically required solely for thermal consideration, the PowerPAK 1212-8 is a good option.

Both the single and dual PowerPAK 1212-8 utilize the same pin-outs as the single and dual PowerPAK SO-8. The low 1.05 mm PowerPAK height profile makes both versions an excellent choice for applications with space constraints.

PowerPAK 1212 SINGLE MOUNTING

To take the advantage of the single PowerPAK 1212-8's thermal performance see Application Note 826, [*Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*](#). Click on the PowerPAK 1212-8 single in the index of this document.

In this figure, the drain land pattern is given to make full contact to the drain pad on the PowerPAK package.

This land pattern can be extended to the left, right, and top of the drawn pattern. This extension will serve to increase the heat dissipation by decreasing the thermal resistance from the foot of the PowerPAK to the PC board and therefore to the ambient. Note that increasing the drain land area beyond a certain point will yield little decrease in foot-to-board and foot-to-ambient thermal resistance. Under specific conditions of board configuration, copper weight, and layer stack, experiments have found that adding copper beyond an area of about 0.3 to 0.5 in² of will yield little improvement in thermal performance.

PowerPAK 1212 DUAL

To take the advantage of the dual PowerPAK 1212-8's thermal performance, the minimum recommended land pattern can be found in Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*. Click on the PowerPAK 1212-8 dual in the index of this document.

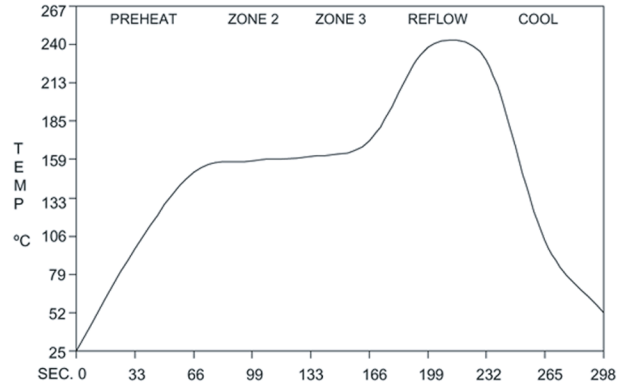
The gap between the two drain pads is 10 mils. This matches the spacing of the two drain pads on the PowerPAK 1212-8 dual package.

This land pattern can be extended to the left, right, and top of the drawn pattern. This extension will serve to increase the heat dissipation by decreasing the thermal resistance from the foot of the PowerPAK to the PC board and therefore to the ambient. Note that increasing the drain land area beyond a certain point will yield little decrease in foot-to-board and foot-to-ambient thermal resistance. Under specific conditions of board configuration, copper weight, and layer stack, experiments have found that adding copper beyond an area of about 0.3 to 0.5 in² of will yield little improvement in thermal performance.

REFLOW SOLDERING

Vishay Siliconix surface-mount packages meet solder reflow reliability requirements. Devices are subjected to solder reflow as a preconditioning test and are then reliability-tested using temperature cycle, bias humidity, HAST, or pressure pot. The solder reflow tempera-

ture profile used, and the temperatures and time duration, are shown in Figures 2 and 3. For the lead (Pb)-free solder profile, see <http://www.vishay.com/doc?73257>.



Ramp-Up Rate	+ 6 °C /Second Maximum
Temperature at 155 ± 15 °C	120 Seconds Maximum
Temperature Above 180 °C	70 - 180 Seconds
Maximum Temperature	240 + 5/- 0 °C
Time at Maximum Temperature	20 - 40 Seconds
Ramp-Down Rate	+ 6 °C/Second Maximum

Figure 2. Solder Reflow Temperature Profile

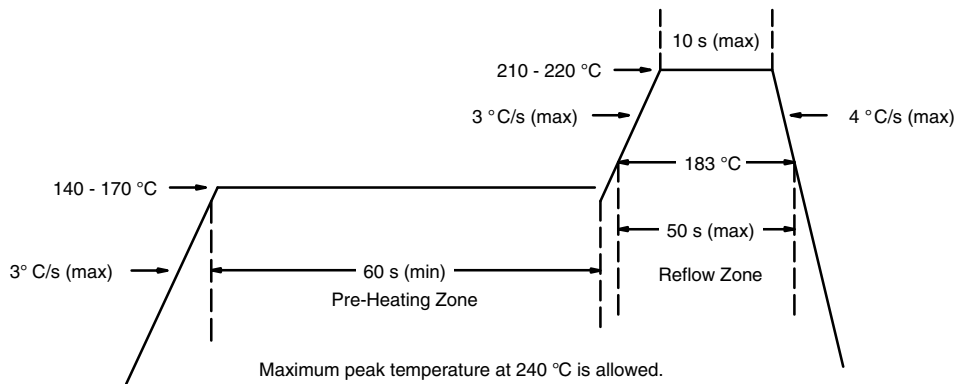
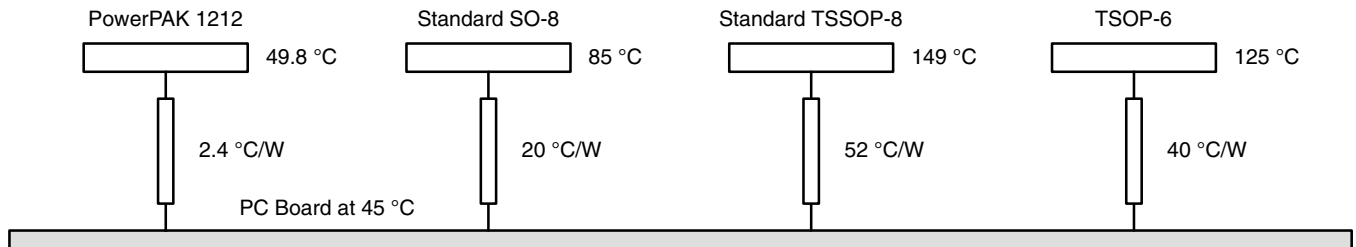


Figure 3. Solder Reflow Temperatures and Time Durations

TABLE 1: EQUIVALENT STEADY STATE PERFORMANCE

Package	SO-8		TSSOP-8		TSOP-8		PPAK 1212		PPAK SO-8	
Configuration	Single	Dual	Single	Dual	Single	Dual	Single	Dual	Single	Dual
Thermal Resistance $R_{thJC}(C/W)$	20	40	52	83	40	90	2.4	5.5	1.8	5.5


Figure 4. Temperature of Devices on a PC Board

THERMAL PERFORMANCE

Introduction

A basic measure of a device's thermal performance is the junction-to-case thermal resistance, $R_{\theta jc}$, or the junction to-foot thermal resistance, $R_{\theta jf}$. This parameter is measured for the device mounted to an infinite heat sink and is therefore a characterization of the device only, in other words, independent of the properties of the object to which the device is mounted. Table 1 shows a comparison of the PowerPAK 1212-8, PowerPAK SO-8, standard TSSOP-8 and SO-8 equivalent steady state performance.

By minimizing the junction-to-foot thermal resistance, the MOSFET die temperature is very close to the temperature of the PC board. Consider four devices mounted on a PC board with a board temperature of 45 °C (Figure 4). Suppose each device is dissipating 2 W. Using the junction-to-foot thermal resistance characteristics of the PowerPAK 1212-8 and the other SMT packages, die temperatures are determined to be 49.8 °C for the PowerPAK 1212-8, 85 °C for the standard SO-8, 149 °C for standard TSSOP-8, and 125 °C for TSOP-6. This is a 4.8 °C rise above the board temperature for the PowerPAK 1212-8, and over 40 °C for other SMT packages. A 4.8 °C rise has minimal effect on $r_{DS(ON)}$ whereas a rise of over 40 °C will cause an increase in $r_{DS(ON)}$ as high as 20 %.

Spreading Copper

Designers add additional copper, spreading copper, to the drain pad to aid in conducting heat from a device. It is helpful to have some information about the thermal performance for a given area of spreading copper.

Figure 5 and Figure 6 show the thermal resistance of a PowerPAK 1212-8 single and dual devices mounted on a 2-in. x 2-in., four-layer FR-4 PC boards. The two internal layers and the backside layer are solid copper. The internal layers were chosen as solid copper to model the large power and ground planes common in many applications. The top layer was cut back to a smaller area and at each step junction-to-ambient thermal resistance measurements were taken. The results indicate that an area above 0.2 to 0.3 square inches of spreading copper gives no additional thermal performance improvement. A subsequent experiment was run where the copper on the back-side was reduced, first to 50 % in stripes to mimic circuit traces, and then totally removed. No significant effect was observed.

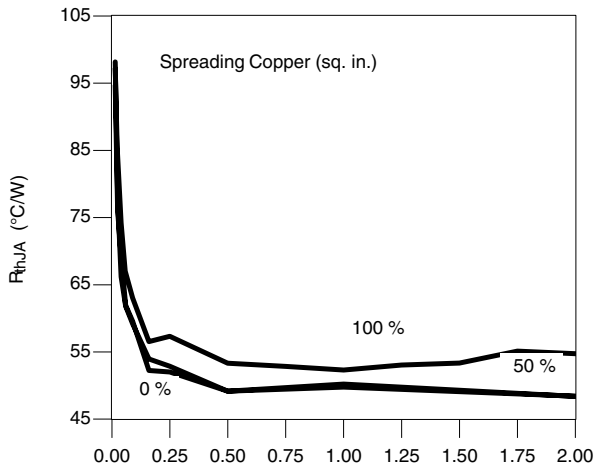


Figure 5. Spreading Copper - Si7401DN

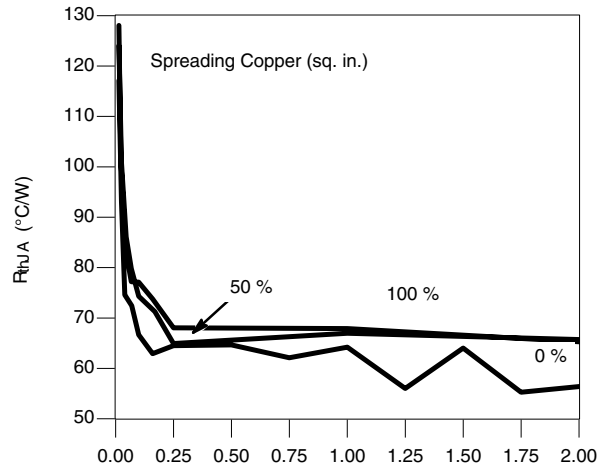


Figure 6. Spreading Copper - Junction-to-Ambient Performance

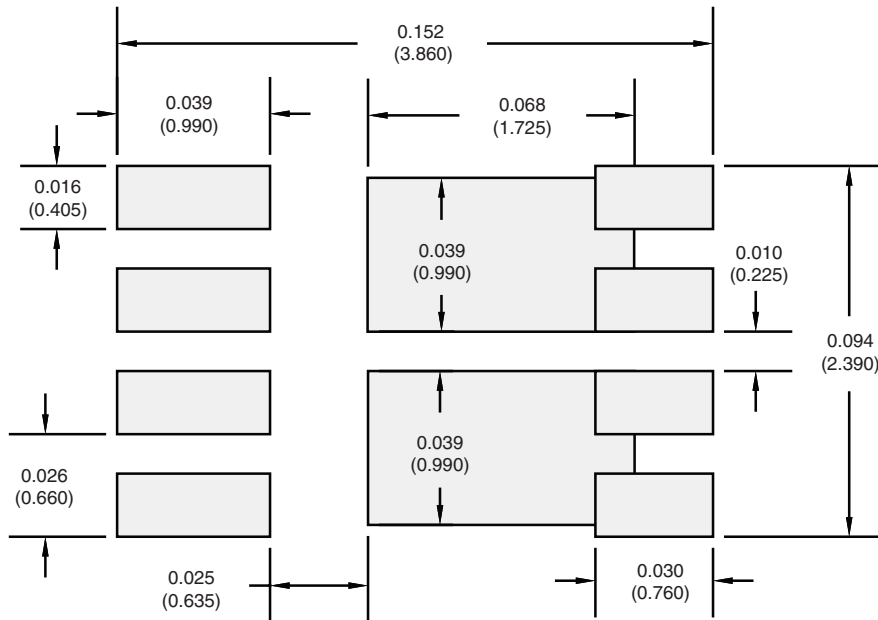
CONCLUSIONS

As a derivative of the PowerPAK SO-8, the PowerPAK 1212-8 uses the same packaging technology and has been shown to have the same level of thermal performance while having a footprint that is more than 40 % smaller than the standard TSSOP-8.

Recommended PowerPAK 1212-8 land patterns are provided to aid in PC board layout for designs using this new package.

The PowerPAK 1212-8 combines small size with attractive thermal characteristics. By minimizing the thermal rise above the board temperature, PowerPAK simplifies thermal design considerations, allows the device to run cooler, keeps $r_{DS(ON)}$ low, and permits the device to handle more current than a same- or larger-size MOSFET die in the standard TSSOP-8 or SO-8 packages.

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Dual



Recommended Minimum PADS for PowerPAK 1212-8 Dual
Dimensions in Inches/(mm)

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