

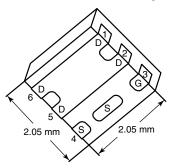
www.vishay.com

Vishay Siliconix

P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY									
V _{DS} (V)	R _{DS(on)} (Ω) (Max.)	I _D (A) ^a	Q _g (Typ.)						
- 20	0.0350 at V _{GS} = - 4.5 V	- 9							
	0.0395 at V _{GS} = - 3.7 V	- 9	10 nC						
	0.0620 at V _{GS} = - 2.5 V	- 9							

PowerPAK SC-70-6L-Single



Ordering Information:SiA459EDJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

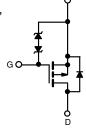
- TrenchFET® Power MOSFET
- Thermally Enhanced PowerPAK® SC-70 Package



- Low On-Resistance
- 100 % R_g Tested
- Typical ESD Protection: 2000 V (HBM)
- Material categorization: For definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Portable Devices such as Smart Phones, Tablet PCs and Mobile Computing
 - DC/DC Converter
 - Battery Switch
 - Load Switch
 - Power Management

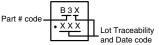


RoHS

COMPLIANT HALOGEN

FREE

Marking Code



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless	otherwise note	d)		
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	- 20	V	
Gate-Source Voltage		V _{GS}	± 12	v	
	T _C = 25 °C		- 9 ^a		
Continuous Drain Current /T 150 °C)	T _C = 70 °C	, [- 9 ^a		
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	- 7.4 ^{b, c}		
	T _A = 70 °C		- 6 ^{b, c}	A	
Pulsed Drain Current (t = 100 μs)	<u>.</u>	I _{DM}	- 40		
Continuous Source-Drain Diode Current	T _C = 25 °C	,	- 9 ^a		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	- 2.4 ^{b, c}		
	T _C = 25 °C		15.6		
Martin or Brown Black attack	T _C = 70 °C		10	١,,,	
Maximum Power Dissipation	T _A = 25 °C	P _D	2.9 ^{b, c}	W	
	T _A = 70 °C		1.8 ^{b, c}		
Operating Junction and Storage Temperature Ra	T _J , T _{stg}	- 50 to 150	°C		
Soldering Recommendations (Peak Temperature		260			

THERMAL RESISTANCE RATINGS									
Parameter		Symbol	Typical	Maximum	Unit				
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	32	43	°C/W				
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	6	8	C/W				

Notes

- a. Package limited.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 80 °C/W.



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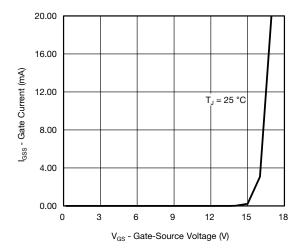
Parameter	Symbol Test Conditions		Min.	Тур.	Max.	Unit
Static				L	L	
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	- 20			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$			- 12		mV/°C
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = - 250 μA		2.2		
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \mu A$	- 0.6		- 1.2	V
Octo Course Lecliens		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 10	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$			± 0.5	
Zon Oale Vellere Build Oansel		V _{DS} = - 20 V, V _{GS} = 0 V			- 1	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	- 10			Α
		V _{GS} = - 4.5 V, I _D = - 5 A		0.0280	0.0350	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 3.7 V, I _D = - 5 A		0.0310	0.0395	Ω
		V _{GS} = - 2.5 V, I _D = - 2 A		0.0450	0.0620	
Forward Transconductance ^a	9 _{fs}	V _{GS} = - 10 V, I _D = - 5 A		15		S
Dynamic ^b						
Input Capacitance	C _{iss}			885		pF
Output Capacitance	C _{oss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		155		
Reverse Transfer Capacitance	C _{rss}			140		
Total Cata Charge	0	$V_{DS} = -10 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -5 \text{ A}$		20	30	nC
Total Gate Charge	Q_g			10	15	
Gate-Source Charge	Q_{gs}	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -5 \text{ A}$		1.6		
Gate-Drain Charge	Q_{gd}			2.9		
Gate Resistance	R_g	f = 1 MHz	2.2	11	22	Ω
Turn-On Delay Time	t _{d(on)}			20	40	
Rise Time	t _r	V_{DD} = - 10 V, R_L = 1.67 Ω		25	50	
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ - 6 A, $V_{GEN}=$ - 4.5 V, $R_g=$ 1 Ω		40	80	
Fall Time	t _f			20	40	
Turn-On Delay Time	t _{d(on)}			7	15	ns
Rise Time	t _r	$V_{DD} = -10 \text{ V}, R_{L} = 1.67 \Omega$		10	20	
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ - 6 A, $V_{GEN}=$ - 10 V, $R_g=$ 1 Ω		40	80	
Fall Time	t _f			20	40	
Drain-Source Body Diode Characterist	ics					
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 9	Α
Pulse Diode Forward Current	I _{SM}				- 40	A
Body Diode Voltage	V _{SD}	I _S = -6 A, V _{GS} = 0 V		- 0.9	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}			21	35	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$I_F = -6 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s},$		9	20	nC
Reverse Recovery Fall Time	t _a	$T_J = 25 ^{\circ}C$		7		
Reverse Recovery Rise Time	t _b			14		ns

Notes

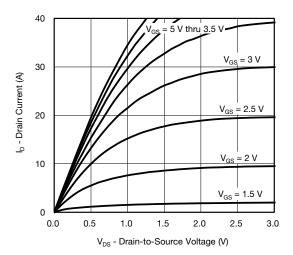
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

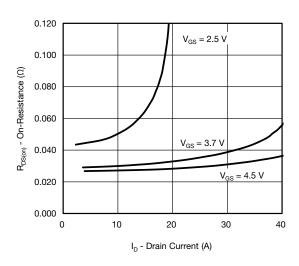




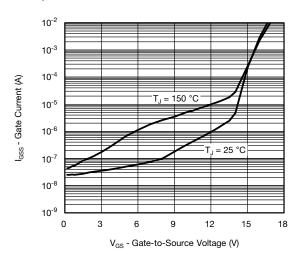
Gate Current vs. Gate-Source Voltage



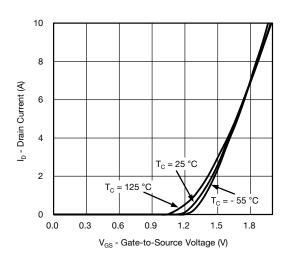
Output Characteristics



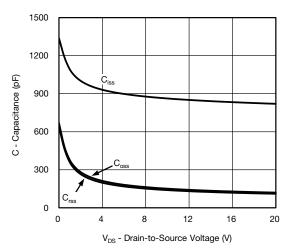
On-Resistance vs. Drain Current and Gate Voltage



Gate Current vs. Gate-to-Source Voltage

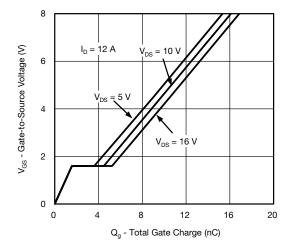


Transfer Characteristics

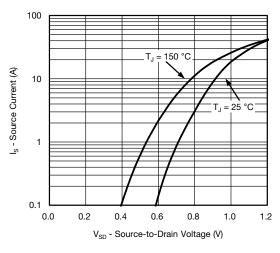


Capacitance

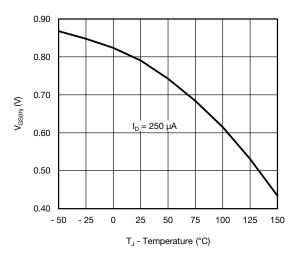




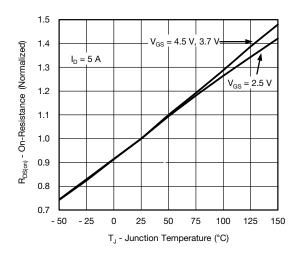
Gate Charge



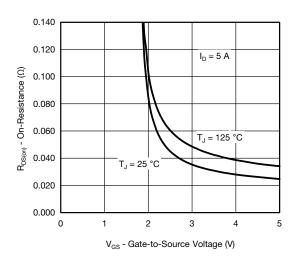
Soure-Drain Diode Forward Voltage



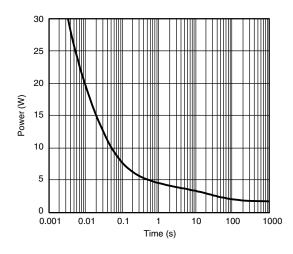
Threshold Voltage



On-Resistance vs. Junction Temperature

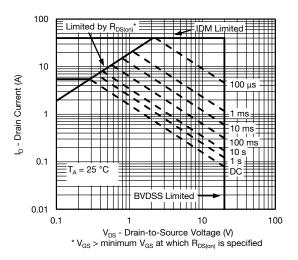


On-Resistance vs. Gate-to-Source Voltage

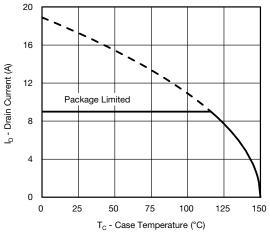


Single Pulse Power, Junction-to-Ambient

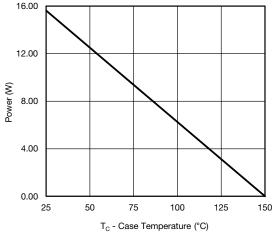




Safe Operating Area, Junction-to-Ambient



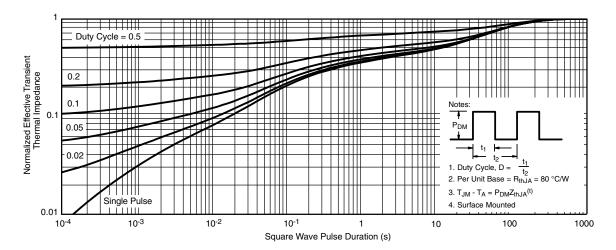




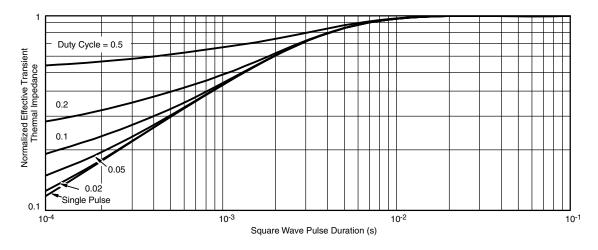
Power Derating

^{*} The power dissipation P_D is based on $T_{J(max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

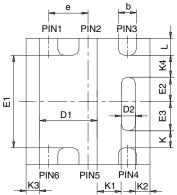
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62912.





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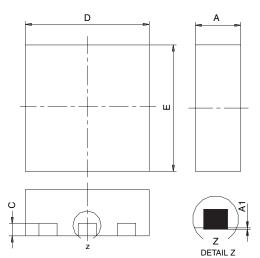
PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
 Package outline exclusive of mold flash and metal burr
 Package outline inclusive of plating

	SINGLE PAD							DUAL PAD				
DIM	MILLIMETERS INCHES MILLIMETE		ILLIMETER	TERS INCHES								
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
е		0.65 BSC			0.026 BSC		0.65 BSC			0.026 BSC		
K		0.275 TYP			0.011 TYP		0.275 TYP		0.011 TYP			
K1		0.400 TYP		0.016 TYP		0.320 TYP			0.013 TYP			
K2		0.240 TYP		0.009 TYP		0.252 TYP		0.010 TYP				
К3		0.225 TYP		0.009 TYP					•	•		
K4		0.355 TYP		0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

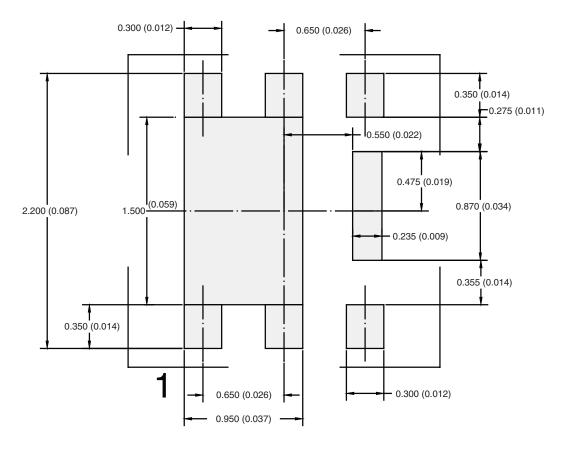
ECN: C-07431 - Rev. C, 06-Aug-07

DWG: 5934

06-Aug-07



RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOT



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Vishay

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