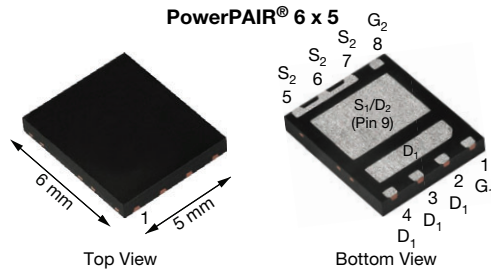


Dual N-Channel 30 V (D-S) MOSFETs



FEATURES

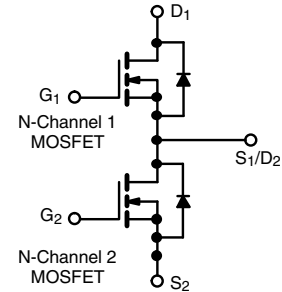
- TrenchFET® power MOSFETs
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Notebook system power
- POL
- Low current DC/DC



PRODUCT SUMMARY		
	CHANNEL-1	CHANNEL-2
V _{DS} (V)	30	30
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.0240	0.0135
R _{DS(on)} max. (Ω) at V _{GS} = 4.5 V	0.0300	0.0170
Q _g typ. (nC)	3.8	7.3
I _D (A) ^a	12	16
Configuration	Dual	

ORDERING INFORMATION

Package	PowerPAIR 6 x 5
Lead (Pb)-free and halogen-free	SiZ904DT-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	CHANNEL-1	CHANNEL-2	UNIT	
Drain-source voltage	V _{DS}	30	30	V	
Gate-source voltage	V _{GS}	± 20	± 20		
Continuous drain current (T _J = 150 °C)	I _D	T _C = 25 °C	12 ^a	16 ^a	A
		T _C = 70 °C	12 ^a	16 ^a	
		T _A = 25 °C	9.5 ^{b, c}	14.5 ^{b, c}	
		T _A = 70 °C	7.6 ^{b, c}	11.6 ^{b, c}	
Pulsed drain current (t = 300 μs)	I _{DM}	30	40	mJ	
Source drain current diode current	I _S	T _C = 25 °C	12 ^a		16 ^a
		T _A = 25 °C	3.2 ^{b, c}		4 ^{b, c}
Single pulse avalanche current	I _{AS}	10	15	mJ	
Single pulse avalanche energy	E _{AS}	5	11		
Maximum power dissipation	P _D	T _C = 25 °C	20	33	W
		T _C = 70 °C	12.9	21	
		T _A = 25 °C	3.8 ^{b, c}	4.8 ^{b, c}	
		T _A = 70 °C	2.4 ^{b, c}	3.1 ^{b, c}	
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150		°C	
Soldering recommendations (peak temperature) ^{d, e}		260			

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	CHANNEL-1		CHANNEL-2		UNIT
		TYP.	MAX.	TYP.	MAX.	
Maximum junction-to-ambient ^{b, f}	R _{thJA}	25	33	20	26	°C/W
Maximum junction-to-case (drain)	R _{thJC}	4.7	6.2	3	3.8	

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- See solder profile (www.vishay.com/doc?273257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 68 °C/W for channel-1 and 61 °C/W for channel-2



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT		
Static								
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-1	30	-	-	V	
		$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-2	30	-	-		
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1	-	35	-	mV/ $^\circ\text{C}$	
		$I_D = 250\text{ }\mu\text{A}$	Ch-2	-	33	-		
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1	-	-4.5	-		
		$I_D = 250\text{ }\mu\text{A}$	Ch-2	-	-5	-		
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	1	-	2.5	V	
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-2	1.2	-	2.5		
Gate-body leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Ch-1	-	-	± 100	nA	
			Ch-2	-	-	± 100		
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-1	-	-	1	μA	
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-2	-	-	1		
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-1	-	-	5		
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-2	-	-	5		
On-state drain current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	20	-	-	A	
		$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-2	20	-	-		
Drain-source on-state resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 7.8\text{ A}$	Ch-1	-	0.0200	0.0240	Ω	
		$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Ch-2	-	0.0105	0.0135		
		$V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$	Ch-1	-	0.0240	0.0300		
		$V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$	Ch-2	-	0.0135	0.0170		
Forward transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 7.8\text{ A}$	Ch-1	-	17	-	S	
		$V_{DS} = 10\text{ V}, I_D = 10\text{ A}$	Ch-2	-	24	-		
Dynamic ^a								
Input capacitance	C_{iss}	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1	-	435	-	pF	
			Ch-2	-	846	-		
Output capacitance	C_{oss}		Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1	-	95		-
				Ch-2	-	187		-
Reverse transfer capacitance	C_{rss}			Ch-1	-	42		-
				Ch-2	-	72		-
Total gate charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 7.8\text{ A}$		Ch-1	-	8	12	nC
				Ch-2	-	15.4	23	
			Ch-1	-	3.8	6		
			Ch-2	-	7.3	11		
Gate-source charge	Q_{gs}	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 7.8\text{ A}$	Ch-1	-	1.4	-		
			Ch-2	-	2.3	-		
Gate-drain charge	Q_{gd}		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch-1	-	1.1	-	
				Ch-2	-	2.2	-	
Gate resistance	R_g	$f = 1\text{ MHz}$		Ch-1	0.6	3.2	6.4	Ω
				Ch-2	0.2	0.8	1.6	



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Dynamic ^a							
Turn-on delay time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}$, $R_L = 2.4\ \Omega$ $I_D \cong 6.3\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\ \Omega$	Ch-1	-	15	30	ns
			Ch-2	-	15	30	
Rise time	t_r		Ch-1	-	12	24	
			Ch-2	-	12	24	
Turn-off delay time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}$, $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\ \Omega$	Ch-1	-	13	26	
			Ch-2	-	13	26	
Fall time	t_f		Ch-1	-	10	20	
			Ch-2	-	10	20	
Turn-on delay time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}$, $R_L = 2.4\ \Omega$ $I_D \cong 6.3\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$	Ch-1	-	5	10	
			Ch-2	-	9	18	
Rise time	t_r		Ch-1	-	10	20	
			Ch-2	-	9	18	
Turn-off delay time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}$, $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$	Ch-1	-	15	30	
			Ch-2	-	14	28	
Fall time	t_f		Ch-1	-	10	20	
			Ch-2	-	8	16	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	$T_C = 25\text{ }^\circ\text{C}$	Ch-1	-	-	12	A
			Ch-2	-	-	16	
Pulse diode forward current ^a	I_{SM}		Ch-1	-	-	30	
			Ch-2	-	-	40	
Body diode voltage	V_{SD}	$I_S = 6.3\text{ A}$, $V_{GS} = 0\text{ V}$	Ch-1	-	0.8	1.2	V
		$I_S = 3\text{ A}$, $V_{GS} = 0\text{ V}$	Ch-2	-	0.78	1.2	
Body diode reverse recovery time	t_{rr}	Channel-1 $I_F = 6.3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	Ch-1	-	15	30	ns
			Ch-2	-	17	34	
Body diode reverse recovery charge	Q_{rr}	Channel-2 $I_F = 10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	Ch-1	-	7	15	nC
			Ch-2	-	9.5	19	
Reverse recovery fall time	t_a		Ch-1	-	9	-	ns
			Ch-2	-	10	-	
Reverse recovery rise time	t_b		Ch-1	-	6	-	
			Ch-2	-	7	-	

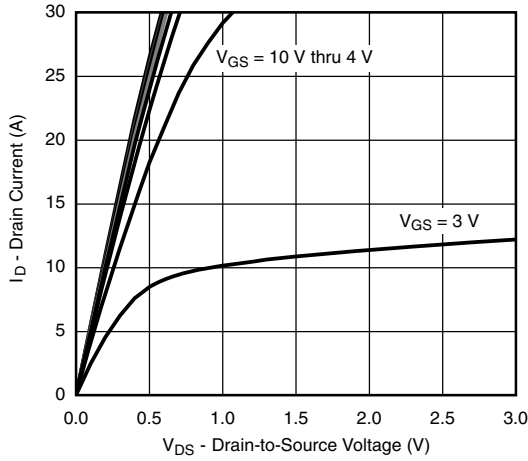
Notes

- a. Guaranteed by design, not subject to production testing
- b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

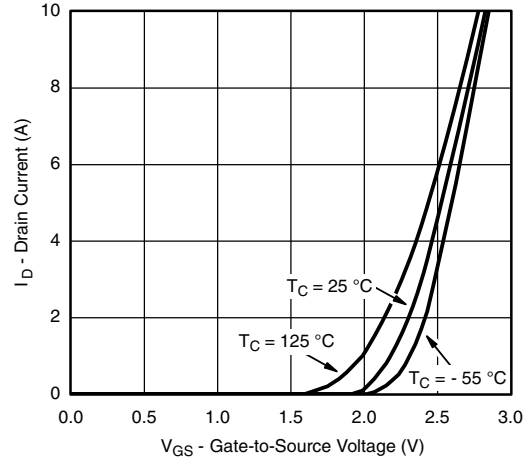
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



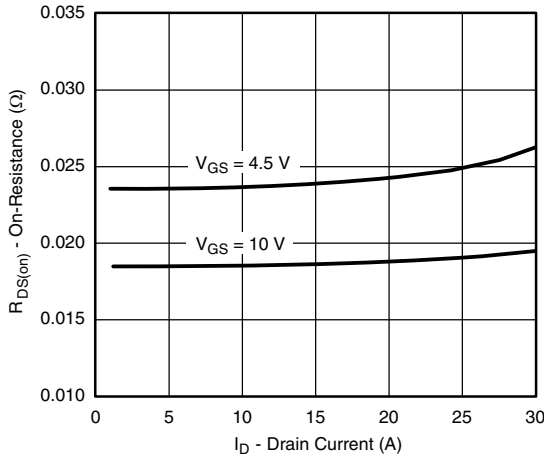
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



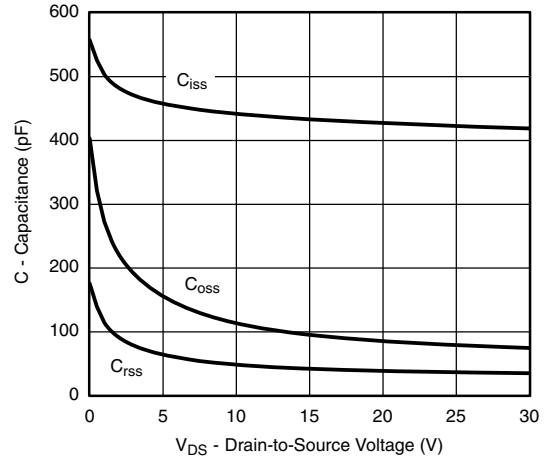
Output Characteristics



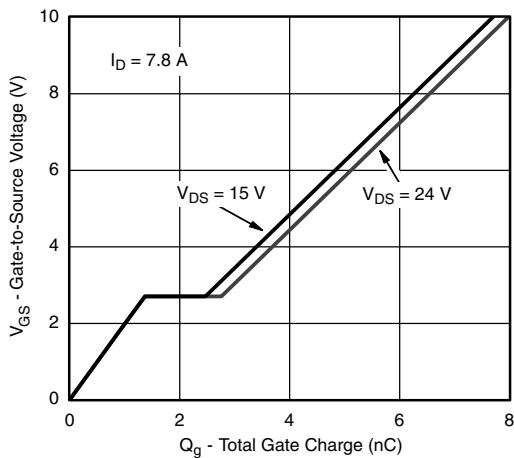
Transfer Characteristics



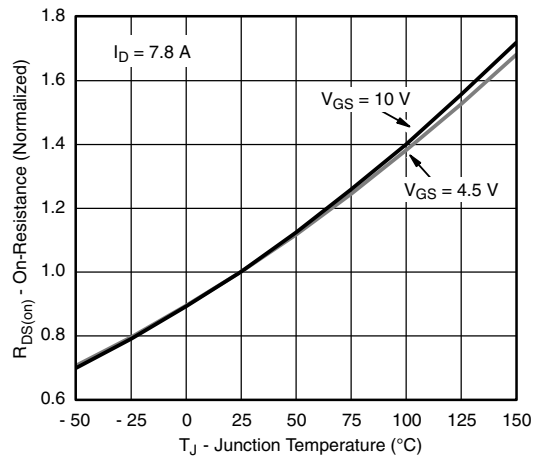
On-Resistance vs. Drain Current



Capacitance



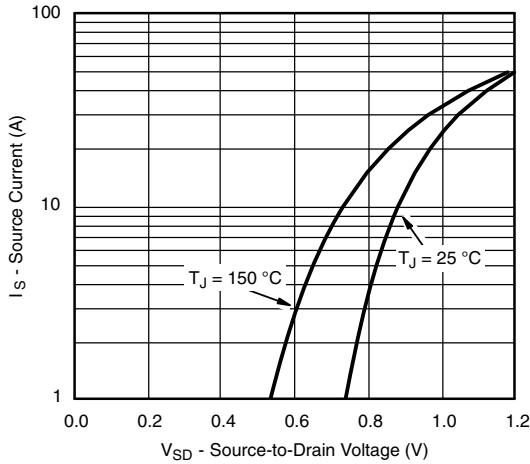
Gate Charge



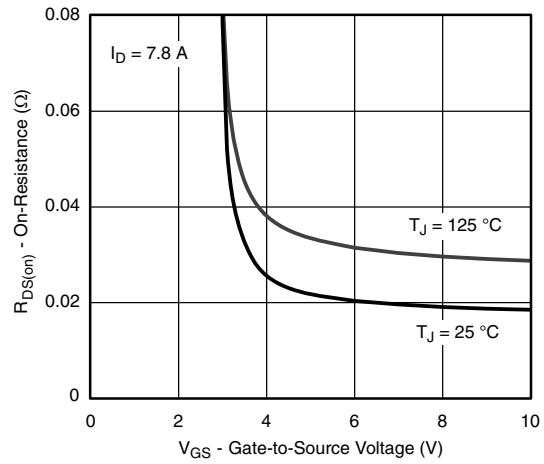
On-Resistance vs. Junction Temperature



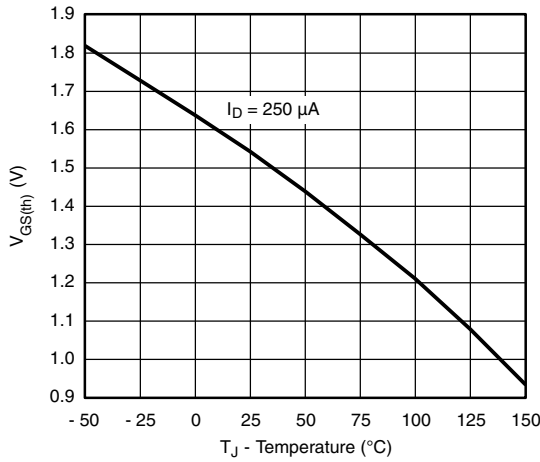
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



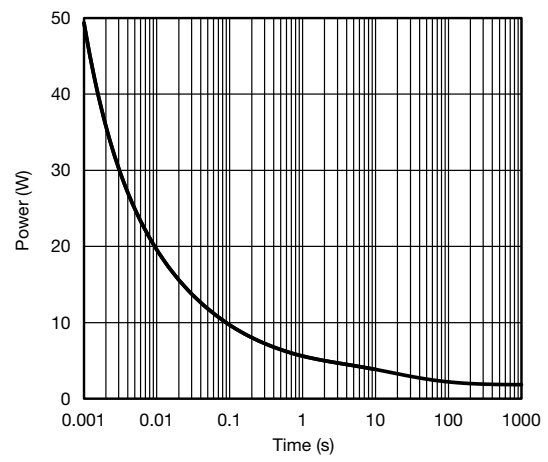
Source-Drain Diode Forward Voltage



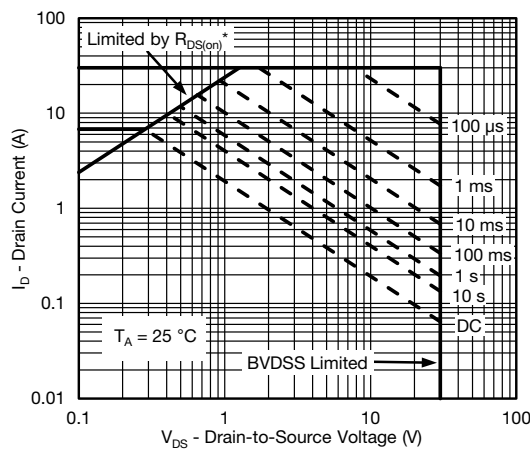
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



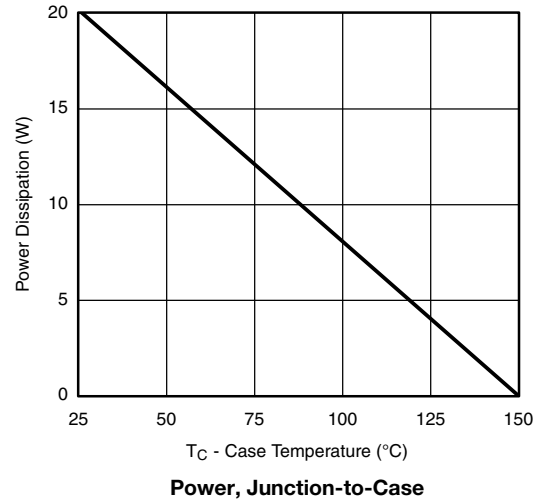
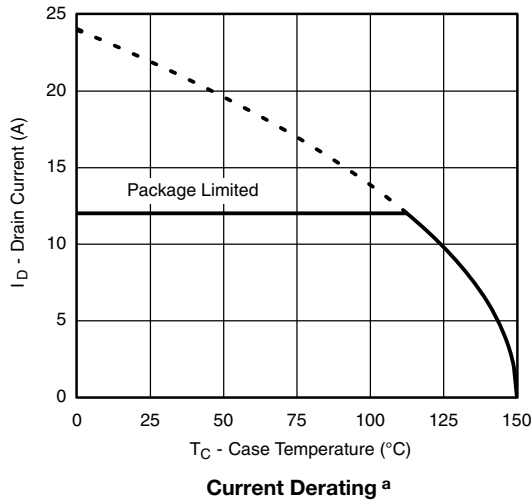
Single Pulse Power



Safe Operating Area, Junction-to-Ambient



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

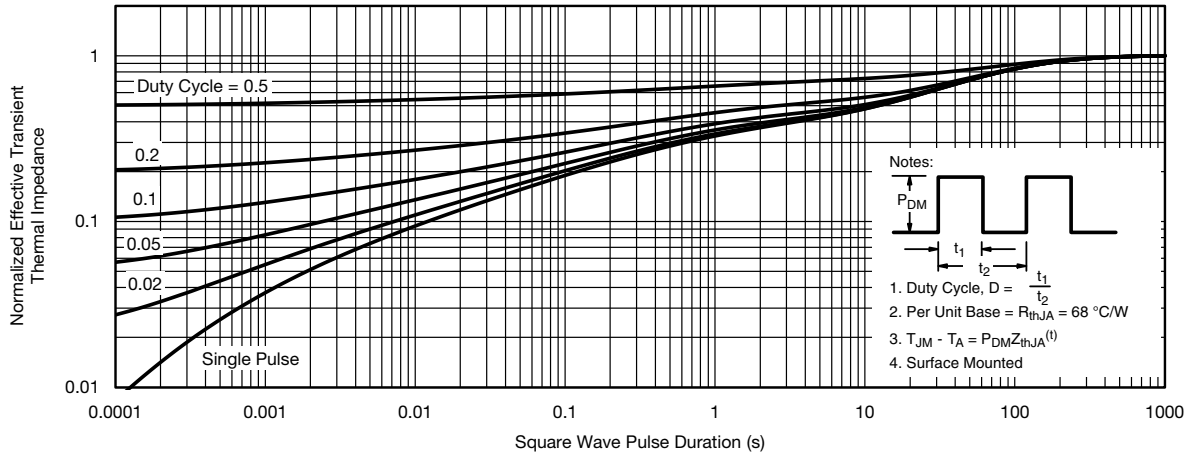


Note

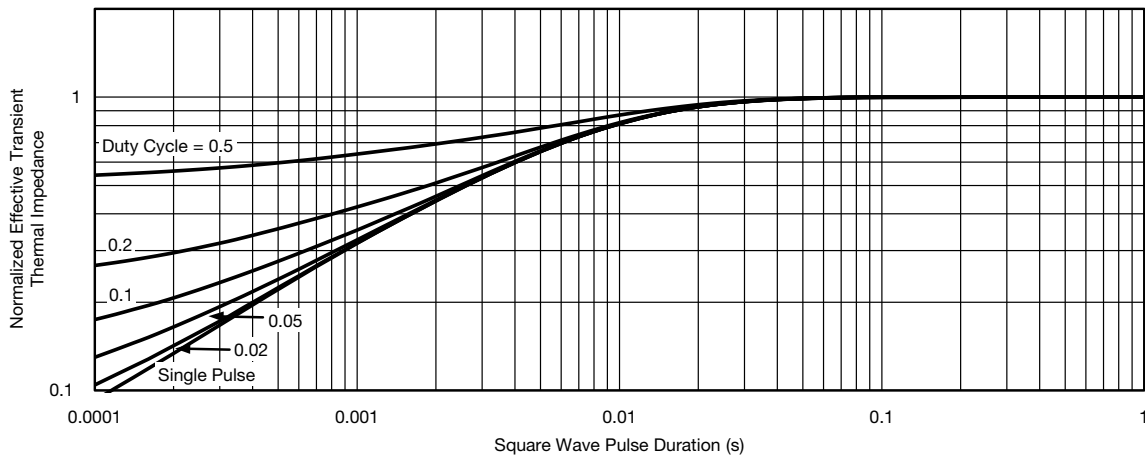
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



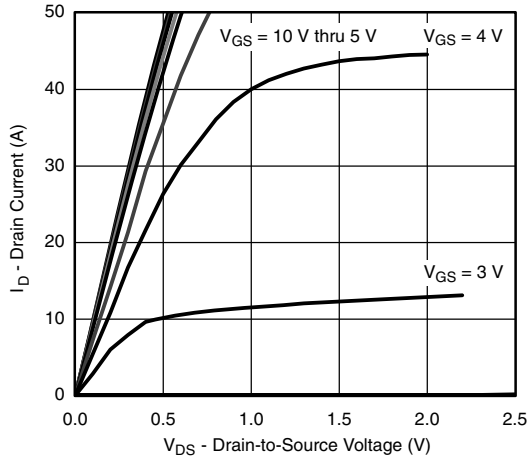
Normalized Thermal Transient Impedance, Junction-to-Ambient



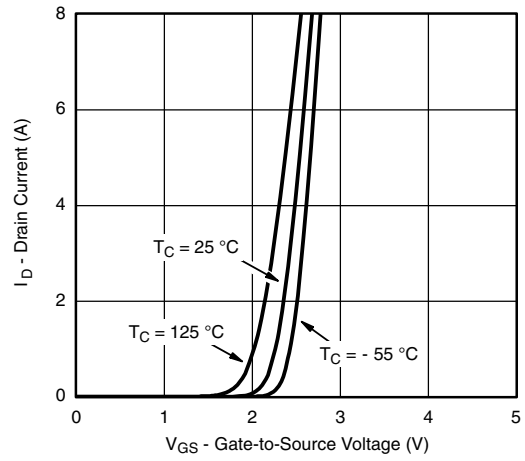
Normalized Thermal Transient Impedance, Junction-to-Case



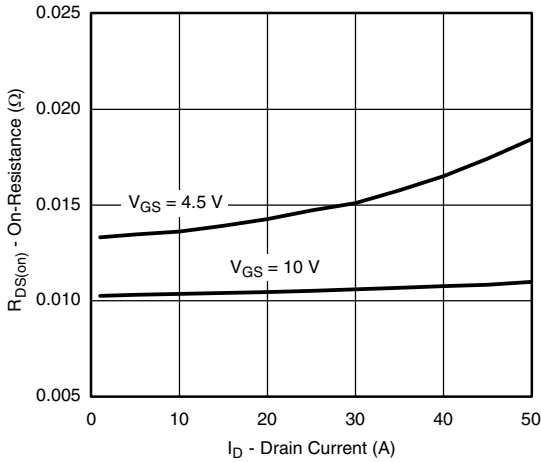
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



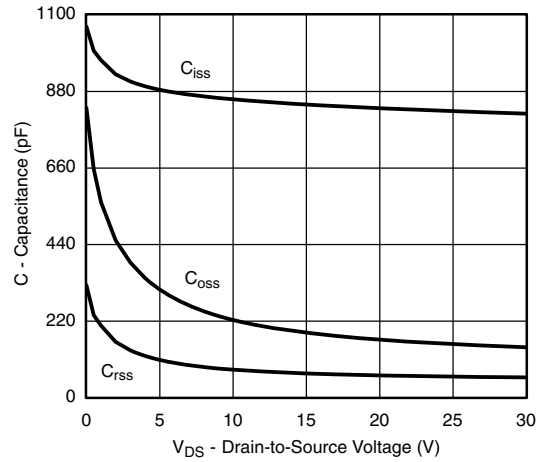
Output Characteristics



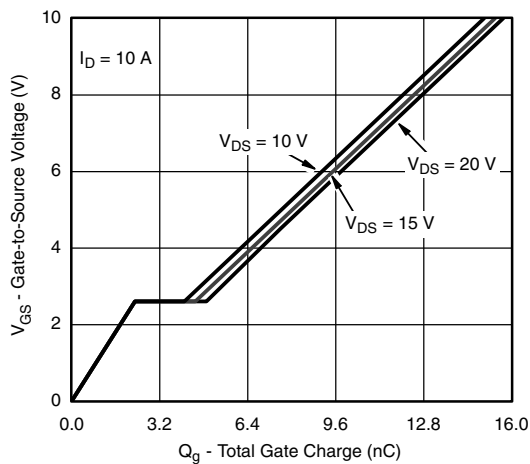
Transfer Characteristics



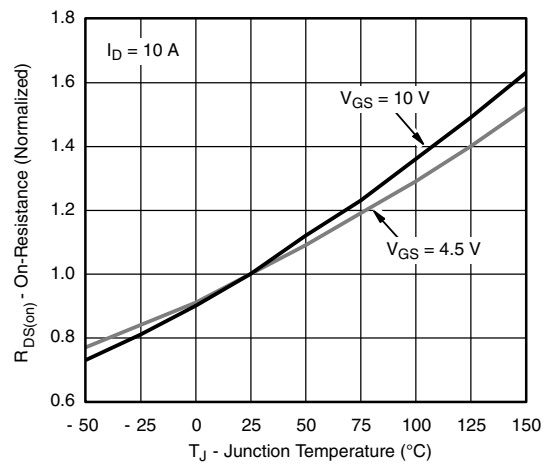
On-Resistance vs. Drain Current



Capacitance



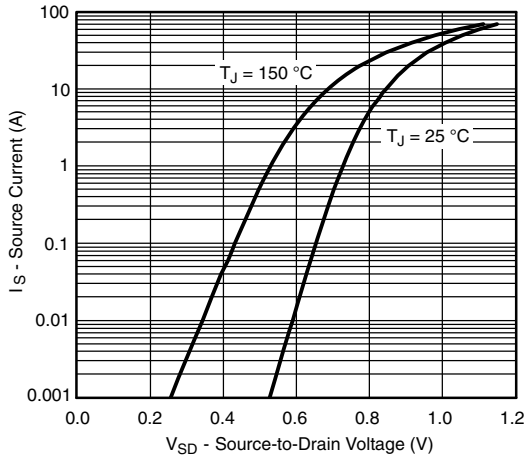
Gate Charge



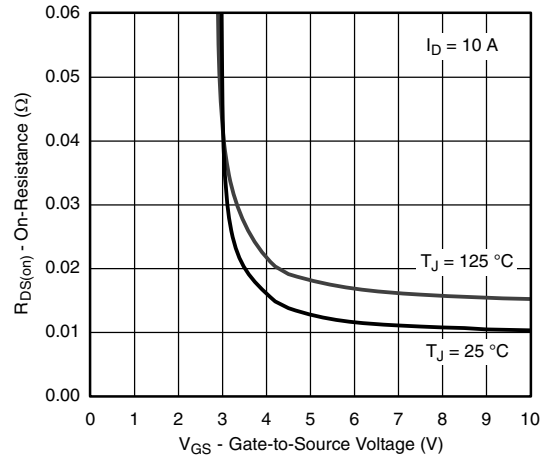
On-Resistance vs. Junction Temperature



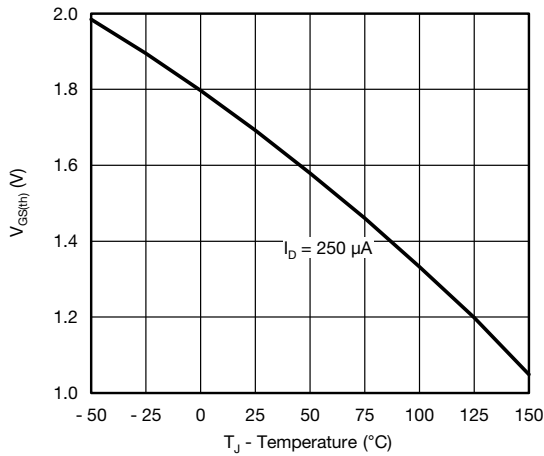
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



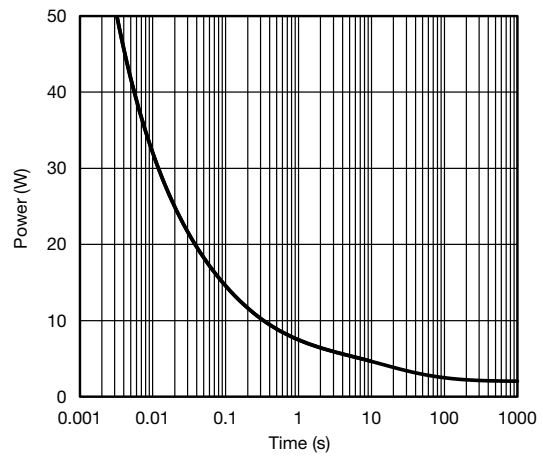
Source-Drain Diode Forward Voltage



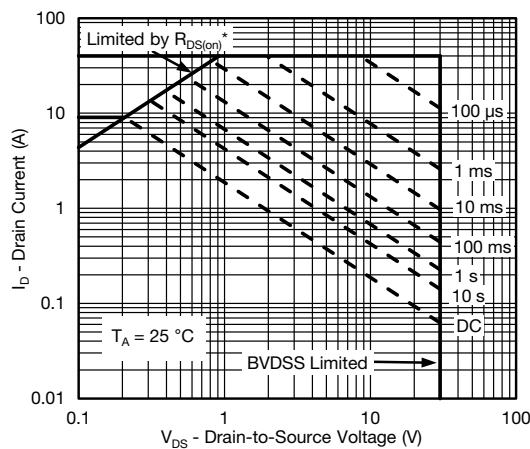
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



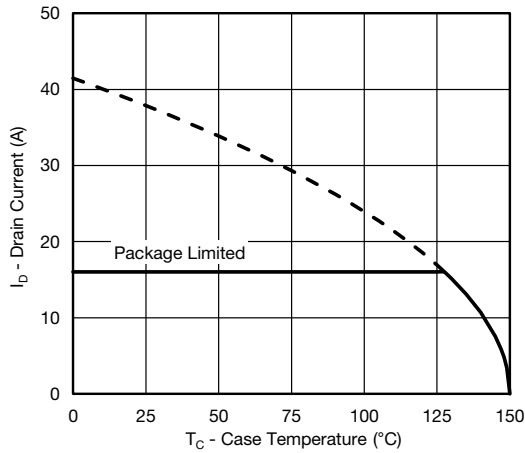
Single Pulse Power



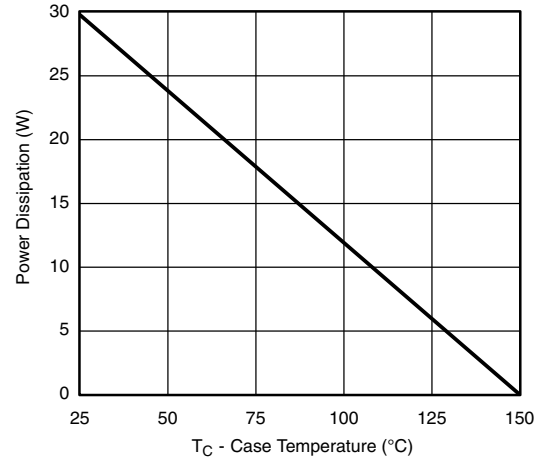
Safe Operating Area, Junction-to-Ambient



CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



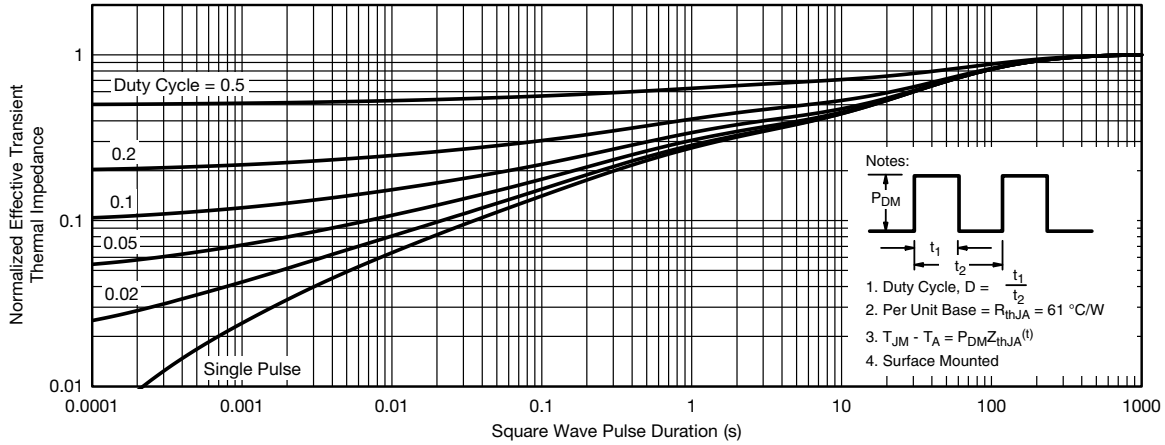
Power, Junction-to-Case

Note

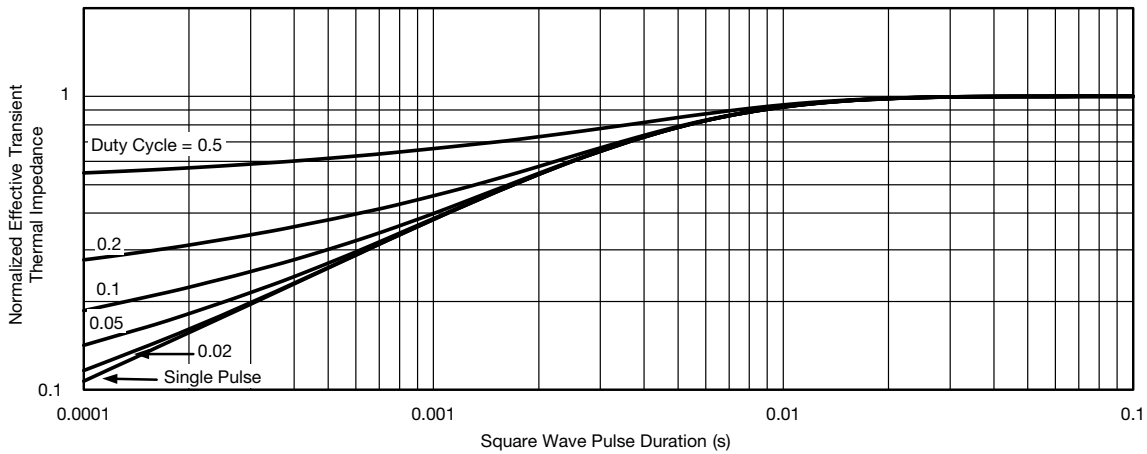
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63482.

PowerPAIR® 6 x 5 Case Outline



Top side view

Back side view

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	-	0.10	0.000	-	0.004
A3	0.15	0.20	0.25	0.006	0.007	0.009
b	0.43	0.51	0.61	0.017	0.020	0.024
b1	0.25 BSC			0.010 BSC		
D	4.90	5.00	5.10	0.192	0.196	0.200
D1	3.75	3.80	3.85	0.148	0.150	0.152
E	5.90	6.00	6.10	0.232	0.236	0.240
E1 Option AA (for W/B)	2.62	2.67	2.72	0.103	0.105	0.107
E1 Option AB (for BWL)	2.42	2.47	2.52	0.095	0.097	0.099
E2	0.87	0.92	0.97	0.034	0.036	0.038
e	1.27 BSC			0.050 BSC		
K Option AA (for W/B)	0.45 typ.			0.018 typ.		
K Option AB (for BWL)	0.65 typ.			0.025 typ.		
K1	0.66 typ.			0.025 typ.		
L	0.33	0.43	0.53	0.013	0.017	0.020
L3	0.23 BSC			0.009 BSC		
z	0.34 BSC			0.013 BSC		
ECN: T14-0782-Rev. C, 22-Dec-14						
DWG: 6005						



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