# 5-V PECL/ECL 1:2 Fanout Buffer

## FEATURES

- 1:2 PECL/ECL Fanout Buffer
- Operating Range
  - PECL: $V_{CC}$ = 4.2 V to 5.7 V With $V_{EE}$ = 0 V
  - NECL: $V_{CC}$ = 0 V With $V_{EE}$ = –4.2 V to –5.7 V
- 5-ps Skew Between Outputs
- Support for Clock Frequencies >2.5 GHz
- 265-ps Typical Propagation Delay
- Deterministic Output Value for Open Input Conditions
- Drop-In Compatible With MC10EL11, MC100EL11
- Built-In Input Pulldown Resistors
- Built-In Temperature Compensation

## APPLICATIONS

- Data and Clock Transmission Over Backplane
- Signaling Level Conversion

## DESCRIPTION

The SN65EL11 is a differential 1:2 PECL/ECL fanout buffer. The device includes circuitry to maintain a known logic level when inputs are in an open condition. The SN65EL11 is housed in an industry-standard SOIC-8 package and is also available in a TSSOP-8 package.

## PINOUT ASSIGNMENT

D-8, DGK-8 Package
(Top View)

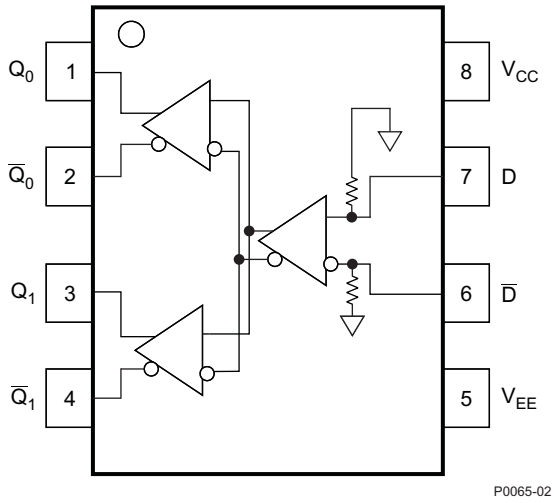


**Table 1. Pin Description**

| PIN | FUNCTION |
|---|---|
| D, $\overline{D}$ | PECL/ECL data inputs |
| $Q_0$, $\overline{Q}_0$, $Q_1$, $\overline{Q}_1$ | PECL/ECL outputs |
| Vcc | Positive supply |
| $V_{EE}$ | Negative supply |

## ORDERING INFORMATION(1)

| PART NUMBER | PART MARKING | PACKAGE | LEAD FINISH |
|---|---|---|---|
| SN65EL11D | SN65EL11 | SOIC | NiPdAu |
| SN65EL11DGK | SN65EL11 | SOIC-TSSOP | NiPdAu |

(1) Leaded device options not initially available; contact a sales representative for further details.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS(1)

| PARAMETER | CONDITIONS | VALUE | UNIT |
|---|---|---|---|
| Absolute PECL-mode supply voltage, $V_{CC}$ | $V_{EE}$ = 0 V | 6 | V |
| Absolute NECL-mode supply voltage, $V_{EE}$ | $V_{CC}$ = 0 V | –6 | V |
| PECL-mode input voltage | $V_{EE}$ = 0 V; $V_I \le V_{CC}$ | 6 | V |
| NECL-mode input voltage | $V_{CC}$ = 0 V; $V_I \ge V_{EE}$ | –6 | V |
| Output current | Continuous | 50 | mA |
| | Surge | 100 | mA |
| Operating temperature range | | –40 to 85 | °C |
| Storage temperature range | | –65 to 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## POWER DISSIPATION RATINGS

| PACKAGE | CIRCUIT BOARD MODEL | POWER RATING $T_A$ < 25°C (mW) | THERMAL RESISTANCE, JUNCTION-TO-AMBIENT, NO AIRFLOW | DERATING FACTOR $T_A$ > 25°C (mW/°C) | POWER RATING $T_A$ = 85°C (mW) |
|---|---|---|---|---|---|
| SOIC | Low-K | 719 | 139 | 7 | 288 |
| | High-K | 840 | 119 | 8 | 336 |
| SOIC-TSSOP | Low-K | 469 | 213 | 5 | 188 |
| | High-K | 527 | 189 | 5 | 211 |

## THERMAL CHARACTERISTICS

| PARAMETER | | PACKAGE | VALUE | UNIT |
|---|---|---|---|---|
| $\theta_{JB}$ | Junction-to-board thermal resistance | SOIC | 79 | °C/W |
| | | SOIC-TSSOP | 120 | |
| $\theta_{JC}$ | Junction-to-case thermal resistance | SOIC | 98 | °C/W |
| | | SOIC-TSSOP | 74 | |

## KEY ATTRIBUTES

| CHARACTERISTICS | VALUE |
|---|---|
| Internal input pulldown resistor | 75 kΩ |
| Moisture sensitivity level | Level 1 |
| Flammability rating (oxygen index: 28 to 34) | UL 94 V-0 at 0.125 in |
| ESD-HBM | 4 kV |
| ESD-machine model | 200 V |
| Meets or exceeds JEDEC Spec EIA/JESD78 latchup test | |

## PECL DC CHARACTERISTICS[1] ($V_{CC}$ = 5 V; $V_{EE}$ = 0 V)[2]

| PARAMETER | | –40°C | | | 25°C | | | 85°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $I_{CC}$ | Power-supply current | | 18 | 26 | | 21 | 26 | | 23 | 26 | mA |
| $V_{OH}$ | Output HIGH voltage[3] | 3915 | | 4120 | 3915 | 4000 | 4120 | 3915 | | 4120 | mV |
| $V_{OL}$ | Output LOW voltage[3] | 3170 | | 3380 | 3170 | 3288 | 3380 | 3170 | | 3380 | mV |
| $V_{IH}$ | Input HIGH voltage (single-ended) | 3835 | | 4120 | 3835 | | 4120 | 3835 | | 4120 | mV |
| $V_{IL}$ | Input LOW voltage (single-ended) | 3190 | | 3525 | 3190 | | 3525 | 3190 | | 3525 | mV |
| $V_{IHCMR}$ | Input HIGH voltage, common-mode range (differential)[4] | 2.5 | | 4.6 | 2.5 | | 4.6 | 2.5 | | 4.6 | V |
| $I_{IH}$ | Input HIGH current | | | 150 | | | 150 | | | 150 | µA |
| $I_{IL}$ | Input LOW current | 0.5 | | | 0.5 | | | 0.5 | | | µA |

(1) The device meets these specifications after thermal equilibrium has been established when mounted in a test socket or printed-circuit board with maintained transverse airflow greater than 500 lfpm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.25 V / –0.5 V.
(3) Outputs are terminated through a 50-Ω resistor to $V_{CC}$ – 2 V.
(4) $V_{IHCMR}$ min varies 1:1 with $V_{EE}$; $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the more-positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP}$ min and 1 V.

## NECL DC CHARACTERISTICS[1] ($V_{CC}$ = 0 V; $V_{EE}$ = 5 V)[2]

| PARAMETER | | –40°C | | | 25°C | | | 85°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $I_{EE}$ | Power-supply current | | 19 | 26 | | 21 | 26 | | 23 | 26 | mA |
| $V_{OH}$ | Output HIGH voltage[3] | –1085 | | –880 | –1025 | –995 | –880 | –1025 | | –880 | mV |
| $V_{OL}$ | Output LOW voltage[3] | –1830 | | –1620 | –1810 | –1712 | –1620 | –1810 | | –1620 | mV |
| $V_{IH}$ | Input HIGH voltage (single-ended) | –1165 | | –880 | –1165 | | –880 | –1165 | | –880 | mV |
| $V_{IL}$ | Input LOW voltage (single-ended) | –1810 | | –1475 | –1810 | | –1475 | –1810 | | –1475 | mV |
| $V_{IHCMR}$ | Input HIGH voltage, common-mode range (differential)[4] | –2.5 | | –0.4 | –2.5 | | –0.4 | –2.5 | | –0.4 | V |
| $I_{IH}$ | Input HIGH current | | | 150 | | | 150 | | | 150 | µA |
| $I_{IL}$ | Input LOW current | 0.5 | | | 0.5 | | | 0.5 | | | µA |

(1) The device meets these specifications after thermal equilibrium has been established when mounted in a test socket or printed-circuit board with maintained transverse airflow greater than 500 lfpm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.25 V / –0.5 V.
(3) Outputs are terminated through a 50-Ω resistor to $V_{CC}$ – 2 V.
(4) $V_{IHCMR}$ min varies 1:1 with $V_{EE}$; $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the more-positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP}$ min and 1 V.

## AC CHARACTERISTICS[1] ($V_{CC}$ = 5 V; $V_{EE}$ = 0 V or $V_{CC}$ = 0 V; $V_{EE}$ = –5 V)[2]

| PARAMETER | | –40°C | | | 25°C | | | 85°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $f_{MAX}$ | Maximum switching frequency[3] (see Figure 6) | | 3.5 | | | 3.4 | | | 3.1 | | GHz |
| $t_{PLH}/t_{PHL}$ | Propagation delay to output (see Figure 2) | 200 | | 300 | 200 | | 300 | 200 | | 300 | ps |
| $t_{SKEW}$ | Device skew[4] (see Figure 5) | | 7 | 15 | | 7 | 15 | | 7 | 15 | ps |
| | Duty cycle skew[5] | | 5 | 15 | | 5 | 15 | | 5 | 15 | |
| $t_{JITTER}$ | Random clock jitter (RMS) | | 0.2 | | | 0.2 | | | 0.2 | | ps |
| $V_{PP}$ | Input swing[6] (see Figure 3) | 150 | | 1000 | 150 | | 1000 | 150 | | 1000 | mV |
| $t_r/t_f$ | Q-output rise/fall times (20%–80%) (see Figure 4) | 150 | | 250 | 150 | | 250 | 150 | | 250 | ps |

(1) The device meets these specifications after thermal equilibrium has been established when mounted in a test socket or printed-circuit board with maintained transverse airflow greater than 500 lfpm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.25 V / –0.5 V.
(3) Maximum switching frequency is measured at an output amplitude of 300 mVpp.
(4) Within-device skew defined as identical transitions on similar paths through a device.
(5) Duty cycle skew is the difference between a $t_{PLH}$ and $t_{PHL}$ propagation delay through a device.
(6) $V_{PP(min)}$ is the minimum input swing for which ac parameters are assured.

## Typical Termination for Output Driver

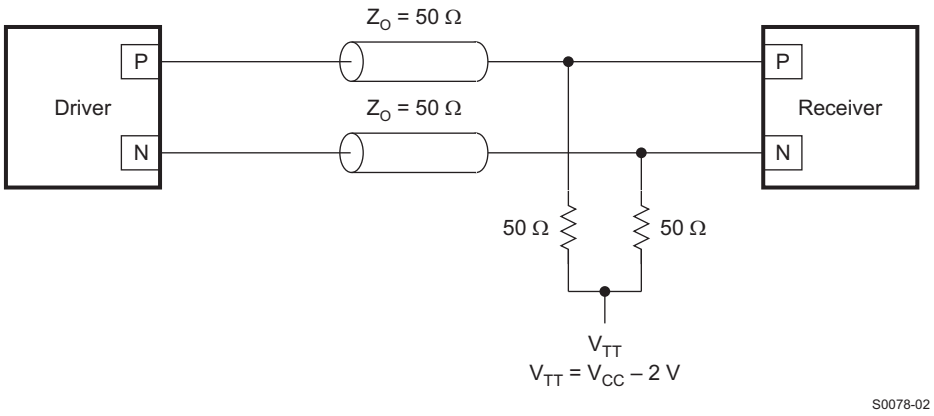


**Figure 1. Typical Termination for Output Driver**

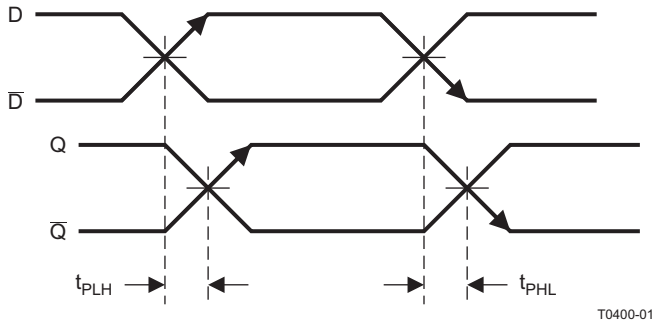


**Figure 2. Propagation Delay**

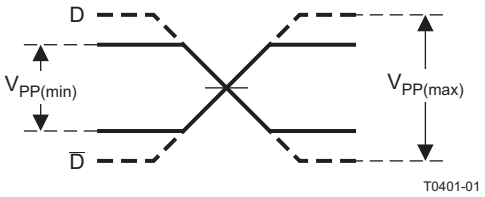


**Figure 3. Input Voltage Swing**

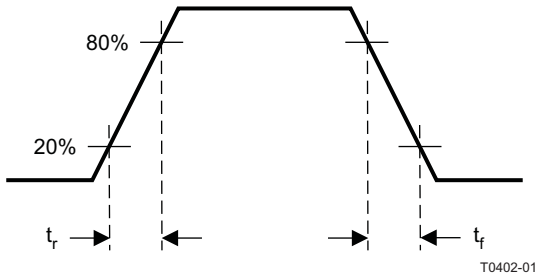


**Figure 4. Output Rise and Fall Times**

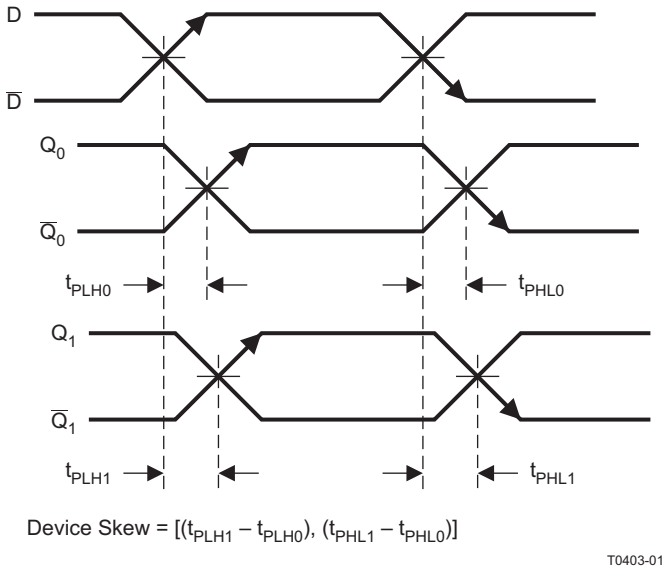


**Figure 5. Device Skew**

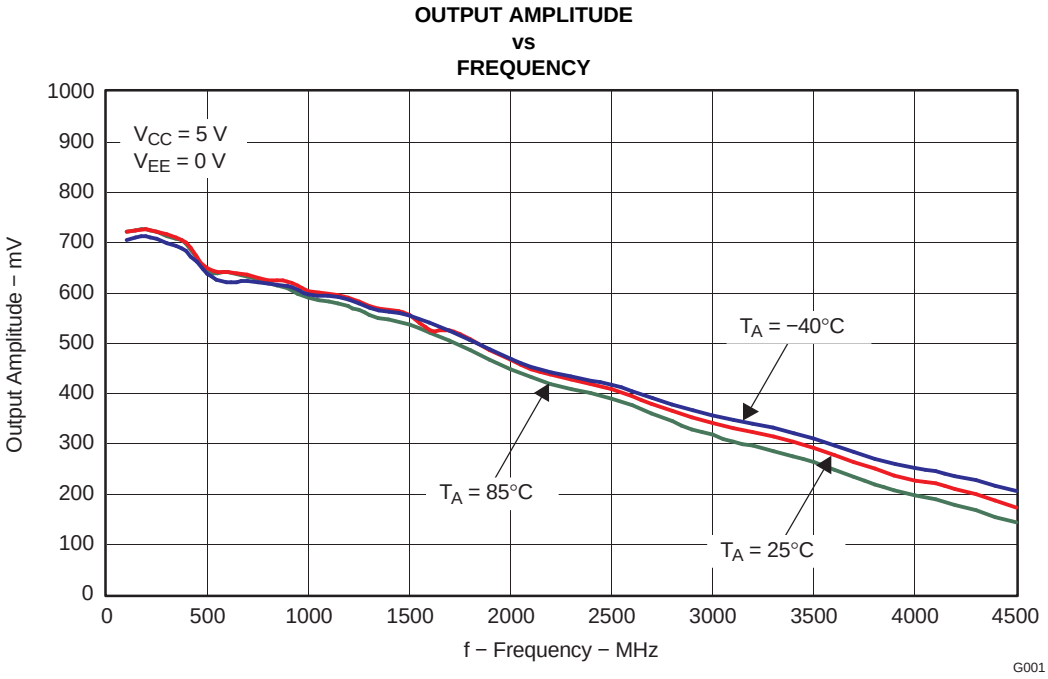


**Figure 6.**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65EL11D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | EL11 | Samples |
| SN65EL11DGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SILI | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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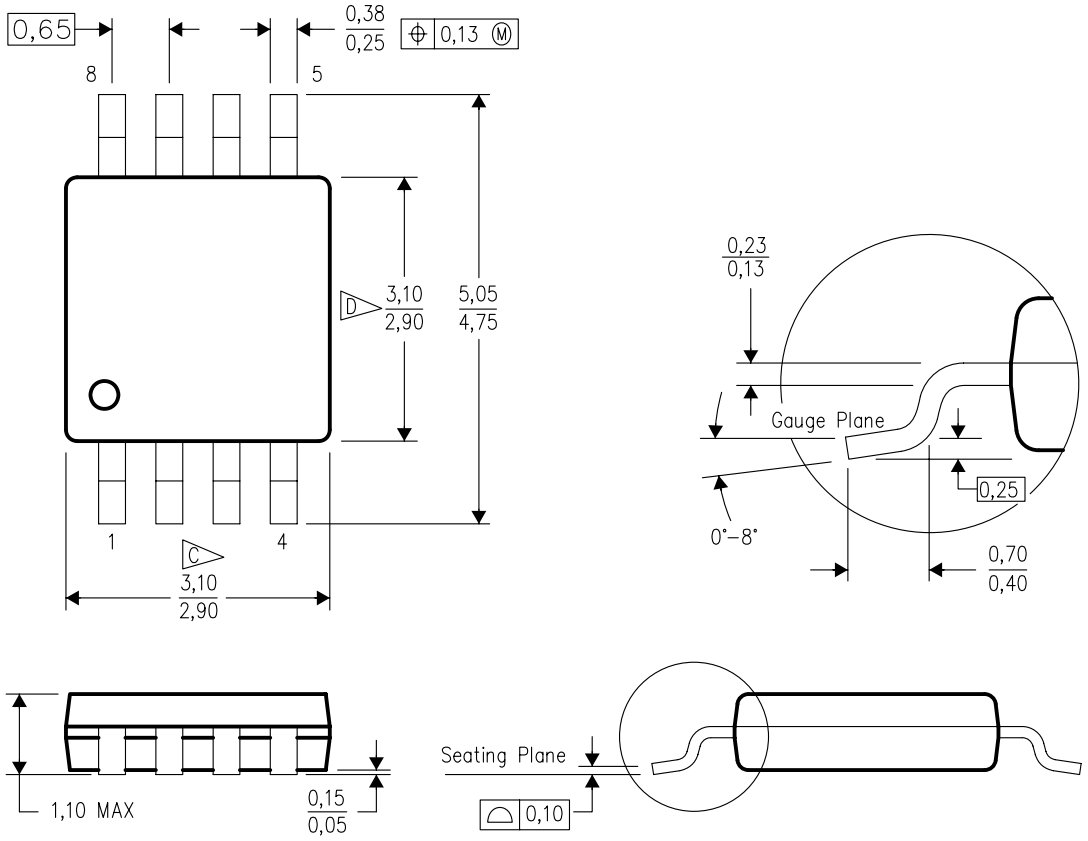
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE

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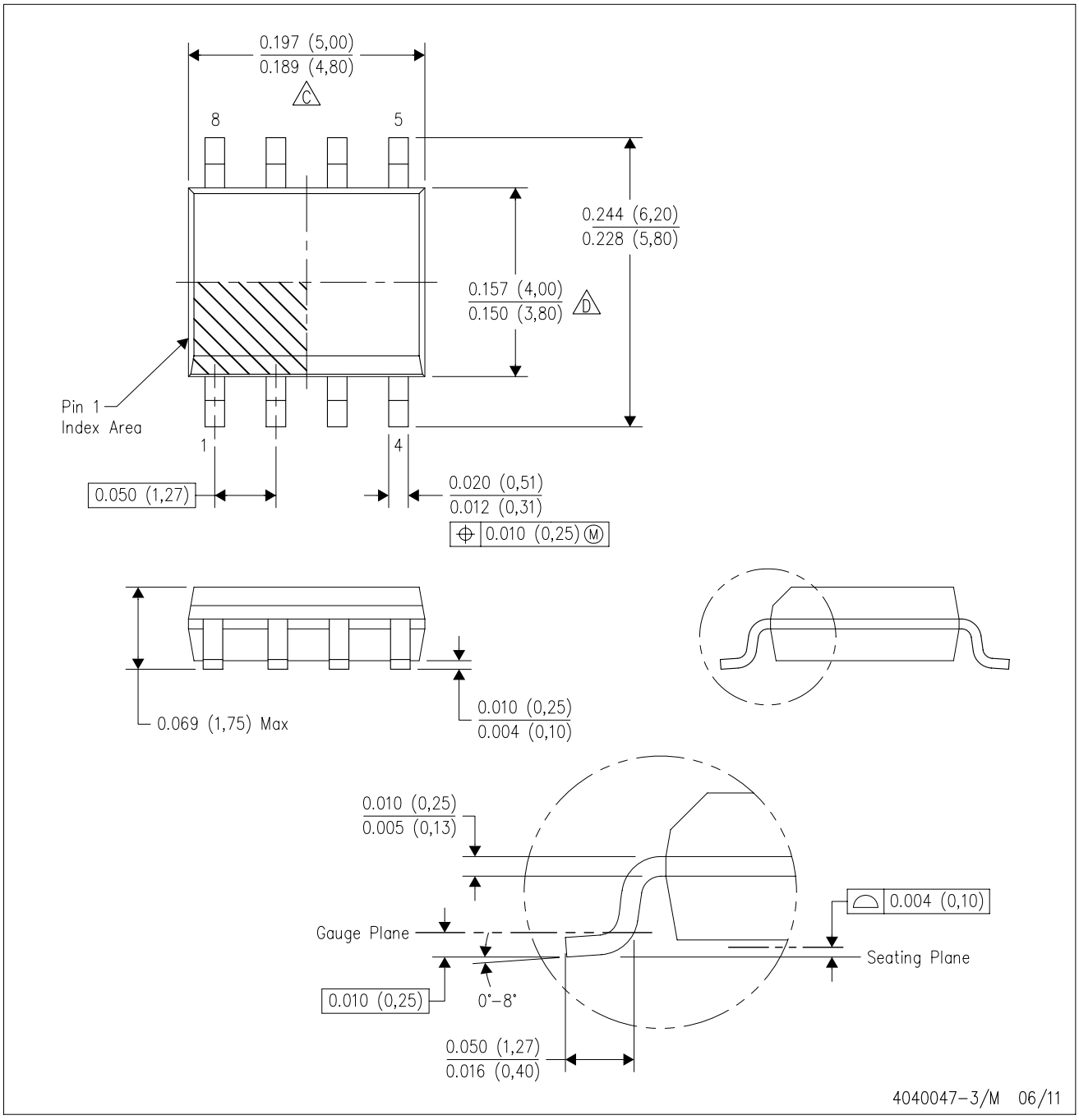
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
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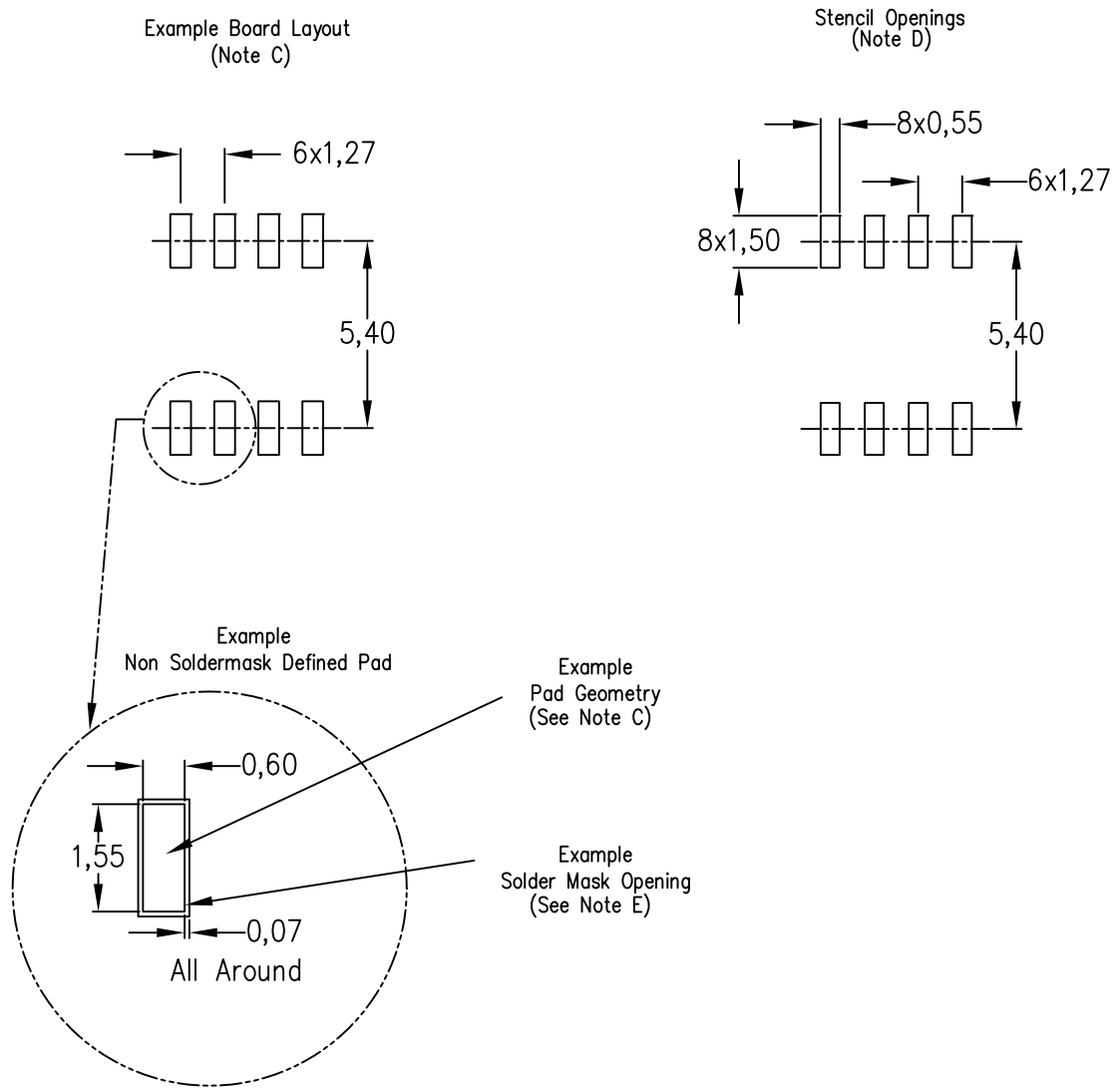
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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