SN74AHC1G04 Single Inverter Gate

1 Features

- Operating Range 2 V to 5.5 V
- Max t_{pd} of 6.5 ns at 5 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±8-mA Output Drive at 5 V
- Schmitt-Trigger Action at All Inputs Makes the Circuit Tolerant for Slower Input Rise and Fall Time
- Latch-Up Performance Exceeds 250 mA Per JESD 17

2 Applications

- Cameras
- E-Meters
- Ethernet Switches
- Infotainment

3 Description

The SN74AHC1G04 contains one inverter gate. The device performs the Boolean function $Y = \overline{A}$.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AHC1G04	SOT-23 (5)	2.90 x 1.60 mm
	SC-70 (5)	2.00 x 1.30 mm
	SOT-553 (5)	1.65 x 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

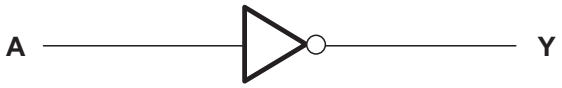


Table of Contents

4 Revision History

Changes from Revision S (December 2014) to Revision T — **Page**

- Removed "Schmitt-Trigger" from the data sheet title ... 1
- Added T_J Junction temperature to the *Absolute Maximum Ratings* ... 4

Changes from Revision R (January 2013) to Revision S — **Page**

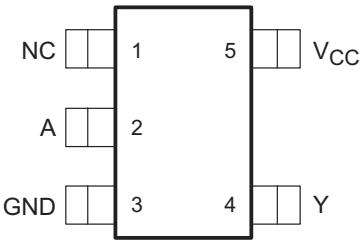
- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table. ... 1
- Changed MAX operating temperature to 125°C in *Recommended Operating Conditions* table. ... 4

Changes from Revision Q (June 2005) to Revision R — **Page**

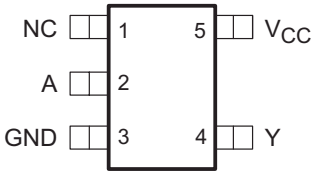
- Changed document format from Quicksilver to DocZone. ... 1

5 Pin Configuration and Functions

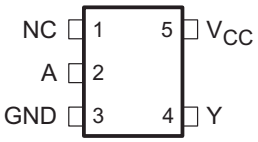
DBV PACKAGE
(TOP VIEW)



DCK PACKAGE
(TOP VIEW)



DRL PACKAGE
(TOP VIEW)



NC – No internal connection

See mechanical drawings for dimensions.

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	NC	—	No Connection
2	A	I	Input A
3	GND	—	Ground Pin
4	Y	O	Output Y
5	V_{CC}	—	Power Pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through each V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		–65	150	°C
T_J	Junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	3500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_{IH}	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC[1]		SN74AHC1G04			UNIT
		DBV	DCK	DRL	
		5 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	231.3	287.6	328.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	119.9	97.7	105.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	60.6	65.0	150.3	
ψ_{JT}	Junction-to-top characterization parameter	17.8	2.0	6.9	
ψ_{JB}	Junction-to-board characterization parameter	60.1	64.2	148.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 µA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OH} = 50 µA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.44		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.44		0.44	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			1		10		10	µA
C_i	V_I = V_{CC} or GND	5 V		2	10		10		10	pF

6.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		5	7.1	1	8.5	1	9.5	ns
t_{PHL}					5	7.1	1	8.5	1	9.5	
t_{PLH}	A	Y	C_L = 50 pF		7.5	10.6	1	12	1	13	ns
t_{PHL}					7.5	10.6	1	12	1	13	

6.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		3.8	5.5	1	6.5	1	7	ns
t_{PHL}					3.8	5.5	1	6.5	1	7	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	6.5	1	7	ns
t_{PHL}					5.3	7.5	1	6.5	1	7	

6.8 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

6.9 Typical Characteristics

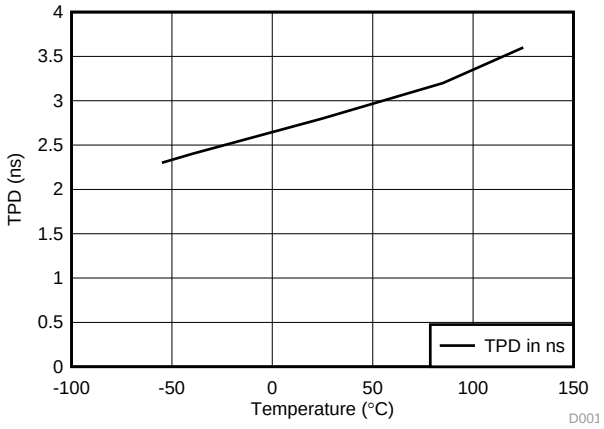


Figure 1. TPD vs Temperature at 5 V

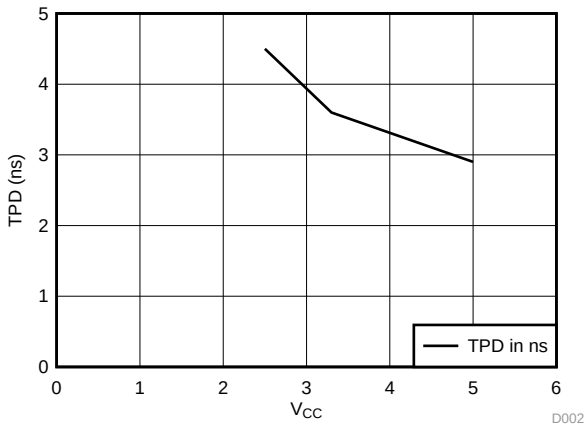
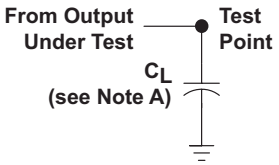
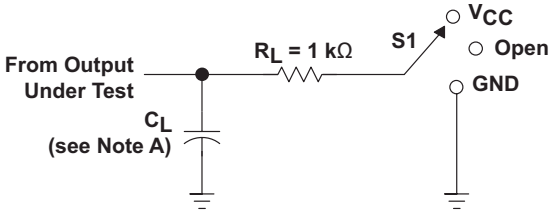


Figure 2. TPD vs V_{CC} at 25°C

7 Parameter Measurement Information

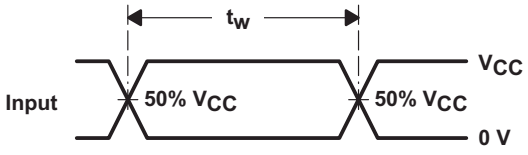


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

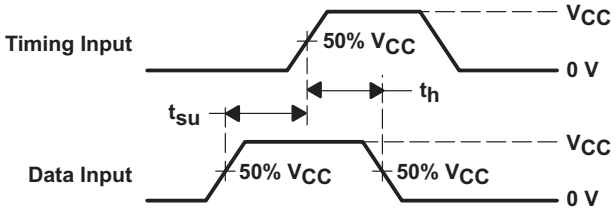


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

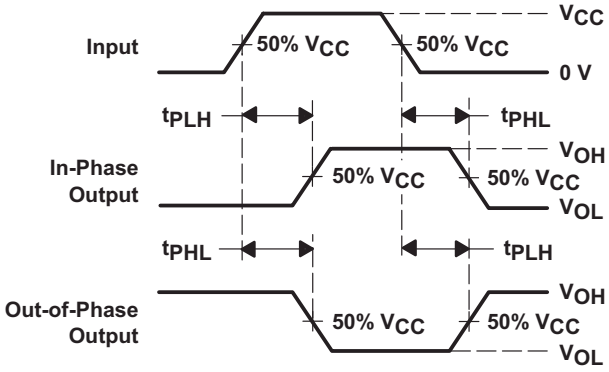
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



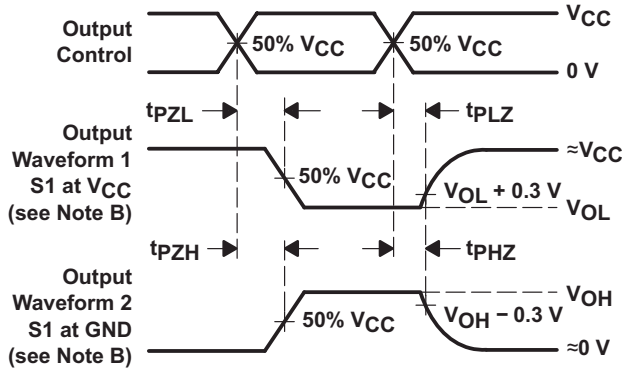
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit And Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74AHC1G04 device contains one inverter gate. The device performs the Boolean function $Y = \overline{A}$.

This single gate inverter has Schmitt-Trigger action on its input, allowing for slower rise and fall times and some noise rejection. This is not a true Schmitt-Trigger, so there is a limit on rise and fall times.

8.2 Functional Block Diagram

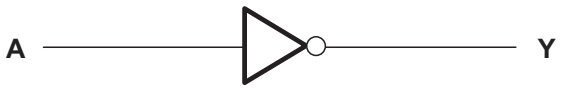


Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

- Wide operating voltage range
  - Operates from 2 V to 5.5 V
- Allows down-voltage translation
  - Inputs accept voltages to 5.5 V
- Lower drive
  - This will produce slower edges and help prevent ringing on outputs

8.4 Device Functional Modes

Table 1. Function Table

INPUT A	OUTPUT Y
H	L
L	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

SN74AHC1G04 is a low-drive CMOS device that can be used for a multitude of inverting buffer type functions. It can produce 8 mA of drive current at 5 V, making it Ideal for driving multiple outputs and good for low-noise applications. The inputs are 5.5-V tolerant, allowing it to translate down to V_{CC}.

9.2 Typical Application

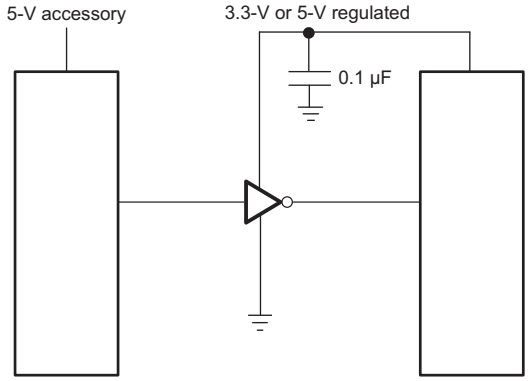


Figure 5. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in the *Recommended Operating Conditions* table.
   - For specified High and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend Output Conditions
   - Load currents should not exceed 25 mA per output and 50 mA total for the part.
   - Outputs should not be pulled above V_{CC}.

Typical Application (continued)

9.2.3 Application Curves

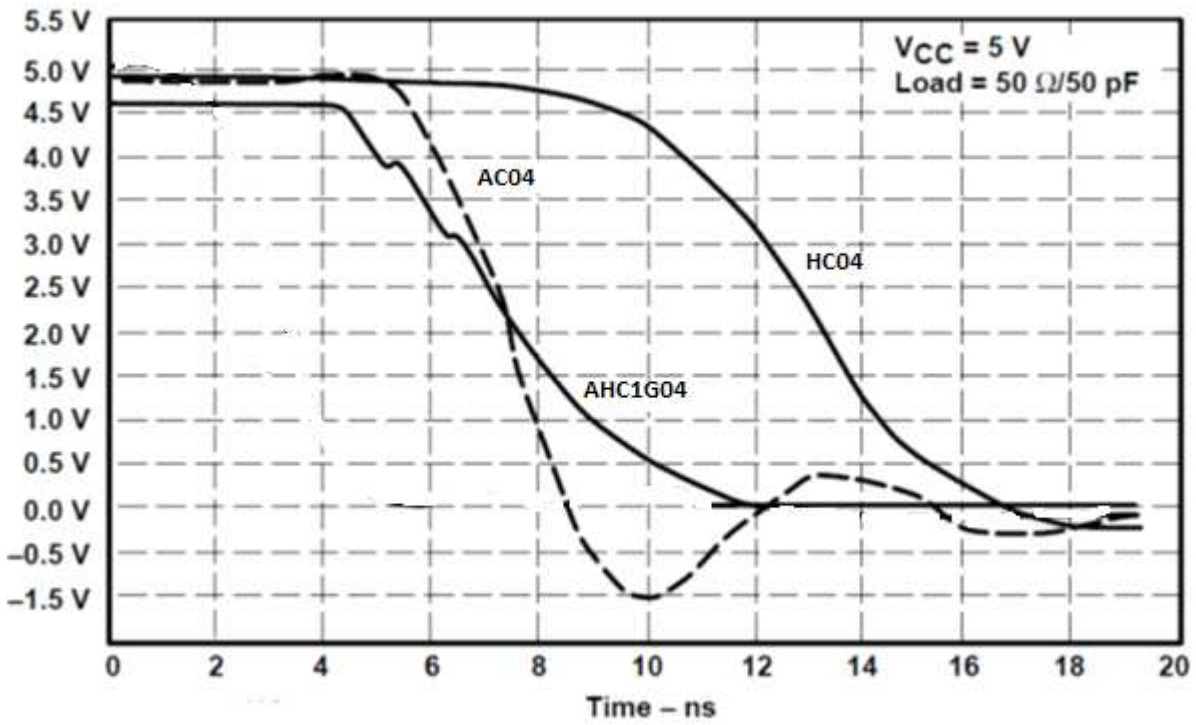


Figure 6. Typical Application Curve

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 7 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

11.2 Layout Example

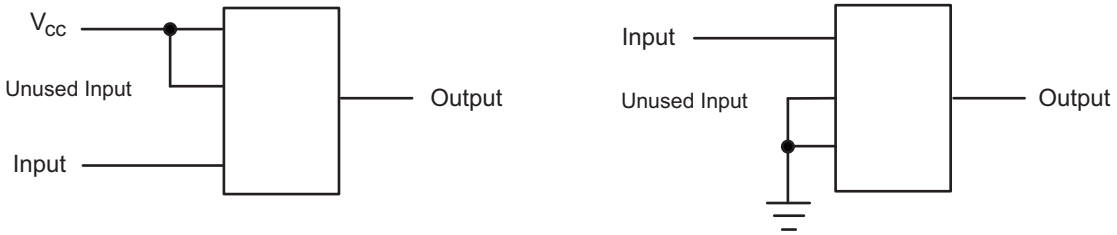


Figure 7. Layout Diagram

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC1G04DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	(A043 ~ A04G ~ A04L ~ A04S)	Samples
SN74AHC1G04DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	A04G	Samples
SN74AHC1G04DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	A04G	Samples
SN74AHC1G04DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	(A043 ~ A04G ~ A04L ~ A04S)	Samples
SN74AHC1G04DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	A04G	Samples
SN74AHC1G04DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AC3 ~ ACG ~ ACL ~ ACS)	Samples
SN74AHC1G04DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AC3 ~ ACG ~ ACL ~ ACS)	Samples
SN74AHC1G04DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AC3 ~ ACG ~ ACL ~ ACS)	Samples
SN74AHC1G04DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AC3 ~ ACG ~ ACL ~ ACS)	Samples
SN74AHC1G04DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AC3 ~ ACG ~ ACL ~ ACS)	Samples
SN74AHC1G04DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AC3 ~ ACG ~ ACL ~ ACS)	Samples
SN74AHC1G04DRLR	ACTIVE	SOT-5X3	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(ACB ~ ACS)	Samples
SN74AHC1G04DRLRG4	ACTIVE	SOT-5X3	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(ACB ~ ACS)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74AHC1G04 :

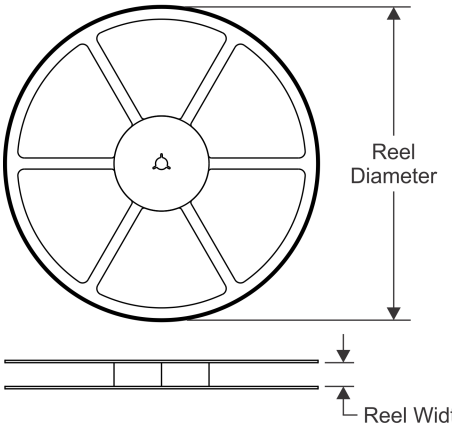
- Automotive: SN74AHC1G04-Q1

NOTE: Qualified Version Definitions:

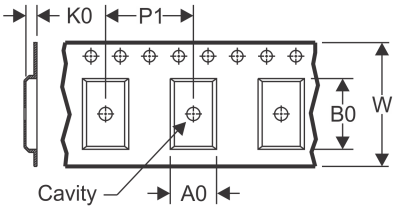
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

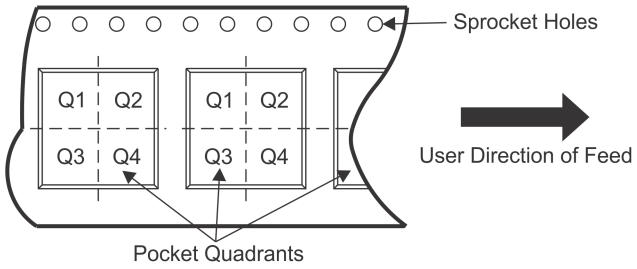


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

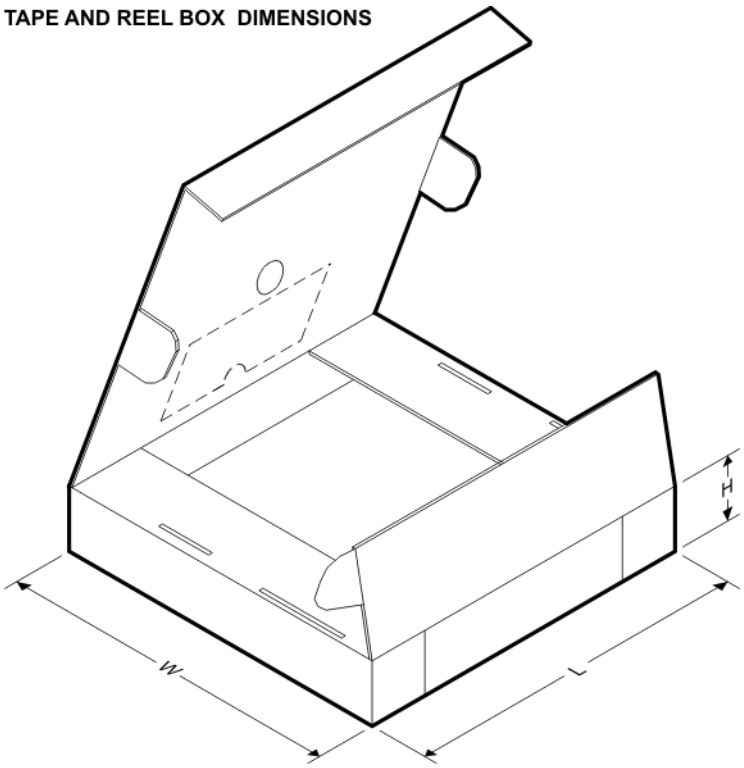
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G04DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74AHC1G04DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G04DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G04DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G04DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74AHC1G04DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G04DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G04DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G04DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G04DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G04DCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AHC1G04DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G04DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

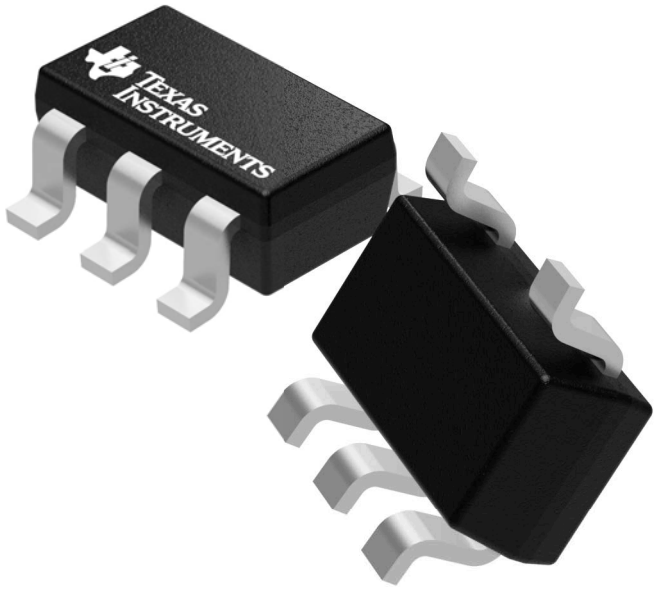


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G04DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G04DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AHC1G04DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G04DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G04DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHC1G04DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHC1G04DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHC1G04DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G04DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G04DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G04DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74AHC1G04DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G04DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



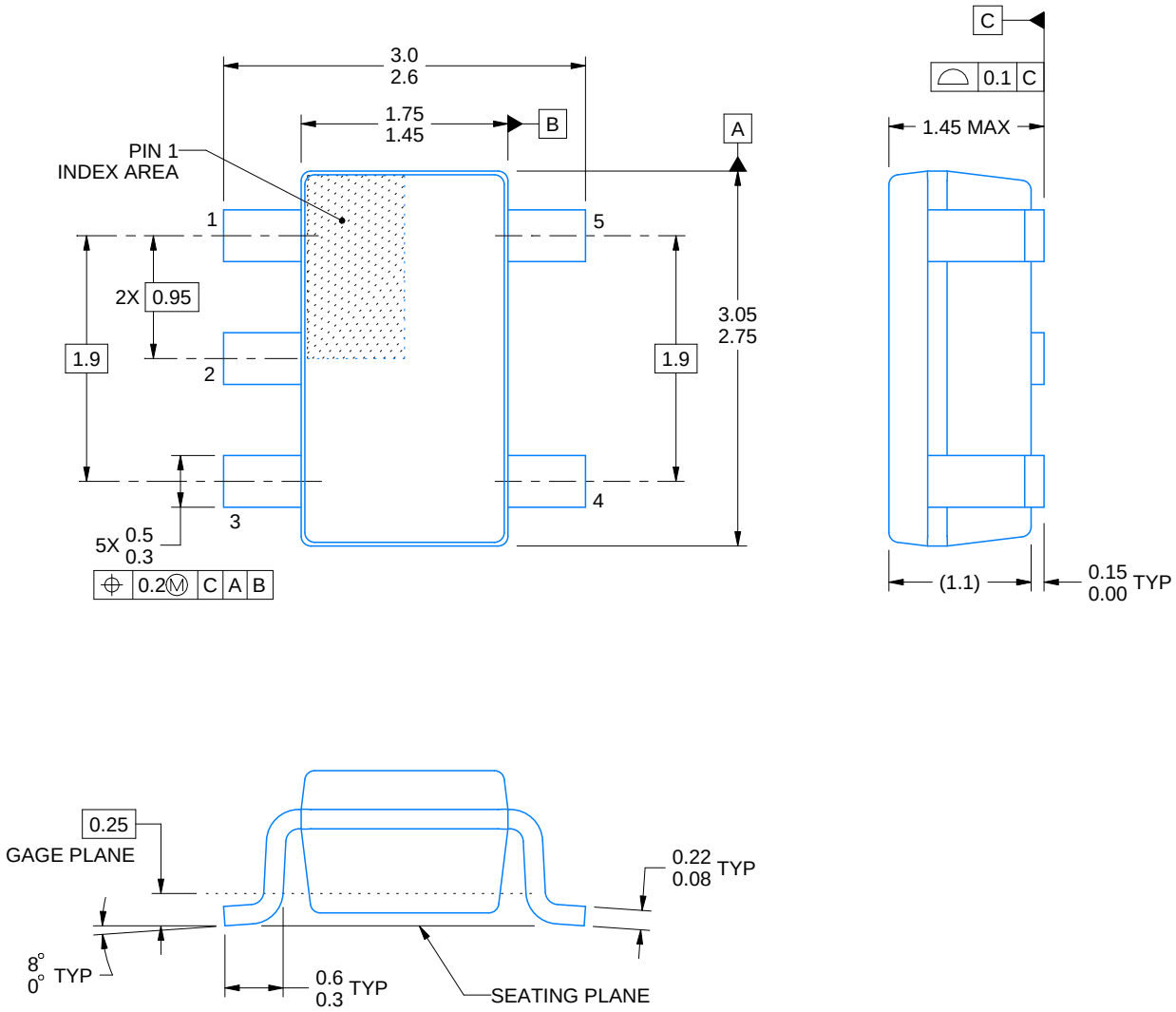
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

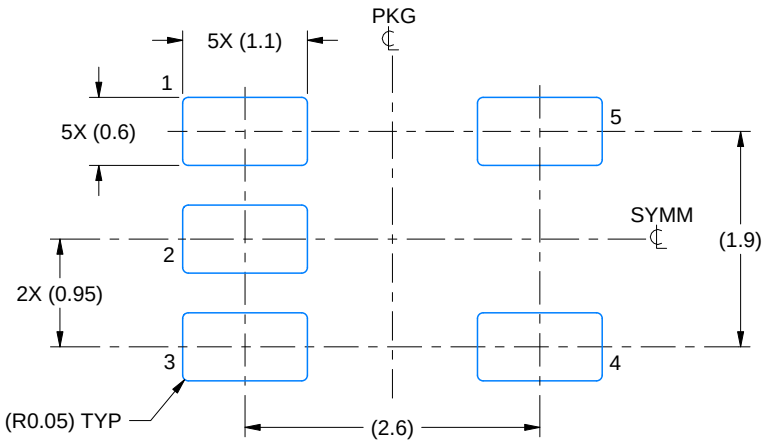
SMALL OUTLINE TRANSISTOR



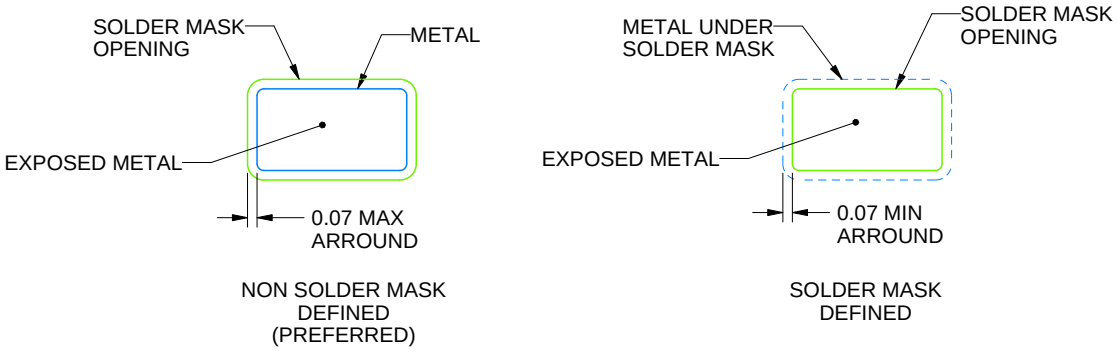
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

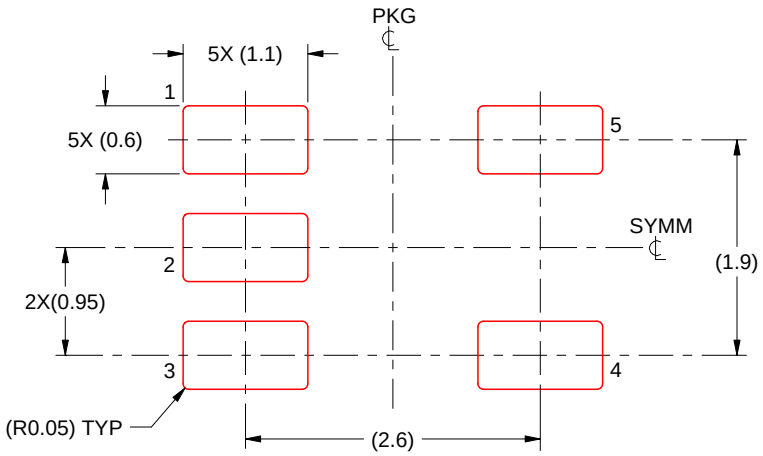


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

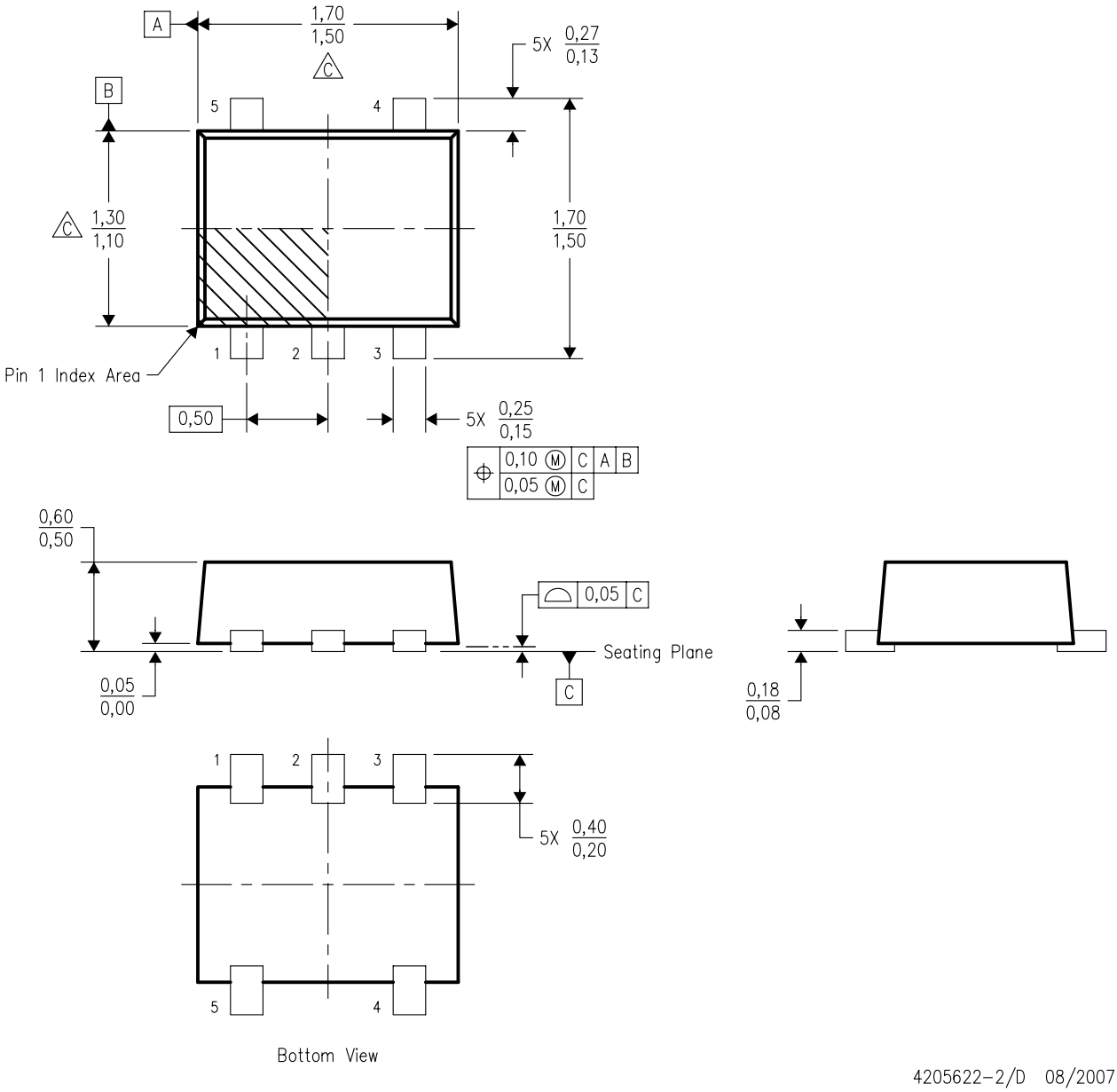


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

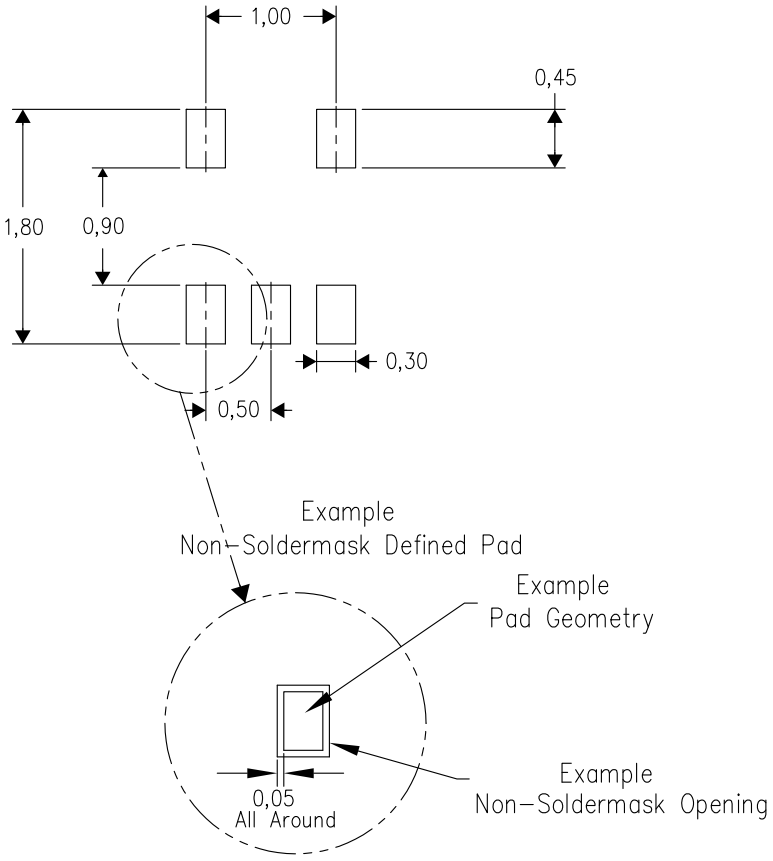
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



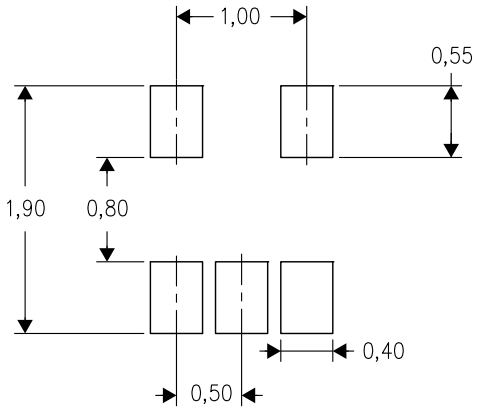
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R–PDSO–N5) PLASTIC SMALL OUTLINE

Example Board Layout



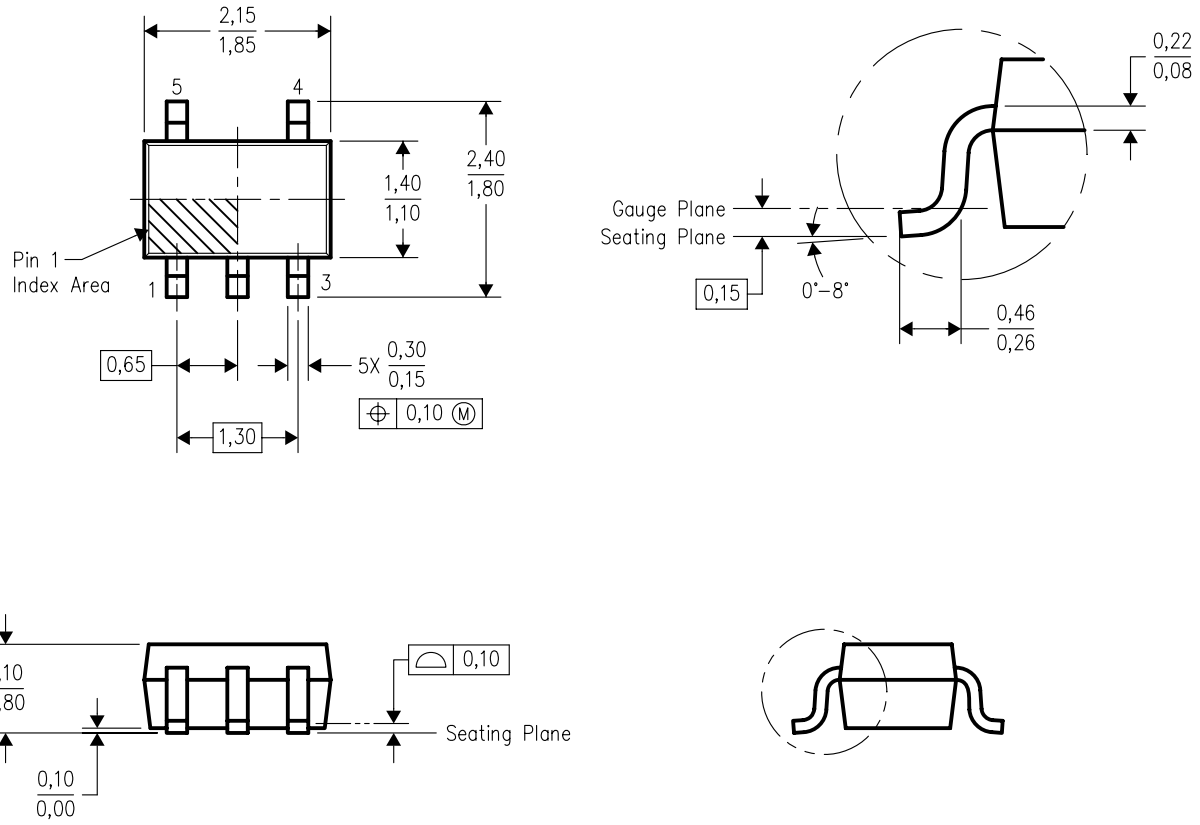
Example Stencil Design
(Note E)



4208207–2/E 06/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

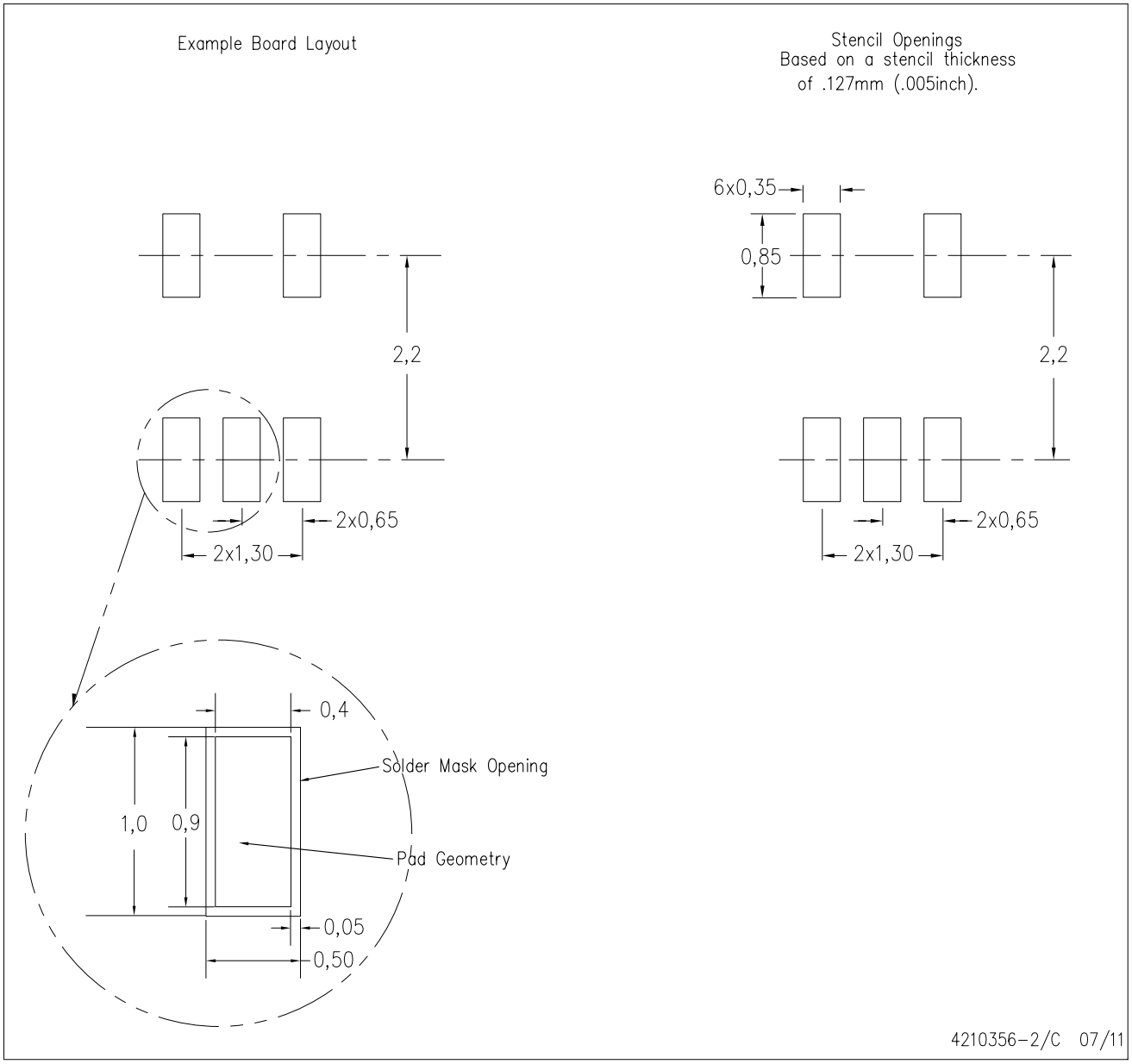
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265