

## SNx4AHC574 Octal Edge-Triggered D-Type Flip-Flops With 3-State Outputs

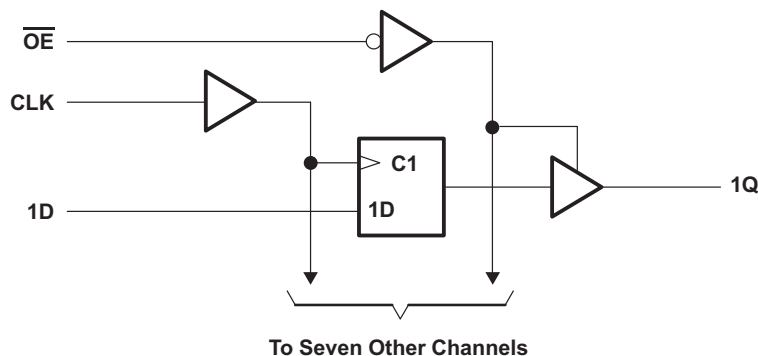
### 1 Features

- Operating Range 2-V to 5.5-V  $V_{CC}$
- 3-State Outputs Drive Bus Lines Directly
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 1000-V Charged-Device Model

### 2 Applications

- Smart Grids
- TVs
- Set Top Boxes
- Audio
- Servers
- Surveillance Cameras
- Network Switches
- Infotainment

### 4 Simplified Schematic



### 3 Description

The SNx4AHC574 devices are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4AHC574	SSOP (20)	7.50 mm × 5.30 mm
	TVSOP (20)	5.00 mm × 4.40 mm
	SOIC (20)	12.80 mm × 7.50 mm
	PDIP (20)	25.40 mm × 6.35 mm
	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>8 Parameter Measurement Information</b> .....	<b>9</b>
<b>2 Applications</b> .....	<b>1</b>	<b>9 Detailed Description</b> .....	<b>10</b>
<b>3 Description</b> .....	<b>1</b>	9.1 Overview .....	10
<b>4 Simplified Schematic</b> .....	<b>1</b>	9.2 Functional Block Diagram .....	10
<b>5 Revision History</b> .....	<b>2</b>	9.3 Feature Description .....	10
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	9.4 Device Functional Modes .....	10
<b>7 Specifications</b> .....	<b>4</b>	<b>10 Application and Implementation</b> .....	<b>11</b>
7.1 Absolute Maximum Ratings .....	4	10.1 Application Information .....	11
7.2 ESD Ratings .....	4	10.2 Typical Application .....	11
7.3 Recommended Operating Conditions .....	4	<b>11 Power Supply Recommendations</b> .....	<b>12</b>
7.4 Thermal Information .....	5	<b>12 Layout</b> .....	<b>13</b>
7.5 Electrical Characteristics .....	5	12.1 Layout Guidelines .....	13
7.6 Timing Requirements, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ .....	5	12.2 Layout Example .....	13
7.7 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....	6	<b>13 Device and Documentation Support</b> .....	<b>13</b>
7.8 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ .....	6	13.1 Related Links .....	13
7.9 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....	7	13.2 Trademarks .....	13
7.10 Noise Characteristics .....	7	13.3 Electrostatic Discharge Caution .....	13
7.11 Operating Characteristics .....	7	13.4 Glossary .....	13
7.12 Typical Characteristics .....	8	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>13</b>

## 5 Revision History

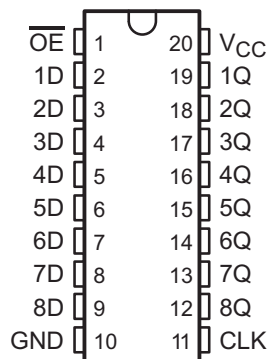
### Changes from Revision I (July 2003) to Revision J

Page

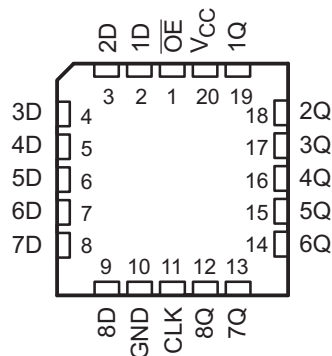
• Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....	1
• Deleted <i>Ordering Information</i> table. ....	1
• Added Military Disclaimer to <i>Features</i> list. ....	1
• Changed MAX operating temperature to 125°C in <i>Recommended Operating Conditions</i> table. ....	4

## 6 Pin Configuration and Functions

SN54AHC574 . . . J OR W PACKAGE  
SN74AHC574 . . . DB, DGV, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AHC574 . . . FK PACKAGE  
(TOP VIEW)



### Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	$\overline{OE}$	I	Output Enable Pin
2	1D	I	1D Input
3	2D	I	2D Input
4	3D	I	3D Input
5	4D	I	4D Input
6	5D	I	5D Input
7	6D	I	6D Input
8	7D	I	7D Input
9	8D	I	8D Input
10	GND	—	Ground Pin
11	CLK	I	Clock Pin
12	8Q	O	8Q Output
13	7Q	O	7Q Output
14	6Q	O	6Q Output
15	5Q	O	5Q Output
16	4Q	O	4Q Output
17	3Q	O	3Q Output
18	2Q	O	2Q Output
19	1Q	O	1Q Output
20	$V_{CC}$	—	Power Pin

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	7	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-20 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±20 mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±25 mA
Continuous current through V <sub>CC</sub> or GND				±75 mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge		
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	1000	
Machine Model (MM)	200		

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54AHC574		SN74AHC574		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V		1.5		V
		V <sub>CC</sub> = 3 V		2.1		
		V <sub>CC</sub> = 5.5 V		3.85		
V <sub>IL</sub>	Low-level Input voltage	V <sub>CC</sub> = 2 V		0.5		V
		V <sub>CC</sub> = 3 V		0.9		
		V <sub>CC</sub> = 5.5 V		1.65		
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		-50		μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V		-4		mA
		V <sub>CC</sub> = 5 V ± 0.5 V		-8		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50		μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V		4		mA
		V <sub>CC</sub> = 5 V ± 0.5 V		8		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V		100		ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V		20		
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	125	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AHC574						UNIT
		DB	DGV	DW	N	NS	PW	
		20 PINS						
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	97.9	117.2	79.4	53.3	79.2	103.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	59.6	32.7	45.7	40.0	45.7	37.8	
R <sub>θJB</sub>	Junction-to-board thermal resistance	53.1	58.7	46.9	34.2	46.8	54.3	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	21.3	1.15	18.7	26.4	19.3	2.9	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	52.7	58.0	46.5	34.1	46.4	53.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

## 7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC574		SN74AHC574				UNIT
						–40°C to 85°C		–40°C to 85°C		–40°C to 125°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	2 V	1.9	2	1.9		1.9		1.9		V	
		3 V	2.9	3	2.9		2.9		2.9			
		4.5 V	4.4	4.5	4.4		4.4		4.4			
	I <sub>OH</sub> = –4 mA	3 V	2.58		2.48		2.48		2.48			
		4.5 V	3.94		3.8		3.8		3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V		0.1		0.1		0.1		0.1	V	
		3 V		0.1		0.1		0.1		0.1		
		4.5 V		0.1		0.1		0.1		0.1		
	I <sub>OH</sub> = 4 mA	3 V		0.36		0.5		0.44		0.44		
		4.5 V		0.36		0.5		0.44		0.44		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V		±0.1		±1 <sup>(1)</sup>		±1		±1	μA	
I <sub>OZ</sub> <sup>(2)</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND V <sub>I</sub> (OE) = V <sub>IL</sub> or V <sub>IH</sub>	5.5 V		±0.25		±2.5		±2.5		±2.5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		4		40		40		40	μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		3	10			10		10	pF	
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		3							pF	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

(2) For input and output pins, I<sub>OZ</sub> includes the input leakage current.

## 7.6 Timing Requirements, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER		T <sub>A</sub> = 25°C		SN54AHC574		SN74AHC574				UNIT
				–40°C to 85°C		–40°C to 85°C		–40°C to 125°C		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, CLK high or low	5		5		5		5.5		ns
t <sub>su</sub>	Setup time, data before CLK↑	3.5		3.5		3.5		4		ns
t <sub>h</sub>	Hold time, data after CLK↑	1.5		1.5		1.5		2		ns

## 7.7 Timing Requirements, $V_{CC} = 5 V \pm 0.5 V$

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER		$T_A = 25^\circ\text{C}$		SN54AHC574		SN74AHC574		UNIT		
				–40°C to 85°C		–40°C to 85°C			–40°C to 125°C	
		MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX
$t_w$	Pulse duration, CLK high or low	5		5		5		5.5		ns
$t_{su}$	Setup time, data before CLK $\uparrow$	3		3		3		3.5		ns
$t_h$	Hold time, data after CLK $\uparrow$	1.5		1.5		1.5		2		ns

## 7.8 Switching Characteristics, $V_{CC} = 3.3 V \pm 0.3 V$

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$		SN54AHC574		SN74AHC574			UNIT		
						–40°C to 85°C		–40°C to 85°C		–40°C to 125°C			
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		MIN	MAX
$f_{MAX}$			$C_L = 15\text{ pF}$	80 <sup>(1)</sup>	125 <sup>(1)</sup>		65 <sup>(1)</sup>		65		65	MHz	
			$C_L = 50\text{ pF}$	50	75		45		45		45		
$t_{PLH}$	CLK	Q	$C_L = 15\text{ pF}$		8.5 <sup>(1)</sup>	13.2 <sup>(1)</sup>	1 <sup>(1)</sup>	15.5 <sup>(1)</sup>	1	15.5	1	17	ns
$t_{PHL}$					8.5 <sup>(1)</sup>	13.2 <sup>(1)</sup>	1 <sup>(1)</sup>	15.5 <sup>(1)</sup>	1	15.5	1	17	
$t_{PZH}$	$\overline{OE}$	Q	$C_L = 15\text{ pF}$		8.2 <sup>(1)</sup>	12.8 <sup>(1)</sup>	1 <sup>(1)</sup>	15 <sup>(1)</sup>	1	15	1	16	ns
$t_{PZL}$					8.2 <sup>(1)</sup>	12.8 <sup>(1)</sup>	1 <sup>(1)</sup>	15 <sup>(1)</sup>	1	15	1	16	
$t_{PHZ}$	$\overline{OE}$	Q	$C_L = 15\text{ pF}$		8.5 <sup>(1)</sup>	13 <sup>(1)</sup>	1 <sup>(1)</sup>	15 <sup>(1)</sup>	1	15	1	16	ns
$t_{PLZ}$					8.5 <sup>(1)</sup>	13 <sup>(1)</sup>	1 <sup>(1)</sup>	15 <sup>(1)</sup>	1	15	1	16	
$t_{PLH}$	CLK	Q	$C_L = 50\text{ pF}$		11	16.7	1	19	1	19	1	20.5	ns
$t_{PHL}$					11	16.7	1	19	1	19	1	20.5	
$t_{PZH}$	$\overline{OE}$	Q	$C_L = 50\text{ pF}$		10.7	16.3	1	18.5	1	18.5	1	19.5	ns
$t_{PZL}$					10.7	16.3	1	18.5	1	18.5	1	19.5	
$t_{PHZ}$	$\overline{OE}$	Q	$C_L = 50\text{ pF}$		11	15	1	17	1	17	1	18	ns
$t_{PLZ}$					11	15	1	17	1	17	1	18	
$t_{sk(o)}$			$C_L = 50\text{ pF}$			1.5 <sup>(2)</sup>						1.5	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 7.9 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$		SN54AHC574		SN74AHC574				UNIT
						–40°C to 85°C		–40°C to 85°C		–40°C to 125°C		
						MIN	TYP	MIN	MAX	MIN	MAX	
$f_{\text{MAX}}$			$C_L = 15\text{ pF}$	130 <sup>(1)</sup>	180 <sup>(1)</sup>	110 <sup>(1)</sup>		110		110		MHz
			$C_L = 50\text{ pF}$	85	115	75		75		75		
$t_{\text{PLH}}$	CLK	Q	$C_L = 15\text{ pF}$	5.6 <sup>(1)</sup>	8.6 <sup>(1)</sup>	1 <sup>(1)</sup>	10 <sup>(1)</sup>	1	10	1	11	ns
$t_{\text{PHL}}$				5.6 <sup>(1)</sup>	8.6 <sup>(1)</sup>	1 <sup>(1)</sup>	10 <sup>(1)</sup>	1	10	1	11	
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	$C_L = 15\text{ pF}$	5.9 <sup>(1)</sup>	9 <sup>(1)</sup>	1 <sup>(1)</sup>	10.5 <sup>(1)</sup>	1	10.5	1	11.5	ns
$t_{\text{PZL}}$				5.9 <sup>(1)</sup>	9 <sup>(1)</sup>	1 <sup>(1)</sup>	10.5 <sup>(1)</sup>	1	10.5	1	11.5	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	$C_L = 15\text{ pF}$	5.5 <sup>(1)</sup>	9 <sup>(1)</sup>	1 <sup>(1)</sup>	10.5 <sup>(1)</sup>	1	10.5	1	11.5	ns
$t_{\text{PLZ}}$				5.5 <sup>(1)</sup>	9 <sup>(1)</sup>	1 <sup>(1)</sup>	10.5 <sup>(1)</sup>	1	10.5	1	11.5	
$t_{\text{PLH}}$	CLK	Q	$C_L = 50\text{ pF}$	7.1	10.6	1	12	1	12	1	13	ns
$t_{\text{PHL}}$				7.1	10.6	1	12	1	12	1	13	
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	$C_L = 50\text{ pF}$	7.4	11	1	12.5	1	12.5	1	13.5	ns
$t_{\text{PZL}}$				7.4	11	1	12.5	1	12.5	1	13.5	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	$C_L = 50\text{ pF}$	7.1	10.1	1	11.5	1	11.5	1	12.5	ns
$t_{\text{PLZ}}$				7.1	10.1	1	11.5	1	11.5	1	12.5	
$t_{\text{sk}(o)}$			$C_L = 50\text{ pF}$		1 <sup>(2)</sup>				1		1	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 7.10 Noise Characteristics

 $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ <sup>(1)</sup>

PARAMETER		SN74AHC574		UNIT
		MIN	MAX	
$V_{\text{OL}(P)}$	Quiet output, maximum dynamic $V_{\text{OL}}$	0.8		V
$V_{\text{OL}(V)}$	Quiet output, minimum dynamic $V_{\text{OL}}$	–0.8		V
$V_{\text{OH}(V)}$	Quiet output, minimum dynamic $V_{\text{OH}}$	4.2		V
$V_{\text{IH}(D)}$	High-level dynamic input voltage	3.5		V
$V_{\text{IL}(D)}$	Low-level dynamic input voltage	1.5		V

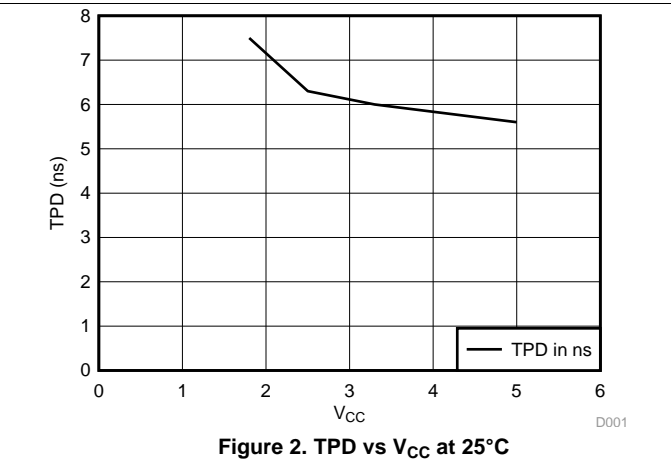
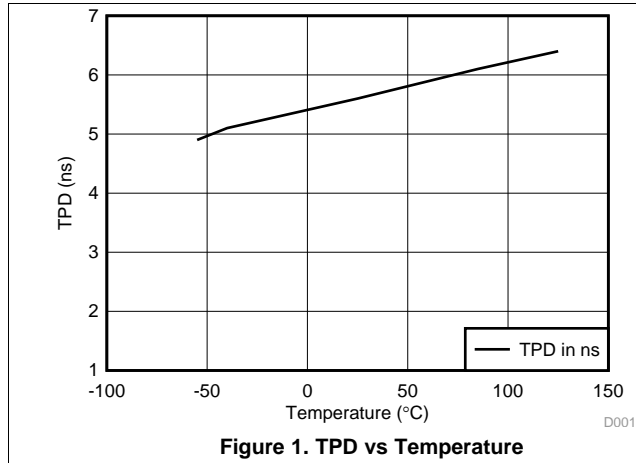
(1) Characteristics are for surface-mount packages only.

## 7.11 Operating Characteristics

 $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

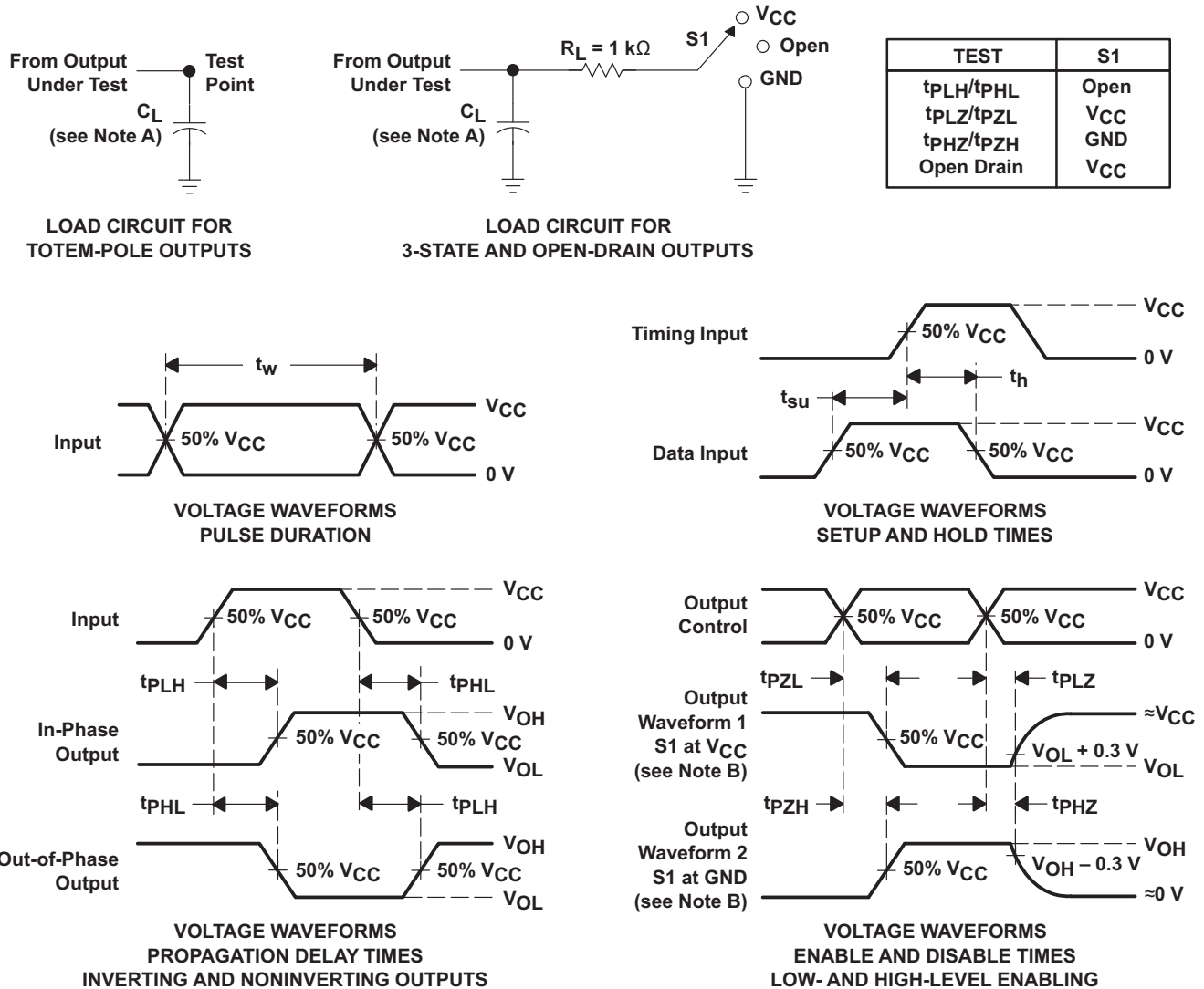
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance No load, $f = 1\text{ MHz}$	28	pF

## 7.12 Typical Characteristics





## 8 Parameter Measurement Information



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

## 9 Detailed Description

### 9.1 Overview

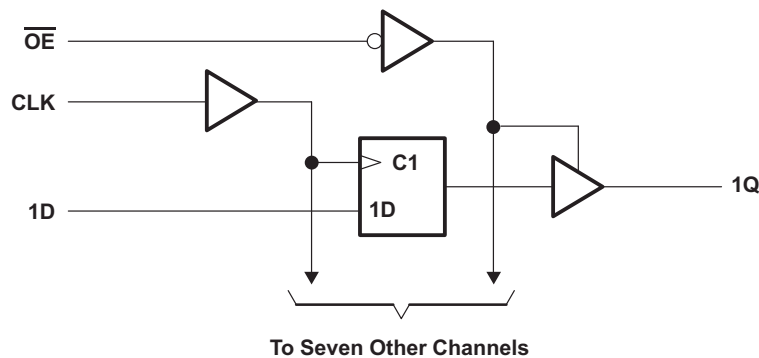
The SNx4AHC574 devices are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

The states of the Q outputs are not predictable until the first valid clock.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pull-up components.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

- 5.5-V tolerant input allows for 5 V to 3.3 V voltage translation
- Slow edges reduce output ringing

### 9.4 Device Functional Modes

**Table 1. Function Table  
(Each Flip-Flop)**

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

SN74AHC574 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid  $V_{CC}$  making it ideal for down translation

### 10.2 Typical Application

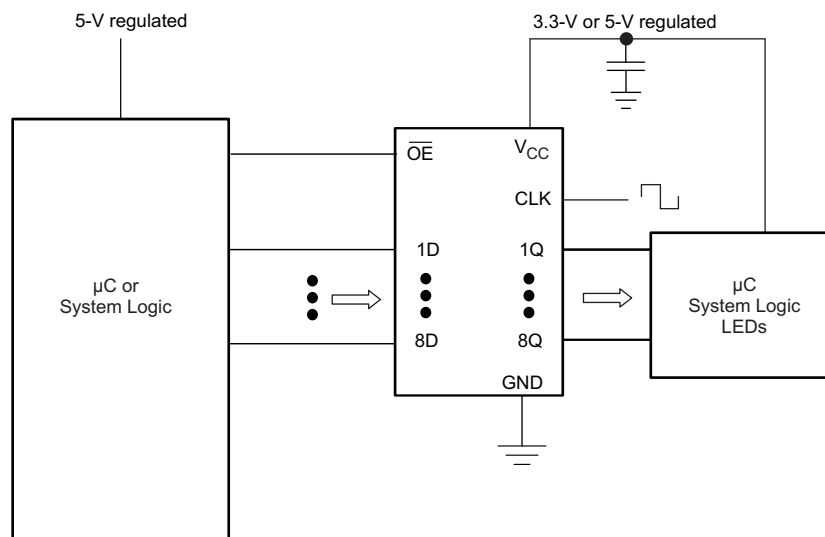


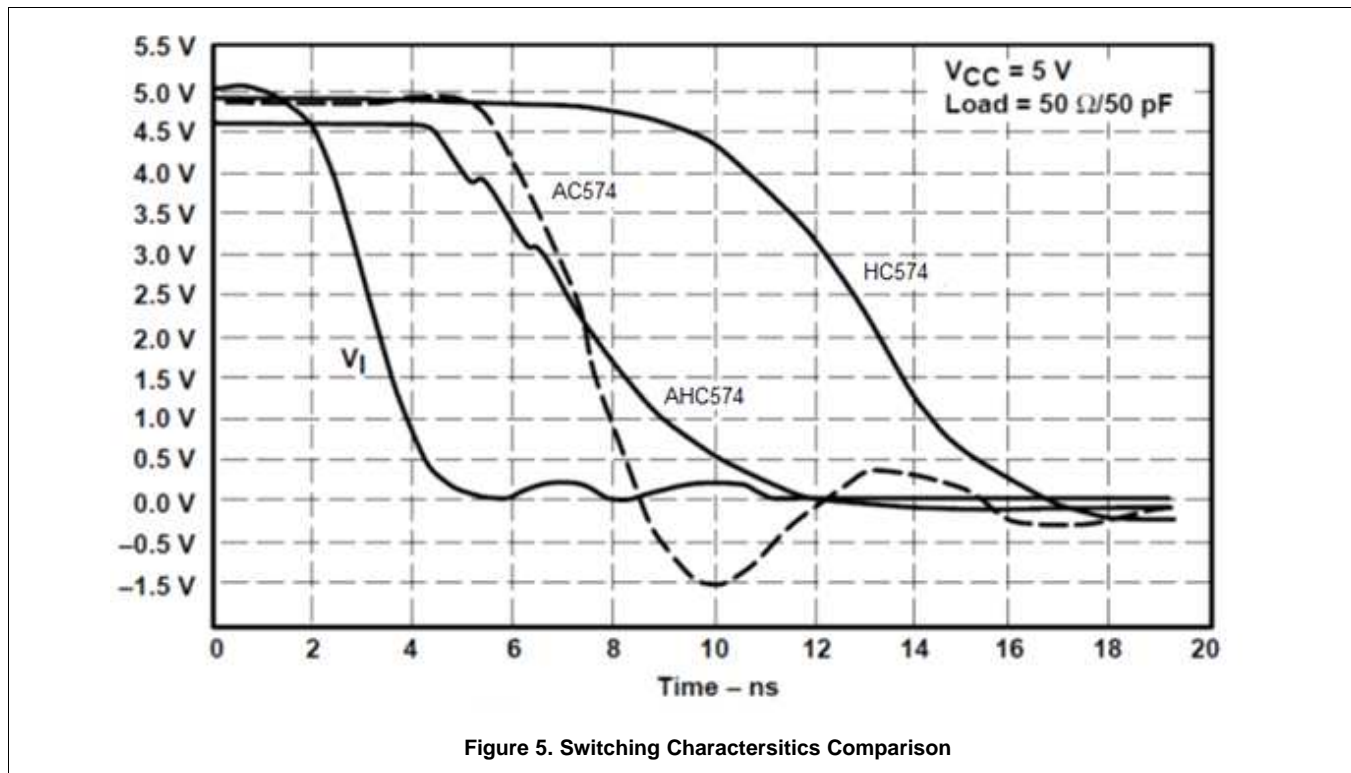
Figure 4. Typical Application Schematic

#### 10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - For rise time and fall time specifications, see  $\Delta t/\Delta V$  in the [Recommended Operating Conditions](#) table.
  - For specified High and low levels, see  $V_{IH}$  and  $V_{IL}$  in the [Recommended Operating Conditions](#) table.
2. Recommend Output Conditions
  - Load currents should not exceed 25 mA per output and 75 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

**Typical Application (continued)**
**10.2.3 Application Curves**

**11 Power Supply Recommendations**

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 6](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

### 12.2 Layout Example

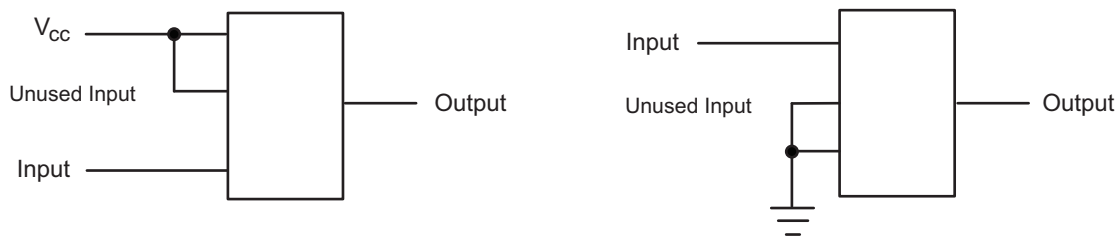


Figure 6. Layout Diagram

## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

### 13.2 Trademarks

All trademarks are the property of their respective owners.

### 13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.4 Glossary

[SLYZ022](#) — *TI Glossary*.




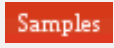
This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9685401Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9685401Q2A SNJ54AHC 574FK	<a href="#">Samples</a>
5962-9685401QRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9685401QR A SNJ54AHC574J	<a href="#">Samples</a>
5962-9685401QSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9685401QS A SNJ54AHC574W	<a href="#">Samples</a>
SN74AHC574DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574	<a href="#">Samples</a>
SN74AHC574DGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574	<a href="#">Samples</a>
SN74AHC574DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574	<a href="#">Samples</a>
SN74AHC574DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574	<a href="#">Samples</a>
SN74AHC574DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574	<a href="#">Samples</a>
SN74AHC574DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574	<a href="#">Samples</a>
SN74AHC574N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC574N	<a href="#">Samples</a>
SN74AHC574NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574	<a href="#">Samples</a>
SN74AHC574PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574	<a href="#">Samples</a>
SN74AHC574PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574	<a href="#">Samples</a>
SN74AHC574PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574	<a href="#">Samples</a>
SN74AHC574PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC574PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574	
SNJ54AHC574FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9685401Q2A SNJ54AHC 574FK	
SNJ54AHC574J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9685401QR A SNJ54AHC574J	
SNJ54AHC574W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9685401QS A SNJ54AHC574W	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54AHC574, SN74AHC574 :**

- Catalog: [SN74AHC574](#)
- Military: [SN54AHC574](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC574DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHC574DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC574DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC574NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHC574PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC574DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74AHC574DGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74AHC574DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHC574NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AHC574PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

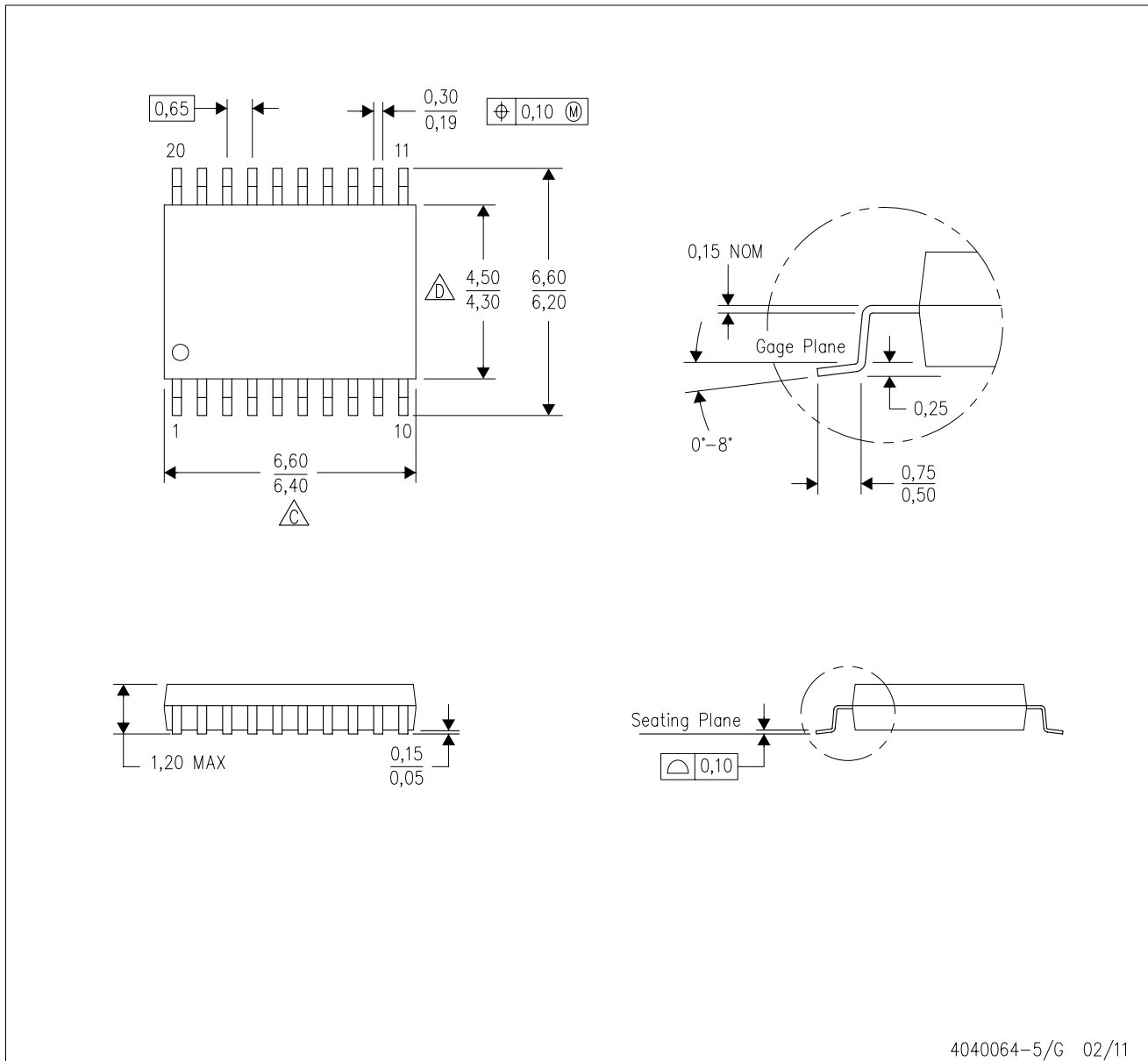
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

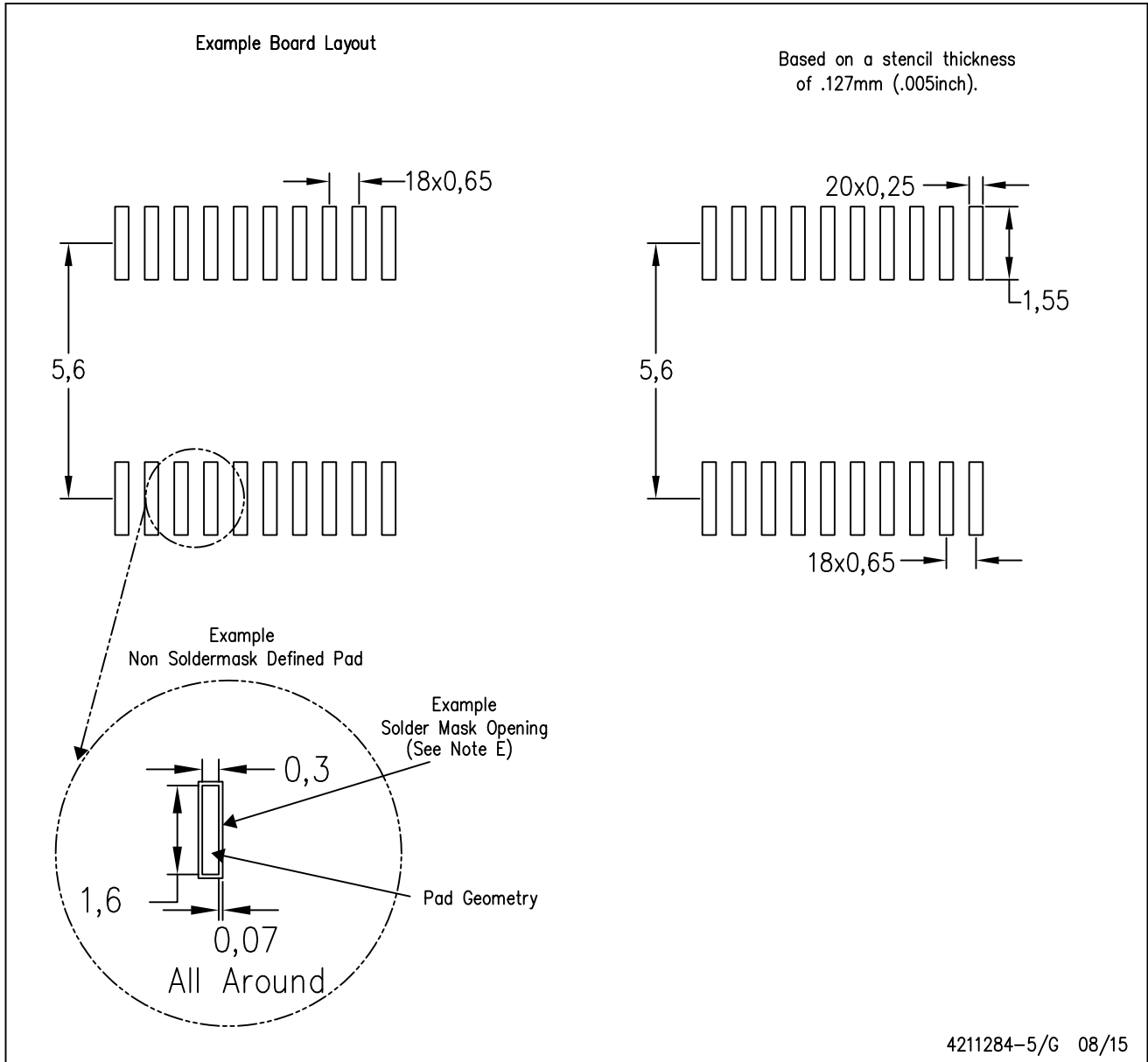


4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002



# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

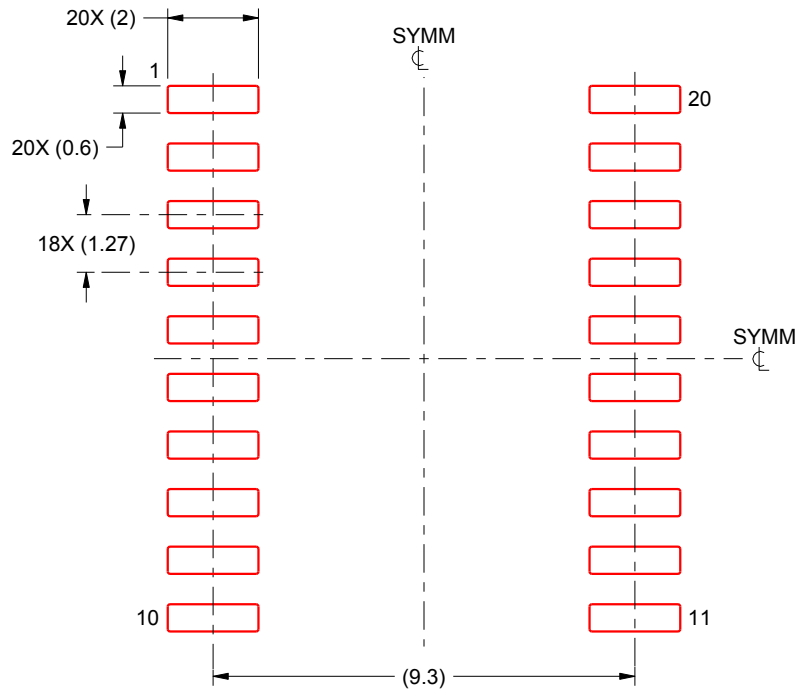
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

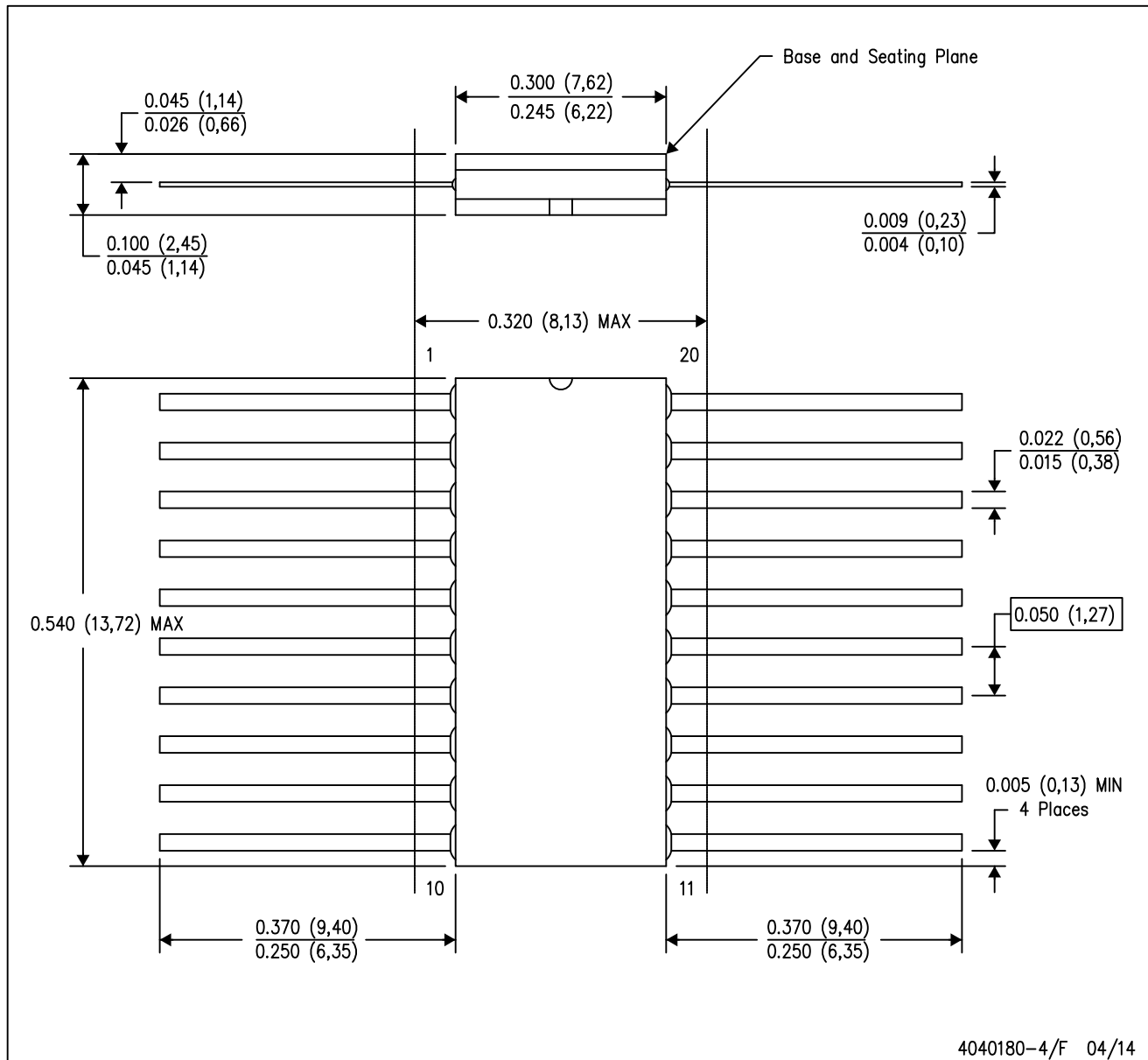
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



4040180-4/F 04/14

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.