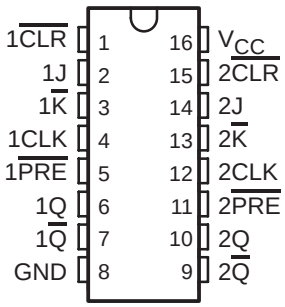
- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

| TYPE | TYPICAL MAXIMUM CLOCK FREQUENCY (MHz) | TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW) |
|---|---|---|
| ′ALS109A | 50 | 6 |
| ′AS109A | 129 | 29 |

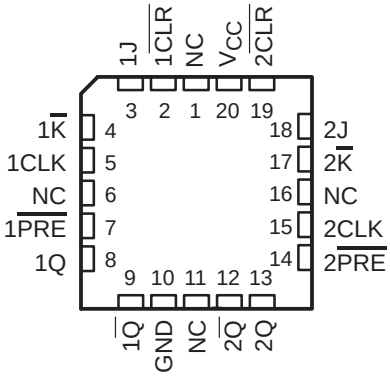
**SN54ALS109A, SN54AS109A . . . J PACKAGE**
**SN74ALS109A, SN74AS109A . . . D OR N PACKAGE**
**(TOP VIEW)**




## description

These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and $\overline{K}$ inputs can be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and tying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

**SN54ALS109A, SN54AS109A . . . FK PACKAGE**
**(TOP VIEW)**




NC − No internal connection

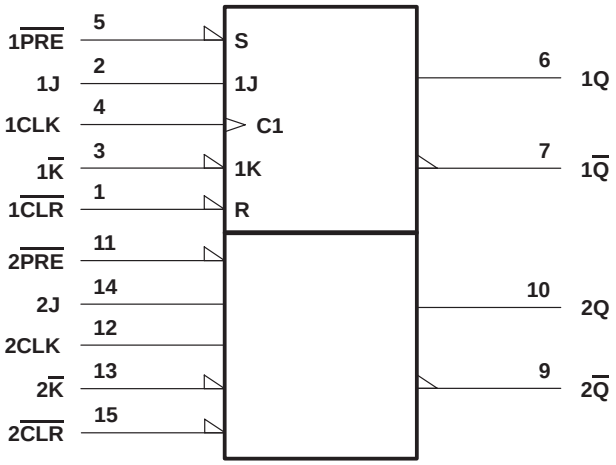
The SN54ALS109A and SN54AS109A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS109A and SN74AS109A are characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | J | $\overline{K}$ | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H† | H† |
| H | H | ↑ | L | L | L | H |
| H | H | ↑ | H | L | Toggle | |
| H | H | ↑ | L | H | Q0 | $\overline{Q}$0 |
| H | H | ↑ | H | H | H | L |
| H | H | L | X | X | Q0 | $\overline{Q}$0 |

† The output levels in this configuration are not specified to meet the minimum levels for $V_{OH}$ if the lows at $\overline{PRE}$ and $\overline{CLR}$ are near $V_{IL}$ maximum. Furthermore, this configuration is nonstable; that is, it does not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ . . . . . 7 V
Operating free-air temperature range, $T_A$: SN54ALS109A . . . . . −55°C to 125°C
SN74ALS109A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | | SN54ALS109A | | | SN74ALS109A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | 4 | | | 8 | mA |
| $f_{clock}$ | Clock frequency | | 0 | | 30 | 0 | | 34 | MHz |
| $t_w$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ low | 15 | | | 15 | | | ns |
| | | CLK high | 16.5 | | | 14.5 | | | |
| | | CLK low | 16.5 | | | 14.5 | | | |
| $t_{su}$ | Setup time before CLK↑ | Data | 15 | | | 15 | | | ns |
| | | $\overline{PRE}$ or $\overline{CLR}$ inactive | 10 | | | 10 | | | |
| $t_h$ | Hold time after CLK↑ | Data | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54ALS109A | | | SN74ALS109A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −0.4 mA | $V_{CC}$−2 | | | $V_{CC}$−2 | | | V |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | CLK, J, or $\overline{K}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| | $\overline{PRE}$ or $\overline{CLR}$ | | | | | 0.2 | | | 0.2 | |
| $I_{IH}$ | CLK, J, or $\overline{K}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| | $\overline{PRE}$ or $\overline{CLR}$ | | | | | 40 | | | 40 | |
| $I_{IL}$ | CLK, J, or $\overline{K}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.2 | | | −0.2 | mA |
| | $\overline{PRE}$ or $\overline{CLR}$ | | | | | −0.4 | | | −0.4 | |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −20 | | −112 | −30 | | −112 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | See Note 1 | | 2.4 | 4 | | 2.4 | 4 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.
NOTE 1: $I_{CC}$ is measured with J, $\overline{K}$, CLK, and $\overline{PRE}$ grounded, then with J, $\overline{K}$, CLK, and $\overline{CLR}$ grounded.

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54ALS109A | | SN74ALS109A | | |
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 30 | | 34 | | MHz |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | 3 | 17 | 3 | 13 | ns |
| $t_{PHL}$ | | | 5 | 17 | 5 | 15 | |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | 5 | 21 | 5 | 16 | ns |
| $t_{PHL}$ | | | 5 | 20 | 5 | 18 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ . . . . . 7 V
Operating free-air temperature range, $T_A$: SN54AS109A . . . . . −55°C to 125°C
SN74AS109A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | | SN54AS109A | | | SN74AS109A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −2 | | | −2 | mA |
| $I_{OL}$ | Low-level output current | | | | 20 | | | 20 | mA |
| $f_{clock}$* | Clock frequency | | 0 | | 90 | 0 | | 105 | MHz |
| $t_w$* | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ low | 4 | | | 4 | | | ns |
| | | CLK high | 4 | | | 4 | | | |
| | | CLK low | 5.5 | | | 5.5 | | | |
| $t_{su}$* | Setup time before CLK↑ | Data | 5.5 | | | 5.5 | | | ns |
| | | $\overline{PRE}$ or $\overline{CLR}$ inactive | 2 | | | 2 | | | |
| $t_h$* | Hold time after CLK↑ | Data | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54AS109A | | | SN74AS109A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −2 mA | $V_{CC}$−2 | | | $V_{CC}$−2 | | | V |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.25 | 0.5 | | 0.25 | 0.5 | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | CLK, J, or $\overline{K}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| | $\overline{PRE}$ or $\overline{CLR}$ | | | | | 40 | | | 40 | |
| $I_{IL}$ | CLK, J, or $\overline{K}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.5 | | | −0.5 | mA |
| | $\overline{PRE}$ or $\overline{CLR}$ | | | | | −1.8 | | | −1.8 | |
| $I_O$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −30 | | −112 | −30 | | −112 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | See Note 1 | | 11.5 | 17 | | 11.5 | 17 | mA |

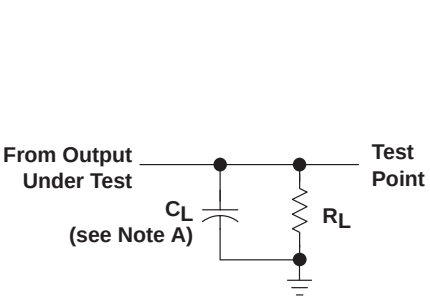
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.
NOTE 1: $I_{CC}$ is measured with J, $\overline{K}$, CLK, and $\overline{PRE}$ grounded, then with J, $\overline{K}$, CLK, and $\overline{CLR}$ grounded.

## switching characteristics (see Figure 1)

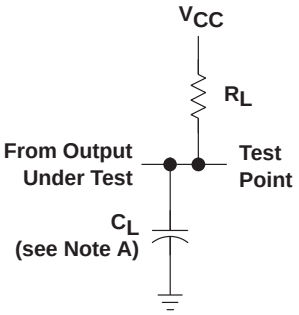
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54AS109A | | SN74AS109A | | |
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$* | | | 90 | | 105 | | MHz |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | 2 | 9 | 2 | 8 | ns |
| $t_{PHL}$ | | | 3.5 | 11.5 | 3.5 | 10.5 | |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | 2.5 | 10 | 2.5 | 9 | ns |
| $t_{PHL}$ | | | 3.5 | 10.5 | 3.5 | 9 | |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

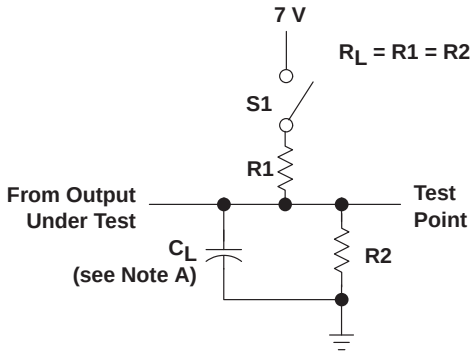
## PARAMETER MEASUREMENT INFORMATION
## SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



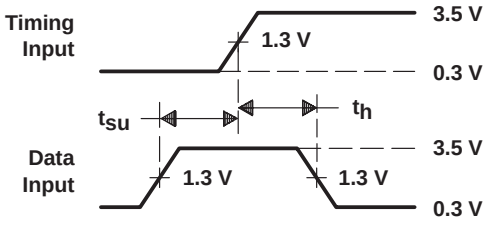

LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



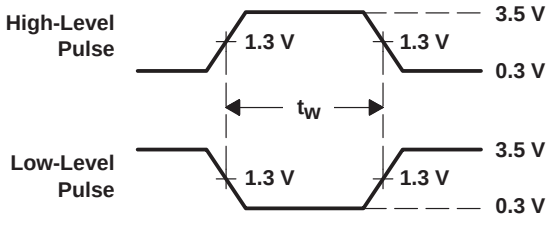

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



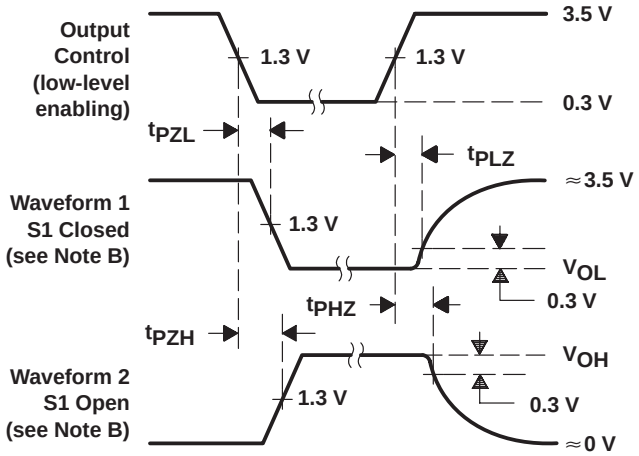

LOAD CIRCUIT
FOR 3-STATE OUTPUTS



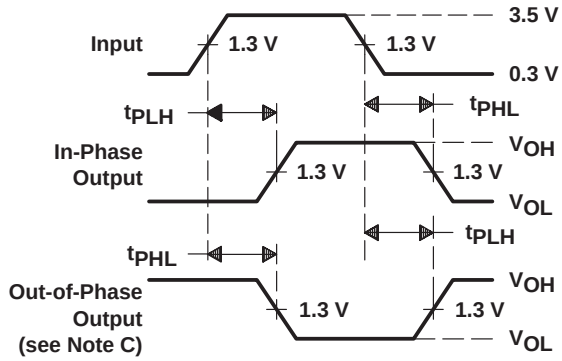

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251−1443

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 84000012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 84000012A SNJ54ALS 109AFK | Samples |
| 8400001EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8400001EA SNJ54ALS109AJ | Samples |
| JM38510/37102B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 37102B2A | Samples |
| JM38510/37102BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 37102BEA | Samples |
| M38510/37102B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 37102B2A | Samples |
| M38510/37102BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 37102BEA | Samples |
| SN54ALS109AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54ALS109AJ | Samples |
| SN74ALS109AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS109A | Samples |
| SN74ALS109ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS109A | Samples |
| SN74ALS109AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS109AN | Samples |
| SN74ALS109ANE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS109AN | Samples |
| SN74ALS109ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS109A | Samples |
| SN74AS109AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS109A | Samples |
| SN74AS109AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS109AN | Samples |
| SN74AS109ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74AS109A | Samples |
| SNJ54ALS109AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 84000012A SNJ54ALS 109AFK | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SNJ54ALS109AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8400001EA SNJ54ALS109AJ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN54ALS109A, SN74ALS109A :**

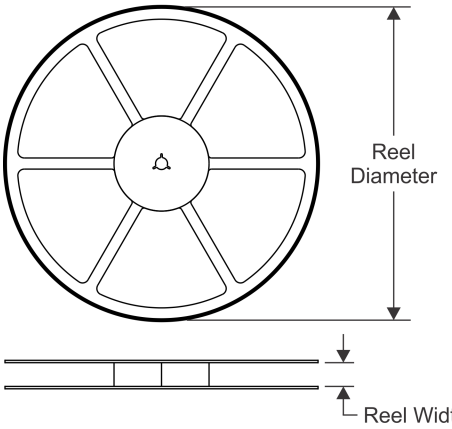
- Catalog: SN74ALS109A
- Military: SN54ALS109A

NOTE: Qualified Version Definitions:

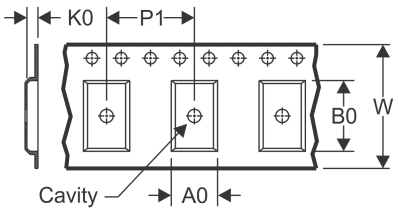
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

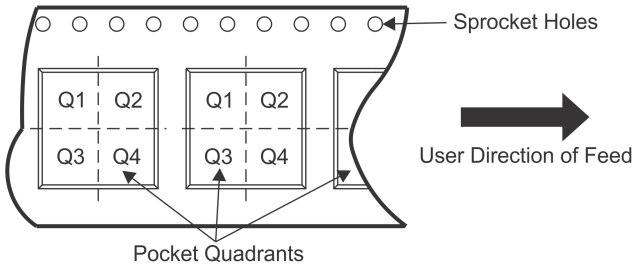



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

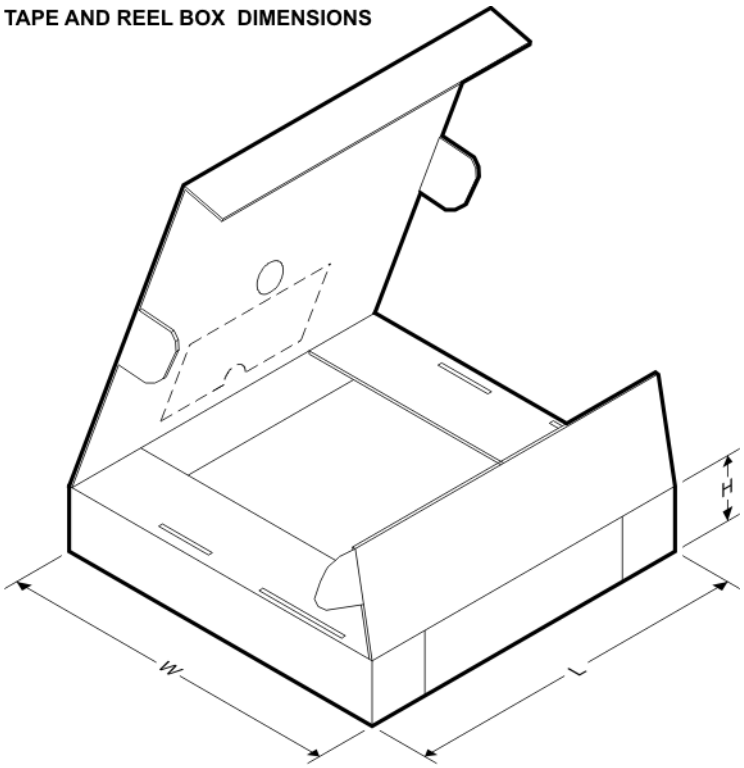
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ALS109ANSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AS109ANSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

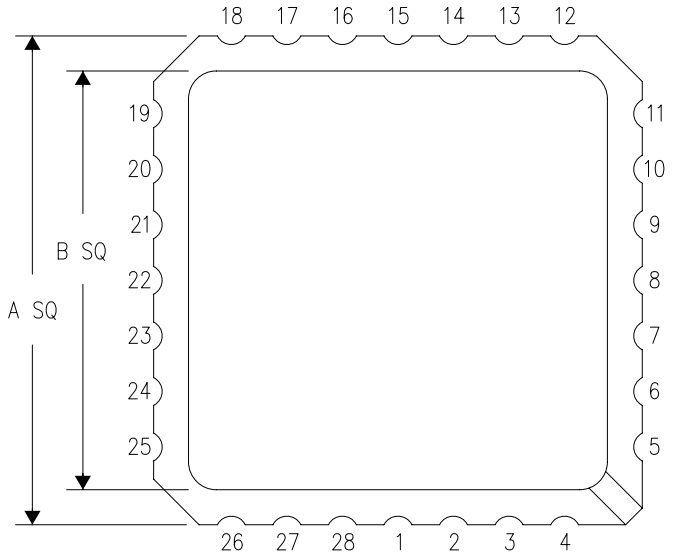



*All dimensions are nominal

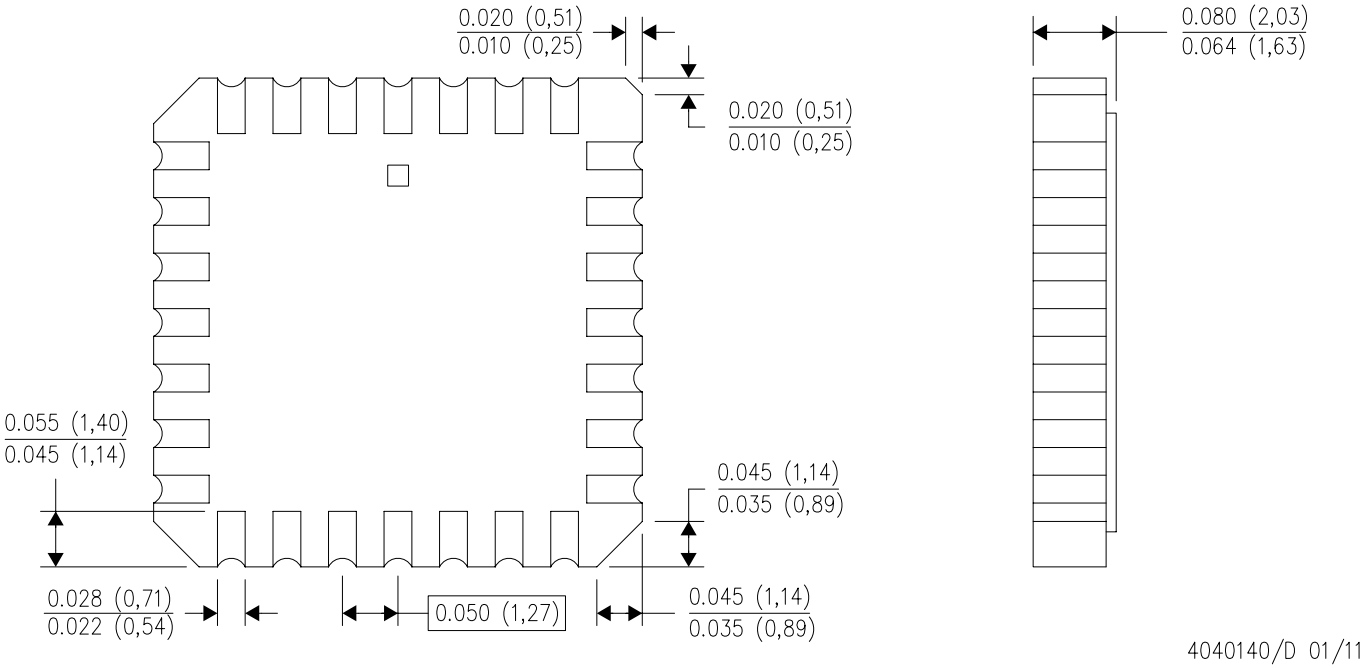
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74ALS109ANSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74AS109ANSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



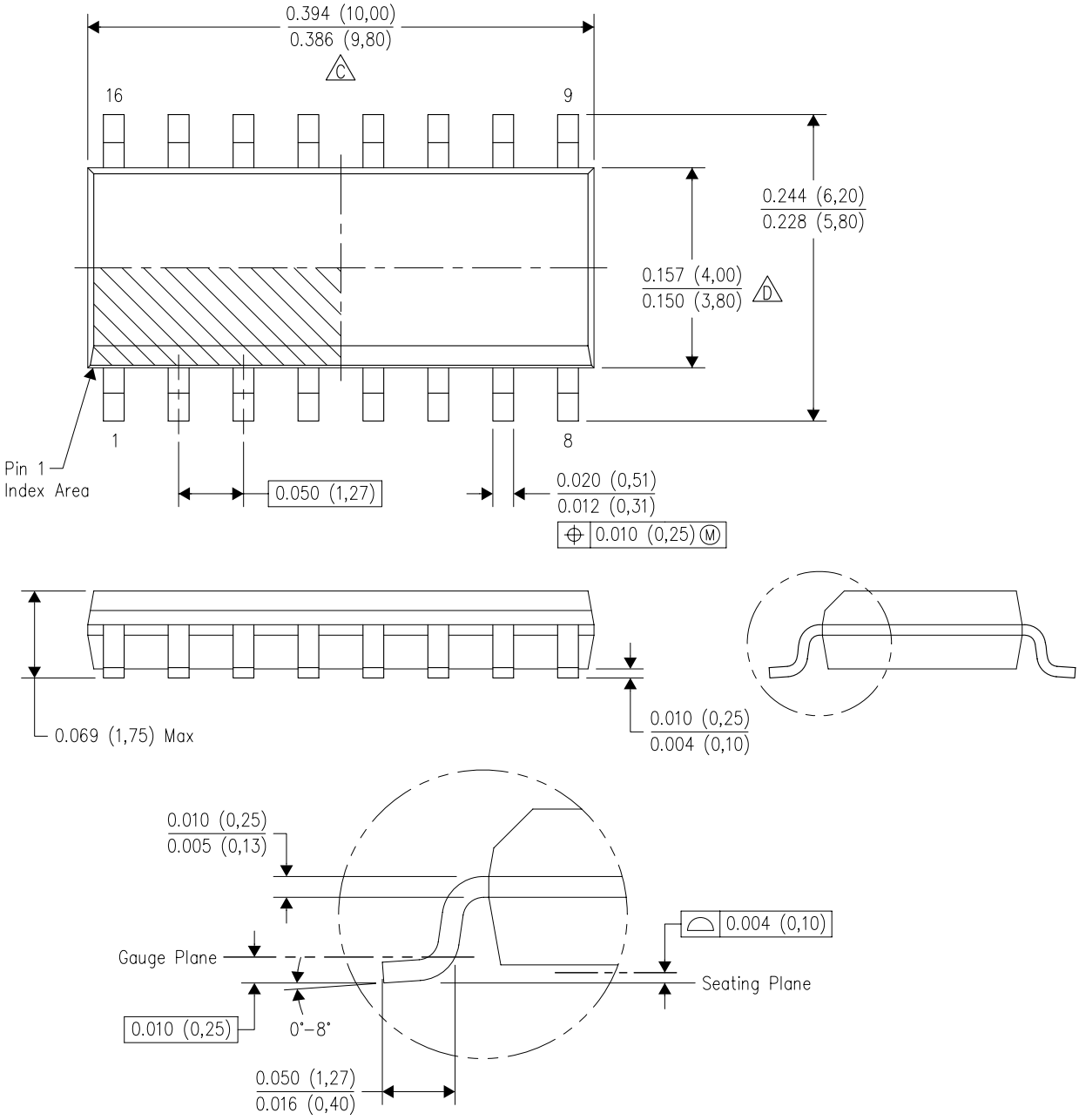

| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |




4040140/D 01/11

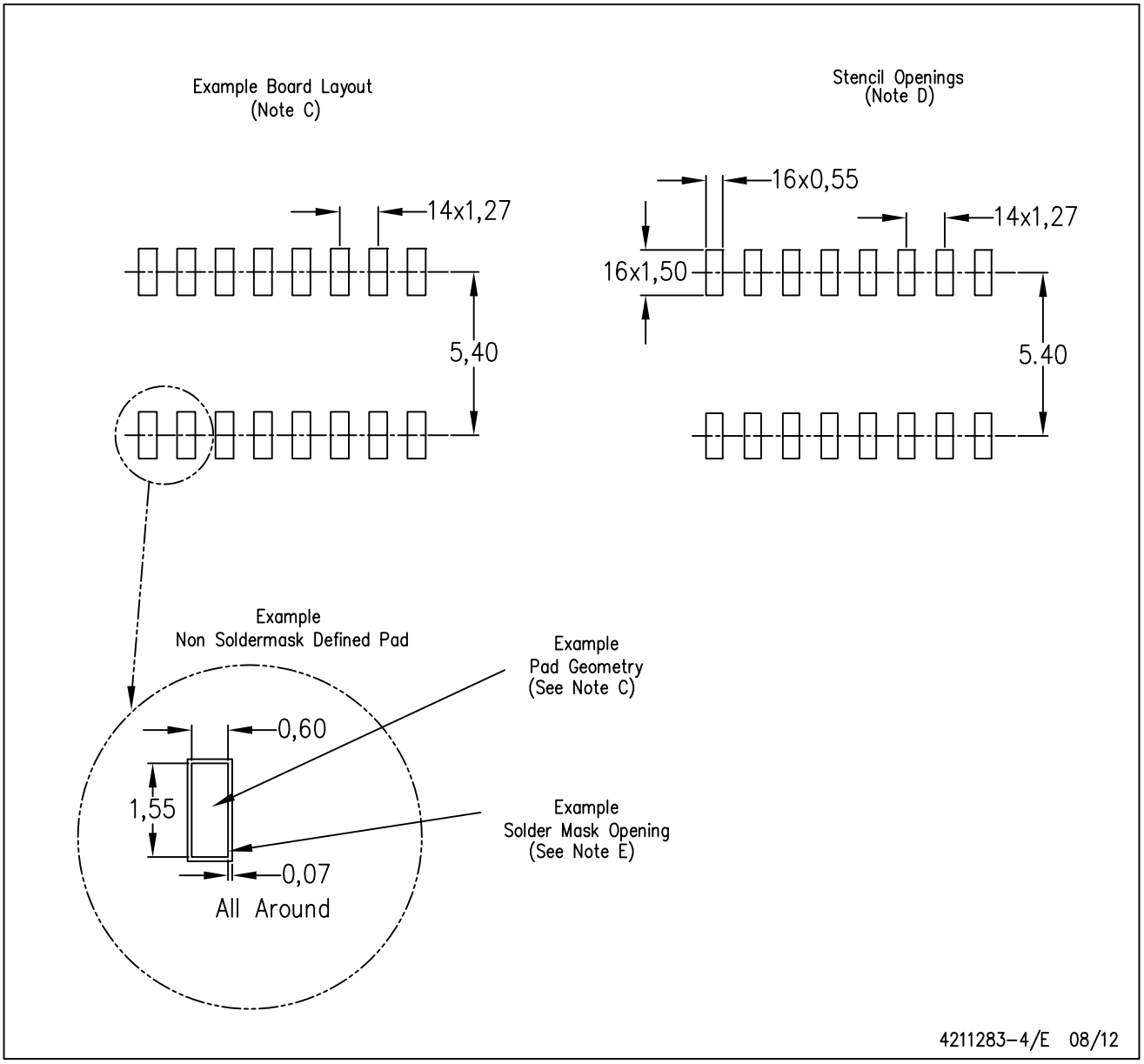
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

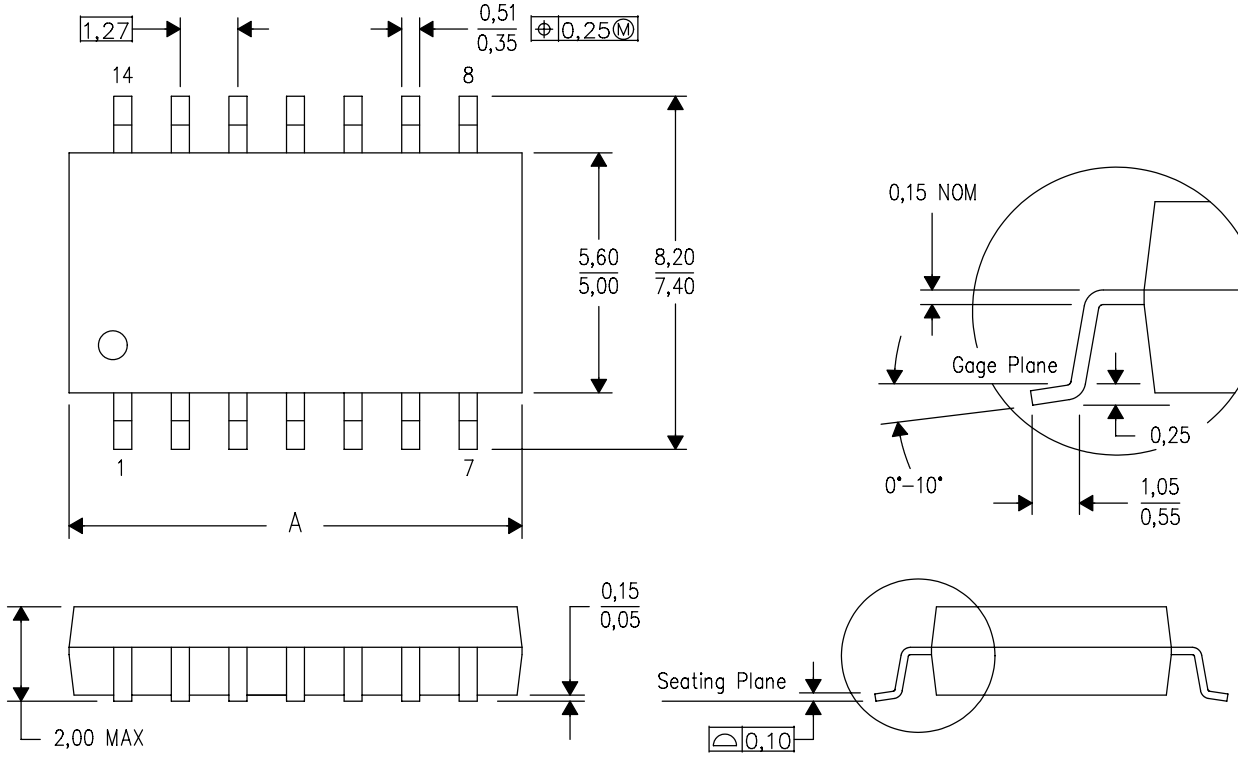



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

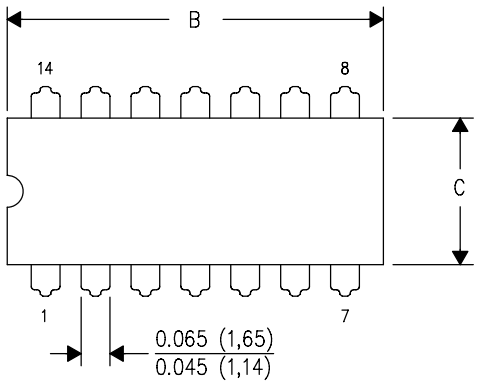
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

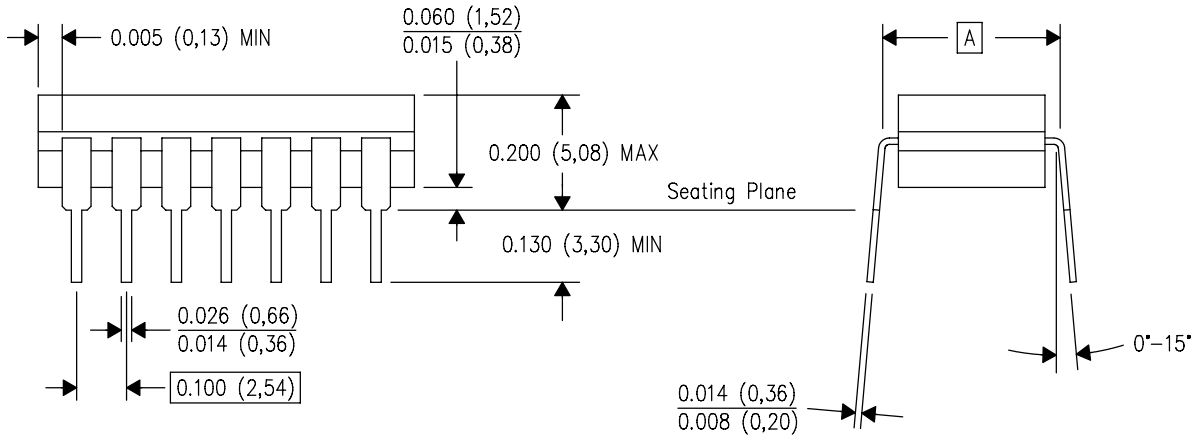
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



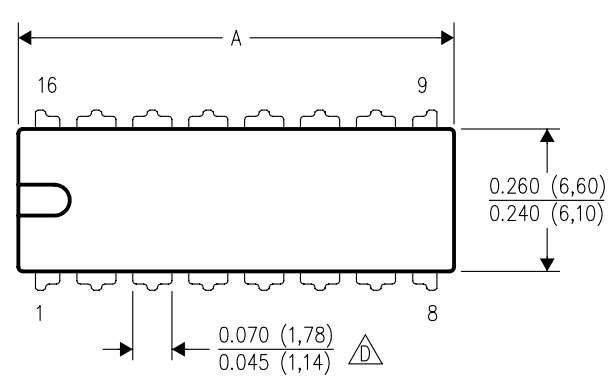

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

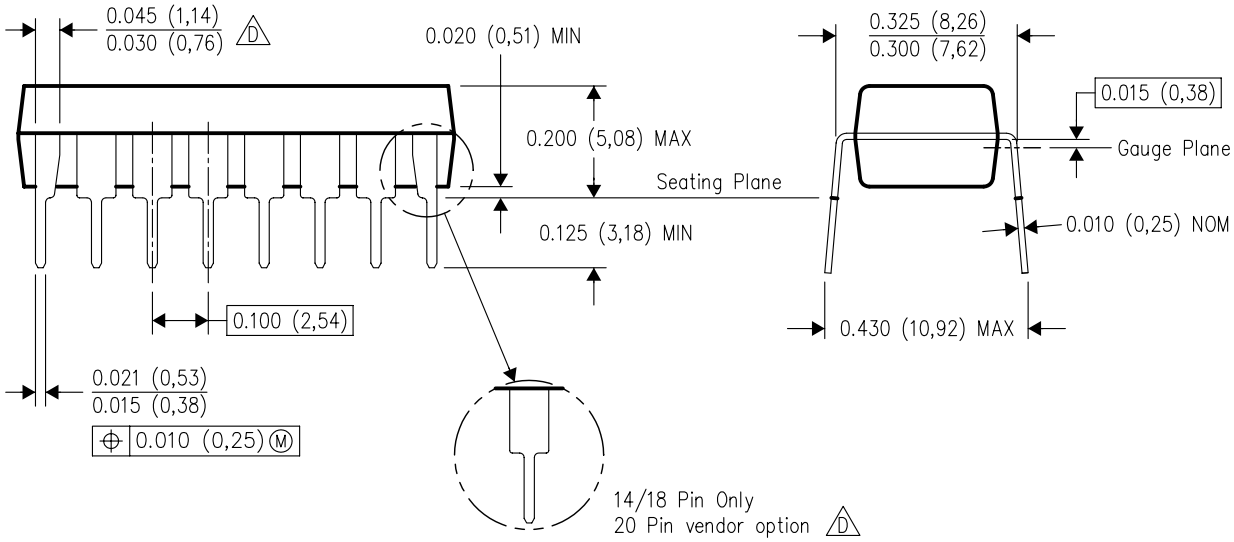
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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