SN74ALVCH16952 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCES011E-JULY 1995-REVISED SEPTEMBER 2004

FEATURES

- Member of the Texas Instruments Widebus™
 Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

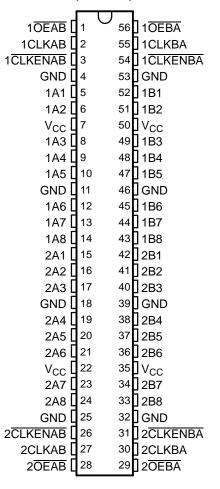
DESCRIPTION

This 16-bit registered transceiver is designed for 1.65-V to 3.6-V $V_{\rm CC}$ operation.

The SN74ALVCH16952 contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. This device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input, provided that the clock-enable (CLKENAB or CLKENBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16952 is characterized for operation from -40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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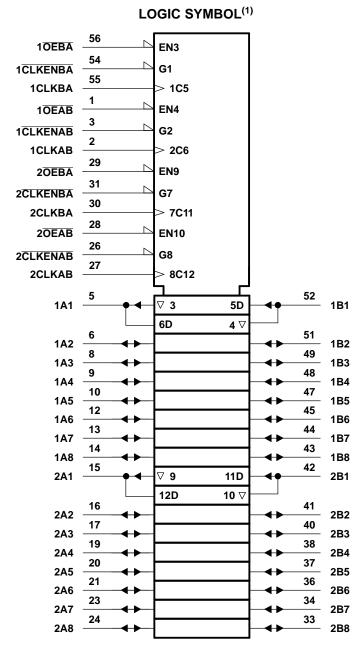


FUNCTION TABLE(1)

	INPUTS							
CLKENAB	CLKAB	OEAB	Α	В				
Н	X	L	Χ	B ₀ ⁽²⁾				
X	L	L	Χ	B ₀ ⁽²⁾ B ₀ ⁽²⁾				
L	1	L	L	L				
L	1	L	Н	Н				
X	Χ	Н	X	Z				

- (1) A-to-B data flow is shown; B-to-A data flow is similar, but uses CLKENBA, CLKBA, and OEBA.
 (2) Level of B before the indicated steady-state input conditions were
- established

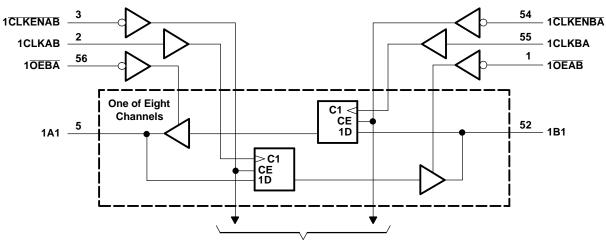




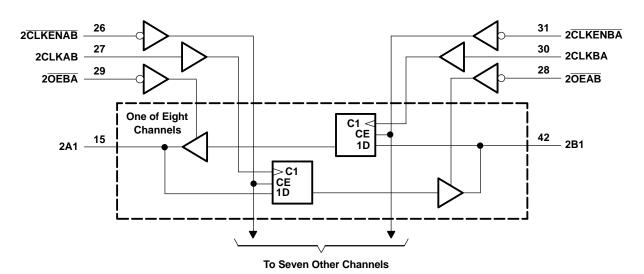
⁽¹⁾ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



LOGIC DIAGRAM (POSITIVE LOGIC)



To Seven Other Channels







ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
W	lanut valtana nana	Except I/O ports ⁽²⁾	-0.5	4.6	V
V _I Input voltage range	I/O ports ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V	
Vo	Output voltage range ⁽²⁾⁽³⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
lok	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through each V _{CC} or	GND		±100	mA
		DGG package		81	
θ_{JA} Package thermal impedance ⁽⁴⁾		DGV package		86	°C/W
		DL package		74	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

	·	·	MIN	MAX	UNIT
V _{CC}	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
	V _{CC} = 2.7 V to 3.6 V		0.8		
VI	Input voltage		0	V _{CC}	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 1.65 V		-4	
	High level output ourrent	$V_{CC} = 2.3 \text{ V}$		-12	mA
I _{OH}	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12	IIIA
		$V_{CC} = 3 V$		-24	
		V _{CC} = 1.65 V		4	
	Lour loval output ourrent	V _{CC} = 2.3 V		12	mA
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12	mA
	V _{CC} = 3 V			24	
Δt/Δν	Input transition rise or fall rate	·		10	ns/V
T _A	Operating free-air temperature		-40	85	°C

⁽¹⁾ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ This value is limited to 4.6 V maximum.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51.

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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾ MAX	UNIT
	$I_{OH} = -100 \mu A$	1.65 V to 3.6 V	V _{CC} - 0.2		
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2		
	$I_{OH} = -6 \text{ mA}$	2.3 V	2		
V _{OH}		2.3 V	1.7		V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2		
		3 V	2.4		
	$I_{OH} = -24 \text{ mA}$	3 V	2		
	$I_{OL} = 100 \mu A$	1.65 V to 3.6 V		0.2	
	I _{OL} = 4 mA	1.65 V		0.45	
V	I _{OL} = 6 mA	2.3 V		0.4	V
V _{OL}	I - 12 mA	2.3 V		0.7	V
	I _{OL} = 12 mA	2.7 V		0.4	
	$I_{OL} = 24 \text{ mA}$	3 V		0.55	
I _I	$V_I = V_{CC}$ or GND	3.6 V		±5	μΑ
	$V_1 = 0.58 \text{ V}$	1.65 V	25		
	V _I = 1.07 V	1.65 V	-25		
	$V_1 = 0.7 \text{ V}$	2.3 V	45		
I _{I(hold)}	V _I = 1.7 V	2.3 V	-45		μΑ
	$V_1 = 0.8 \text{ V}$	3 V	75		
	V _I = 2 V	3 V	-75		
	$V_1 = 0$ to 3.6 $V^{(2)}$	3.6 V		±500	
I _{OZ} ⁽³⁾	$V_O = V_{CC}$ or GND	3.6 V		±10	μΑ
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μΑ
Δl _{CC}	One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V		750	μΑ
C _i Control inputs	$V_I = V_{CC}$ or GND	3.3 V		3.5	pF
C _{io} A or B ports	$V_O = V_{CC}$ or GND	3.3 V		8.5	pF

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

			V _{CC} =	1.8 V	V _{CC} = ± 0.	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} = ± 0.		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency			(1)		150		150		150	MHz	
	Pulse duration	CLKEN high	(1)		3.3		3.3		3.3		nc	
t _w	Pulse duration	CLK high or low	(1)		3.3		3.3		3.3		ns	
	Catua tima	Data before CLK	(1)		1.7		1.9		1.5			
t _{su}	Setup time	CLKEN before CLK	(1)		1.2		1		1		ns	
	Hold time	Data after CLK	(1)		0.6		0.6		0.8			
t _h	Hold time	CLKEN after CLK	(1)		1.1		0.9		1.1		ns	

⁽¹⁾ This information was not available at the time of publication.

⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. (2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to

⁽³⁾ For I/O ports, the parameter $I_{\mbox{\scriptsize OZ}}$ includes the input leakage current.



WITH 3-STATE OUTPUTS
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SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V_{CC} = 2.5 V \pm 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INPUT)	(001701)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			(1)		150		150		150		MHz
t _{pd}	CLK	A or B		(1)	1	4.1		4.6	1	3.9	ns
t _{en}	OEBA or OEAB	A or B		(1)	1	5.4		5.3	1	4.4	ns
t _{dis}	OEBA or OEAB	A or B		(1)	1	5.3		4.4	1.1	4	ns

⁽¹⁾ This information was not available at the time of publication.

OPERATING CHARACTERISTICS

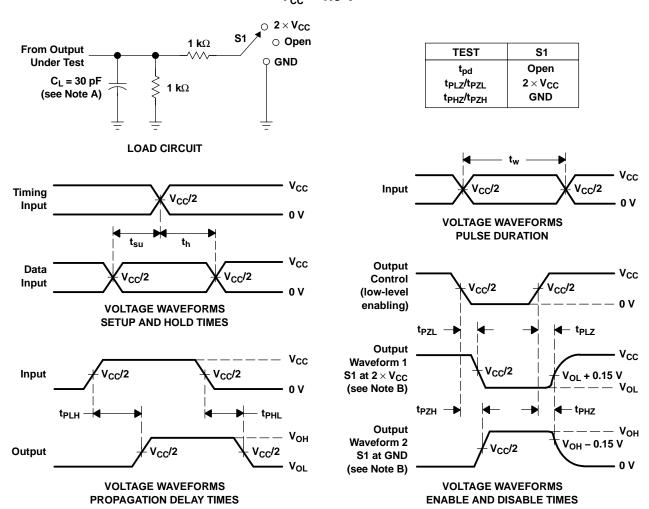
 $T_A = 25^{\circ}C$

	PARAMET	TEST (CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT	
0	Power dissipation	Outputs enabled	C - 0	f = 10 MHz	(1)	53	71	nE
C _{pd}	capacitance	Outputs disabled	$C_L = 0$,	I = IO WINZ	(1)	34	40	рF

⁽¹⁾ This information was not available at the time of publication.



PARAMETER MEASUREMENT INFORMATION $V_{cc} = 1.8 \text{ V}$



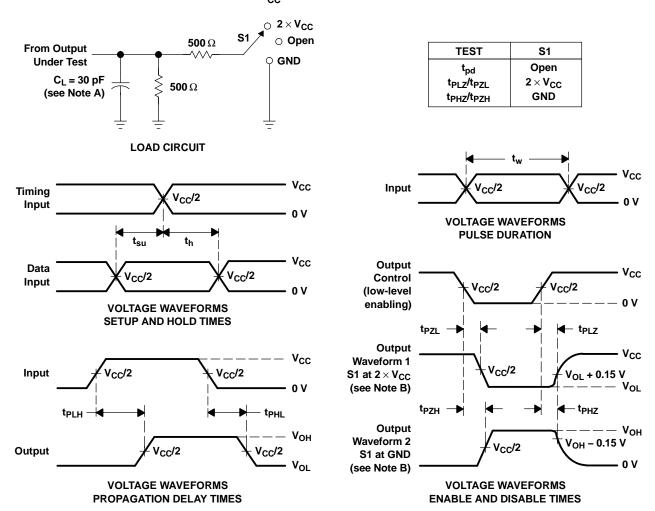
NOTES: A. C₁ includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z $_{O}$ = 50 Ω , t_{f} \leq 2 ns, t_{f} \leq 2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PL7} and t_{PH7} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{\rm CC}$ = 2.5 V \pm 0.2 V



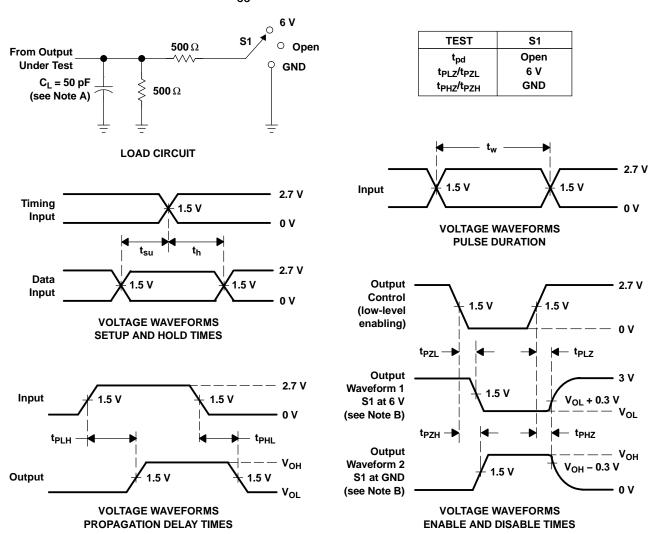
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω , $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PL7} and t_{PH7} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{O} = 50 Ω , $t_{f} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Load Circuit and Voltage Waveforms





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVCH16952DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16952DGVRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16952DGVRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16952DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16952DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16952DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16952DGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16952DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16952DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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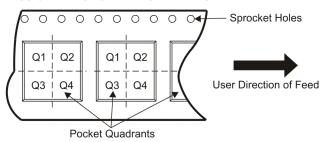
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

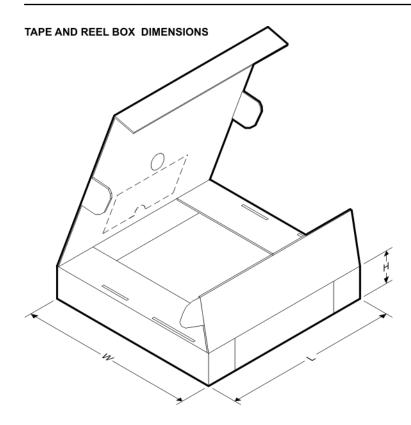
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16952DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ALVCH16952DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74ALVCH16952DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1





*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16952DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74ALVCH16952DGVR	TVSOP	DGV	56	2000	346.0	346.0	41.0
SN74ALVCH16952DLR	SSOP	DL	56	1000	346.0	346.0	49.0

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

DL (R-PDSO-G**)

48 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

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