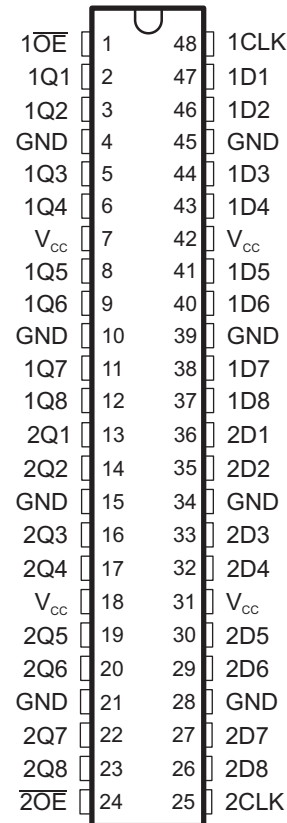


## FEATURES

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Widebus™ Design for 2.5-V and 3.3-V Operation and Low Static Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V  $V_{CC}$ )**
- **Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **High Drive ( $-24/24$  mA at 2.5-V  $V_{CC}$  and  $-32/64$  mA at 3.3-V )**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **High-Impedance State During Power Up and Power Down Prevents Driver Conflict**
- **Uses Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating**
- **Auto3-State Eliminates Bus Current Loading When Output Exceeds  $V_{CC} + 0.5$  V**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection**
  - Exceeds 2000 V Per MIL-STD-883, Method 3015
  - Exceeds 200 V Using Machine Model
  - Exceeds 1000 V Using Charged-Device Model, Robotic Method
- **Flow-Through Architecture Facilitates Printed Circuit Board Layout**
- **Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package**

SN54ALVTH16374...WD PACKAGE  
SN74ALVTH16374...DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The 'ALVTH16374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for 2.5-V or 3.3-V  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the flip-flops store the logic levels set up at the data (D) inputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

**SN54ALVTH16374, SN74ALVTH16374**  
**2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

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**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When  $V_{CC}$  is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

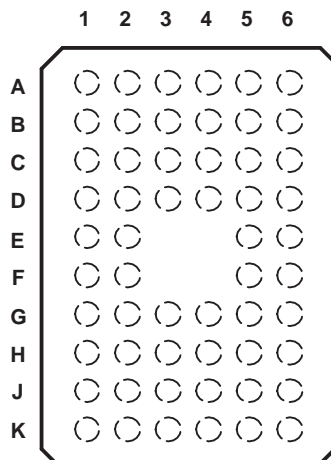
The SN54ALVTH16374 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

The SN74ALVTH16374 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**ORDERING INFORMATION**

$T_A$	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	TSSOP – DGG	Reel of 2000	74ALVTH16374GRE4	
			SN74ALVTH16374GR	
	TVSOP – DGV	Reel of 2000	74ALVTH16374VRE4	
			SN74ALVTH16374VR	
	SSOP – DL	Tube of 25	74ALVTH16374DL	
			SN74ALVTH16374DLG4	
		Reel of 1000	SN74ALVTH16374DLR	
			SN74ALVTH16374DLRG4	

**ZQL PACKAGE  
(TOP VIEW)**



**TERMINAL ASSIGNMENTS<sup>(1)</sup>**

	1	2	3	4	5	6
<b>A</b>	1 $\overline{OE}$	NC	NC	NC	NC	1CLK
<b>B</b>	1Q2	1Q1	GND	GND	1D1	1D2
<b>C</b>	1Q4	1Q3	V <sub>CC</sub>	V <sub>CC</sub>	1D3	1D4
<b>D</b>	1Q6	1Q5	GND	GND	1D5	1D6
<b>E</b>	1Q8	1Q7			1D7	1D8
<b>F</b>	2Q1	2Q2			2D2	2D1
<b>G</b>	2Q3	2Q4	GND	GND	2D4	2D3
<b>H</b>	2Q5	2Q6	V <sub>CC</sub>	V <sub>CC</sub>	2D6	2D5
<b>J</b>	2Q7	2Q8	GND	GND	2D8	2D7
<b>K</b>	2 $\overline{OE}$	NC	NC	NC	NC	2CLK

(1) NC – No internal connection

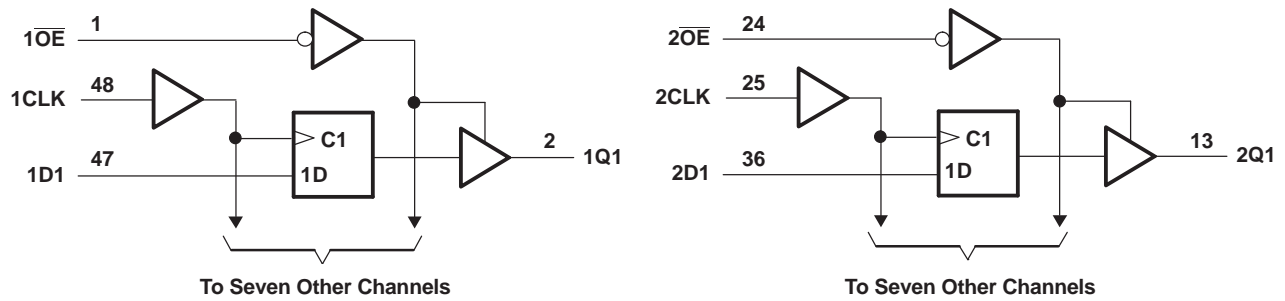
**FUNCTION TABLE  
(each 8-bit section)**

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q <sub>0</sub>
H	X	X	Z

# SN54ALVTH16374, SN74ALVTH16374 2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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## LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DL, and WD packages.

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	7	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V
$V_O$	Voltage range applied to any output in the high state <sup>(2)</sup>	-0.5	7	V
$I_O$	Output current in the low state	SN54ALVTH16374 <sup>(3)</sup>	96	mA
		SN74ALVTH16374	128	
$I_O$	Output current in the high state	SN54ALVTH16374 <sup>(3)</sup>	-48	mA
		SN74ALVTH16374	-64	
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package	89	°C/W
		DGV package	93	
		DL package	94	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) Product preview
- (4) The package thermal impedance is calculated in accordance with JESD 51.

### Recommended Operating Conditions<sup>(1)</sup>

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

		SN54ALVTH16374 <sup>(2)</sup>			SN74ALVTH16374			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage	2.3		2.7	2.3		2.7	V
$V_{IH}$	High-level input voltage	1.7			1.7			V
$V_{IL}$	Low-level input voltage			0.7			0.7	V
$V_I$	Input voltage	0	$V_{CC}$	5.5	0	$V_{CC}$	5.5	V
$I_{OH}$	High-level output current			–6			–8	mA
$I_{OL}$	Low-level output current			6			8	mA
	Low-level output current; current duty cycle $\leq 50\%$ ; $f \geq 1 \text{ kHz}$			18			24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
$T_A$	Operating free-air temperature	–55		125	–40		85	$^{\circ}\text{C}$

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).  
(2) Product preview

### Recommended Operating Conditions<sup>(1)</sup>

$$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$$

		SN54ALVTH16374 <sup>(2)</sup>			SN74ALVTH16374			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage	3		3.6	3		3.6	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$V_I$	Input voltage	0	$V_{CC}$	5.5	0	$V_{CC}$	5.5	V
$I_{OH}$	High-level output current			–24			–32	mA
$I_{OL}$	Low-level output current			24			32	mA
	Low-level output current; current duty cycle $\leq 50\%$ ; $f \geq 1 \text{ kHz}$			48			64	
$\Delta t/\Delta v$	Input transition rise or fall rate			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
$T_A$	Operating free-air temperature	–55		125	–40		85	$^{\circ}\text{C}$

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).  
(2) Product preview

# SN54ALVTH16374, SN74ALVTH16374

## 2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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### Electrical Characteristics

over operating free-air temperature range  $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALVTH16374 <sup>(1)</sup>		SN74ALVTH16374		UNIT	
			MIN	TYP <sup>(2)</sup>	MAX	MIN		TYP <sup>(2)</sup>
$V_{IK}$	$V_{CC} = 2.3 \text{ V}$ ,	$I_I = -18 \text{ mA}$			-1.2		-1.2	V
$V_{OH}$	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ , $I_{OH} = -100 \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$		V	
	$V_{CC} = 2.3 \text{ V}$	$I_{OH} = -6 \text{ mA}$	1.8					
$V_{OL}$		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ , $I_{OL} = 100 \mu\text{A}$		0.2		0.2		V
	$V_{CC} = 2.3 \text{ V}$	$I_{OL} = 6 \text{ mA}$	0.4					
		$I_{OL} = 8 \text{ mA}$			0.4			
		$I_{OL} = 18 \text{ mA}$	0.5					
$I_I$	Control inputs	$V_{CC} = 2.7 \text{ V}$ ,	$V_I = V_{CC}$ or GND	$\pm 1$		$\pm 1$		$\mu\text{A}$
		$V_{CC} = 0$ or $2.7 \text{ V}$ ,	$V_I = 5.5 \text{ V}$	10		10		
	Data inputs	$V_{CC} = 2.7 \text{ V}$	$V_I = 5.5 \text{ V}$	10		10		
			$V_I = V_{CC}$	1		1		
$I_{off}$	$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to $4.5 \text{ V}$			$\pm 100$		$\mu\text{A}$	
$I_{BHL}$ <sup>(3)</sup>	$V_{CC} = 2.3 \text{ V}$ ,	$V_I = 0.7 \text{ V}$	115		115		$\mu\text{A}$	
$I_{BHH}$ <sup>(4)</sup>	$V_{CC} = 2.3 \text{ V}$ ,	$V_I = 1.7 \text{ V}$	-10		-10		$\mu\text{A}$	
$I_{BHLO}$ <sup>(5)</sup>	$V_{CC} = 2.7 \text{ V}$ ,	$V_I = 0$ to $V_{CC}$	300		300		$\mu\text{A}$	
$I_{BHHO}$ <sup>(6)</sup>	$V_{CC} = 2.7 \text{ V}$ ,	$V_I = 0$ to $V_{CC}$	-300		-300		$\mu\text{A}$	
$I_{EX}$ <sup>(7)</sup>	$V_{CC} = 2.3 \text{ V}$ ,	$V_O = 5.5 \text{ V}$	125		125		$\mu\text{A}$	
$I_{OZ(PU/PD)}$ <sup>(8)</sup>	$V_{CC} \leq 1.2 \text{ V}$ , $V_O = 0.5 \text{ V to } V_{CC}$ , $V_I = \text{GND}$ or $V_{CC}$ , $\overline{OE} = \text{don't care}$		$\pm 100$		$\pm 100$		$\mu\text{A}$	
$I_{OZH}$	$V_{CC} = 2.7 \text{ V}$ , $V_O = 2.3 \text{ V}$ ,	$V_I = 0.7 \text{ V}$ or $1.7 \text{ V}$	5		5		$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 2.7 \text{ V}$ , $V_O = 0.5 \text{ V}$ ,	$V_I = 0.7 \text{ V}$ or $1.7 \text{ V}$	-5		-5		$\mu\text{A}$	
$I_{CC}$	$V_{CC} = 2.7 \text{ V}$ ,	Outputs high	0.04	0.1	0.1		mA	
		Outputs low	2.3	4.5	4.5			
		Outputs disabled	0.04	0.1	0.1			
$C_i$	$V_{CC} = 2.5 \text{ V}$ ,	$V_I = 2.5 \text{ V}$ or 0	3.5				pF	
$C_o$	$V_{CC} = 2.5 \text{ V}$ ,	$V_O = 2.5 \text{ V}$ or 0	6				pF	

(1) Product preview

(2) All typical values are at  $V_{CC} = 2.5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(3) The bus-hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max.  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{IL}$  max.

(4) The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

(5) An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.

(6) An external driver must sink at least  $I_{BHHO}$  to switch this node from high to low.

(7) Current into an output in the high state when  $V_O > V_{CC}$

(8) High-impedance state during power up or power down

**Electrical Characteristics**

 over recommended operating free-air temperature range  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALVTH16374 <sup>(1)</sup>		SN74ALVTH16374		UNIT
		MIN	TYP <sup>(2)</sup> MAX	MIN	TYP <sup>(2)</sup> MAX	
$V_{IK}$	$V_{CC} = 3 \text{ V}$ , $I_I = -18 \text{ mA}$		-1.2		-1.2	V
$V_{OH}$	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ , $I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$		$V_{CC} - 0.2$		V
	$V_{CC} = 3 \text{ V}$	2		2		
$V_{OL}$	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ , $I_{OL} = 100 \mu\text{A}$	0.2		0.2		V
	$V_{CC} = 3 \text{ V}$	$I_{OL} = 16 \text{ mA}$		0.4		
		$I_{OL} = 24 \text{ mA}$		0.5		
		$I_{OL} = 32 \text{ mA}$		0.5		
		$I_{OL} = 48 \text{ mA}$		0.55		
$I_{OL} = 64 \text{ mA}$		0.55		0.55		
$I_I$	Control inputs	$V_{CC} = 3.6 \text{ V}$ , $V_I = V_{CC}$ or GND		$\pm 1$		$\mu\text{A}$
		$V_{CC} = 0$ or $3.6 \text{ V}$ , $V_I = 5.5 \text{ V}$		10		
	Data inputs	$V_I = 5.5 \text{ V}$		10		
		$V_{CC} = 3.6 \text{ V}$	$V_I = V_{CC}$		1	
$V_I = 0$			-5		-5	
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to $4.5 \text{ V}$			$\pm 100$		$\mu\text{A}$
$I_{BHL}$ <sup>(3)</sup>	$V_{CC} = 3 \text{ V}$ , $V_I = 0.8 \text{ V}$	75		75		$\mu\text{A}$
$I_{BHH}$ <sup>(4)</sup>	$V_{CC} = 3 \text{ V}$ , $V_I = 2 \text{ V}$	-75		-75		$\mu\text{A}$
$I_{BHLO}$ <sup>(5)</sup>	$V_{CC} = 3.6 \text{ V}$ , $V_I = 0$ to $V_{CC}$	500		500		$\mu\text{A}$
$I_{BHHO}$ <sup>(6)</sup>	$V_{CC} = 3.6 \text{ V}$ , $V_I = 0$ to $V_{CC}$	-500		-500		$\mu\text{A}$
$I_{EX}$ <sup>(7)</sup>	$V_{CC} = 3 \text{ V}$ , $V_O = 5.5 \text{ V}$	125		125		$\mu\text{A}$
$I_{OZ(PU/PD)}$ <sup>(8)</sup>	$V_{CC} \leq 1.2 \text{ V}$ , $V_O = 0.5 \text{ V to } V_{CC}$ , $V_I = \text{GND or } V_{CC}$ , $\overline{OE} = \text{don't care}$	$\pm 100$		$\pm 100$		$\mu\text{A}$
$I_{OZH}$	$V_{CC} = 3.6 \text{ V}$ , $V_O = 3 \text{ V}$ , $V_I = 0.8 \text{ V or } 27 \text{ V}$	5		5		$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 3.6 \text{ V}$ , $V_O = 0.5 \text{ V}$ , $V_I = 0.8 \text{ V or } 2 \text{ V}$	-5		-5		$\mu\text{A}$
$I_{CC}$	$V_{CC} = 3.6 \text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND	Outputs high		0.07	0.1	mA
		Outputs low		3.2	5	
		Outputs disabled		0.07	0.1	
$\Delta I_{CC}$ <sup>(9)</sup>	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ , One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC}$ or GND	0.4		0.4		mA
$C_i$	$V_{CC} = 3.3 \text{ V}$ , $V_I = 3.3 \text{ V or } 0$	3.5		3.5		pF
$C_o$	$V_{CC} = 3.3 \text{ V}$ , $V_O = 3.3 \text{ V or } 0$	6		6		pF

(1) Product preview

 (2) All typical values are at  $V_{CC} = 2.5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

 (3) The bus-hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max.  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{IL}$  max.

 (4) The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

 (5) An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.

 (6) An external driver must sink at least  $I_{BHHO}$  to switch this node from high to low.

 (7) Current into an output in the high state when  $V_O > V_{CC}$ 

(8) High-impedance state during power up or power down

 (9) This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

# SN54ALVTH16374, SN74ALVTH16374

## 2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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### Timing Requirements

over recommended operating free-air temperature range  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see [Figure 1](#))

		SN54ALVTH16374 <sup>(1)</sup>		SN74ALVTH16374		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	150		150		MHz
$t_w$	Pulse duration, CLK high or low	1.5		1.5		ns
$t_{\text{su}}$	Setup time, data before CLK $\uparrow$	Data high	1.1	1		ns
		Data low	1.4	1.3		
$t_h$	Hold time, data after CLK $\uparrow$	Data high	0.6	0.5		ns
		Data low	0.9	0.8		

(1) Product preview

### Timing Requirements

over recommended operating free-air temperature range  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see [Figure 2](#))

		SN54ALVTH16374 <sup>(1)</sup>		SN74ALVTH16374		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	25		250		MHz
$t_w$	Pulse duration, CLK high or low	1.5		1.5		ns
$t_{\text{su}}$	Setup time, data before CLK $\uparrow$	Data high	1.1	1		ns
		Data low	1.6	1.5		
$t_h$	Hold time, data after CLK $\uparrow$	Data high	0.6	0.5		ns
		Data low	1.1	1		

(1) Product preview



### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 30$  pF,  $V_{CC} = 2.5$  V  $\pm$  0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16374 <sup>(1)</sup>		SN74ALVTH16374		UNIT
			MIN	MAX	MIN	MAX	
$f_{max}$			150		150		MHz
$t_{PLH}$	CLK	Q	1.4	3.9	1.5	3.8	ns
$t_{PHL}$			1.4	3.9	1.5	3.8	
$t_{PZH}$	$\overline{OE}$	Q	1	4.2	1	4.1	ns
$t_{PZL}$			1	3.8	1	3.7	
$t_{PHZ}$	$\overline{OE}$	Q	1.7	4.3	1.8	4.2	ns
$t_{PLZ}$			1	3.5	1	3.4	

(1) Product preview

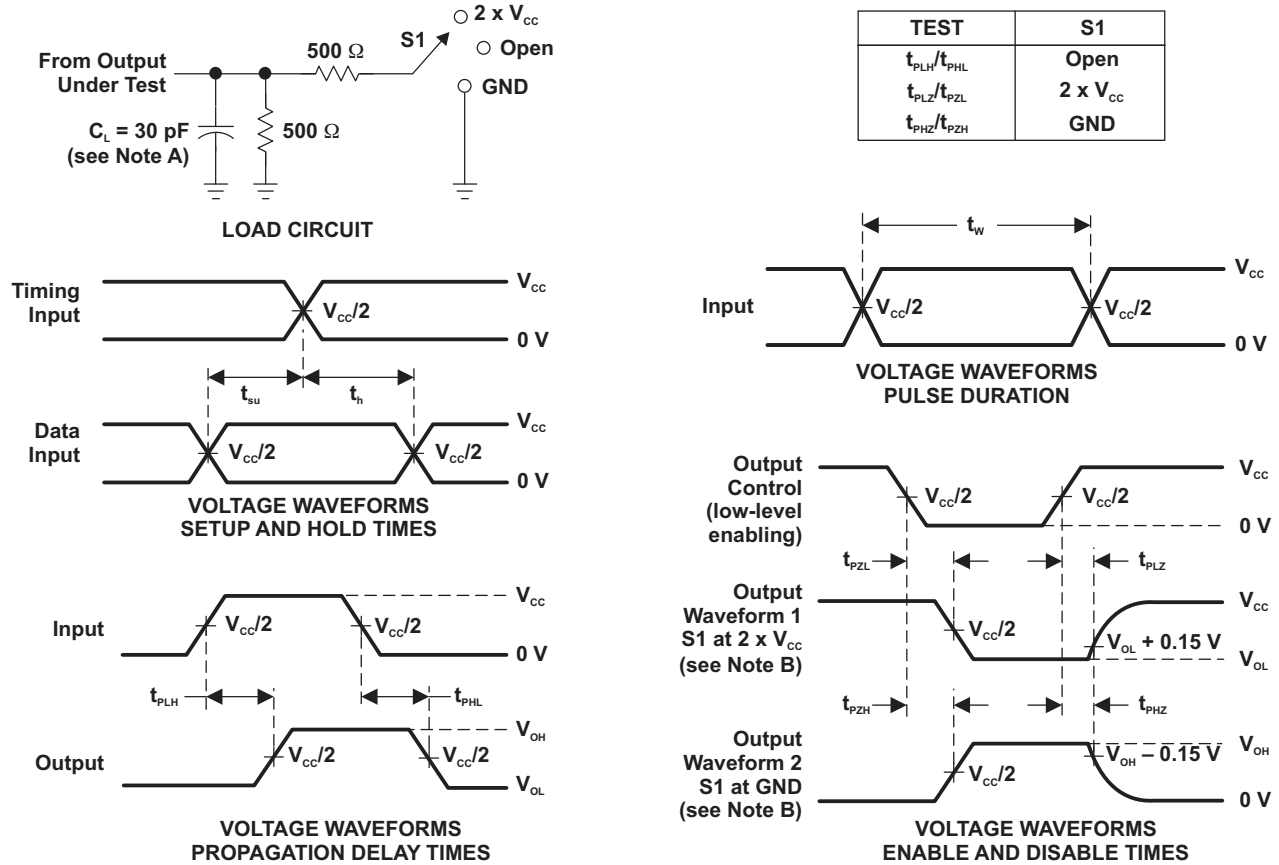
### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50$  pF,  $V_{CC} = 3.3$  V  $\pm$  0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16374 <sup>(1)</sup>		SN74ALVTH16374		UNIT
			MIN	MAX	MIN	MAX	
$f_{max}$			250		250		MHz
$t_{PLH}$	CLK	Q	1	3.4	1	3.2	ns
$t_{PHL}$			1	3.3	1	3.2	
$t_{PZH}$	$\overline{OE}$	Q	1	3.9	1	3.8	ns
$t_{PZL}$			1	3.4	1	3.3	
$t_{PHZ}$	$\overline{OE}$	Q	1	4.7	1	4.6	ns
$t_{PLZ}$			1	4.4	1	4.2	

(1) Product preview

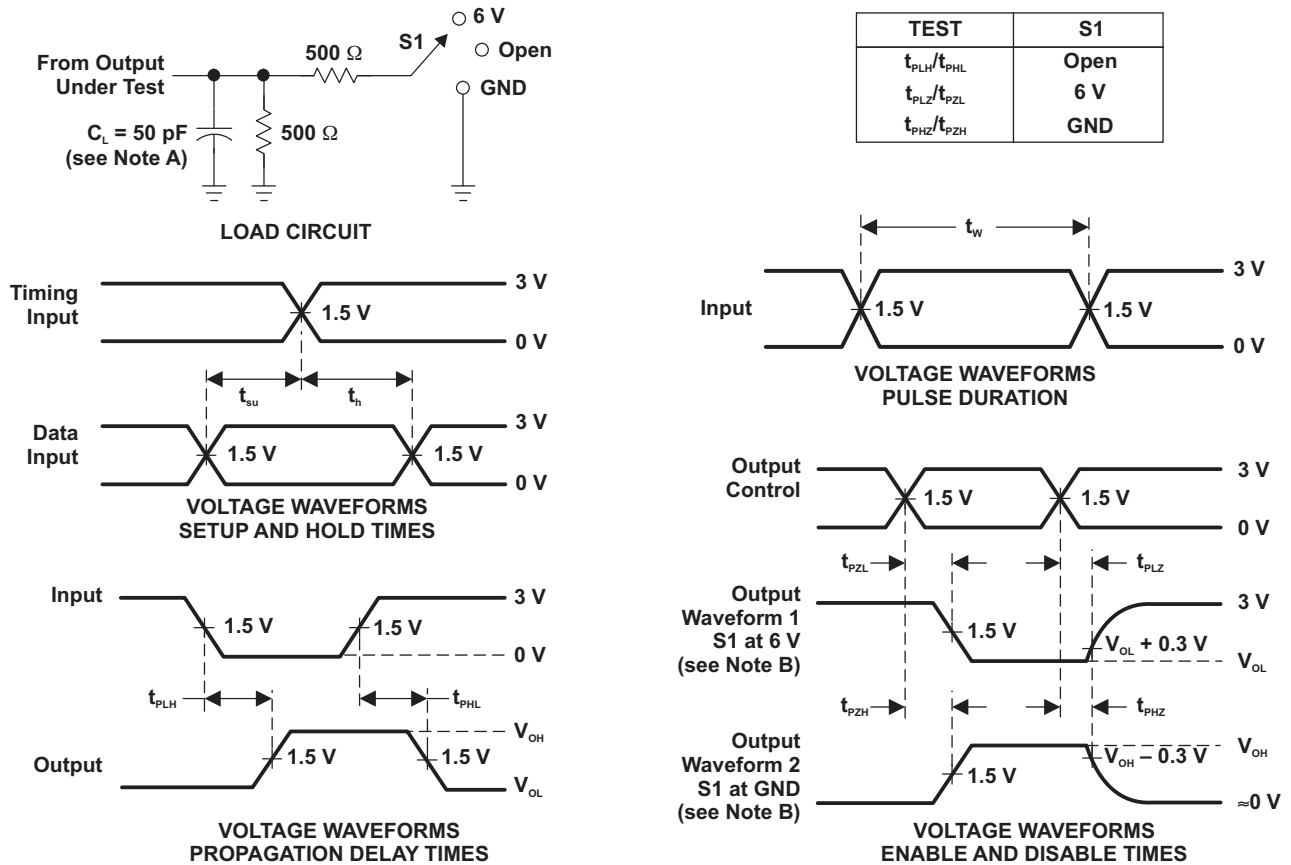
PARAMETER MEASUREMENT INFORMATION  
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_o = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_o = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74ALVTH16374ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	VT374	<a href="#">Samples</a>
SN74ALVTH16374DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVTH16374	<a href="#">Samples</a>
SN74ALVTH16374DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVTH16374	<a href="#">Samples</a>
SN74ALVTH16374GR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVTH16374	<a href="#">Samples</a>
SN74ALVTH16374VR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VT374	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ALVTH16374ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
SN74ALVTH16374DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74ALVTH16374GR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ALVTH16374VR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



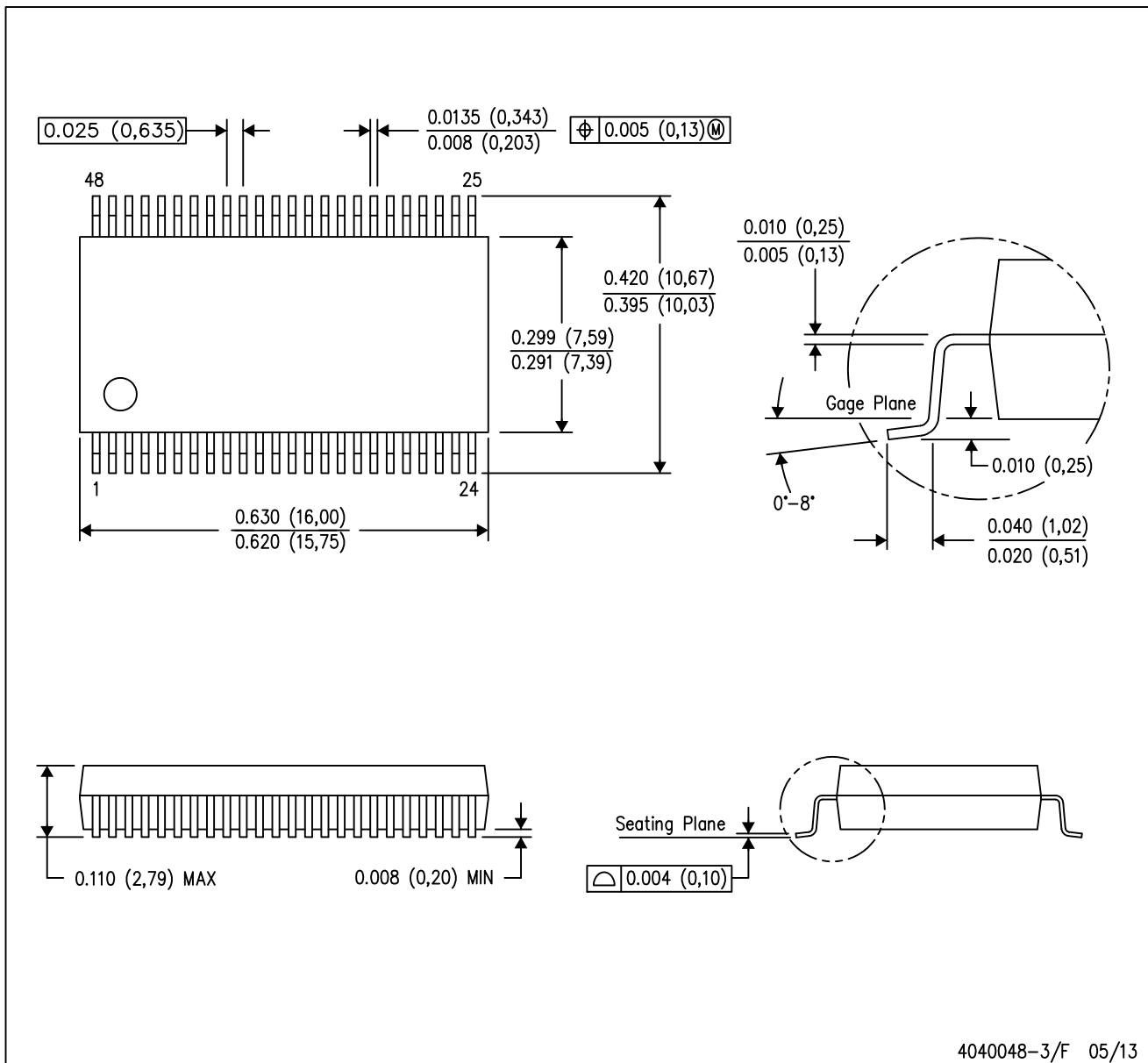
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ALVTH16374ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	336.6	336.6	28.6
SN74ALVTH16374DLR	SSOP	DL	48	1000	367.0	367.0	55.0
SN74ALVTH16374GR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ALVTH16374VR	TVSOP	DGV	48	2000	367.0	367.0	38.0

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

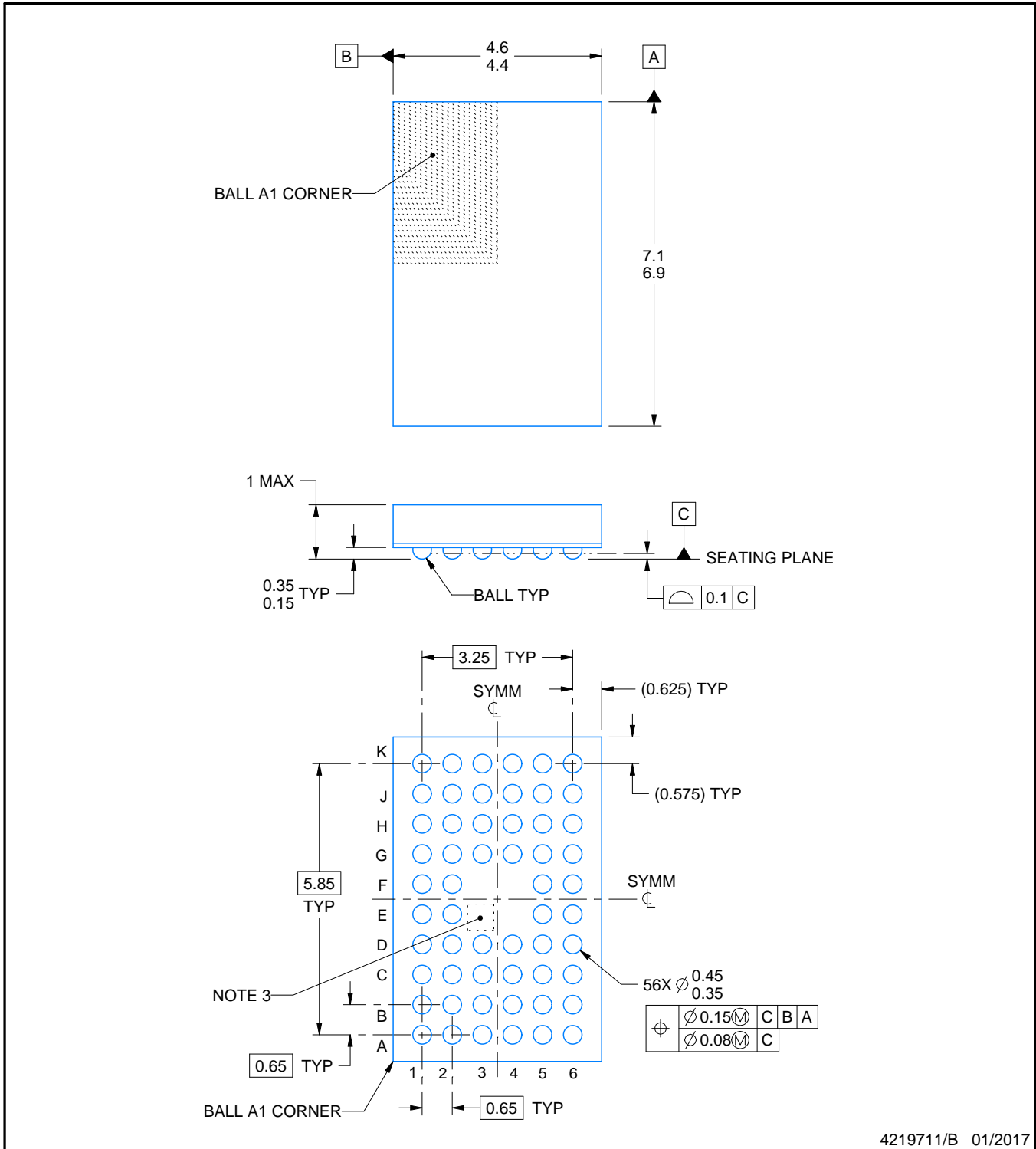
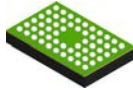
DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



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NOTES:

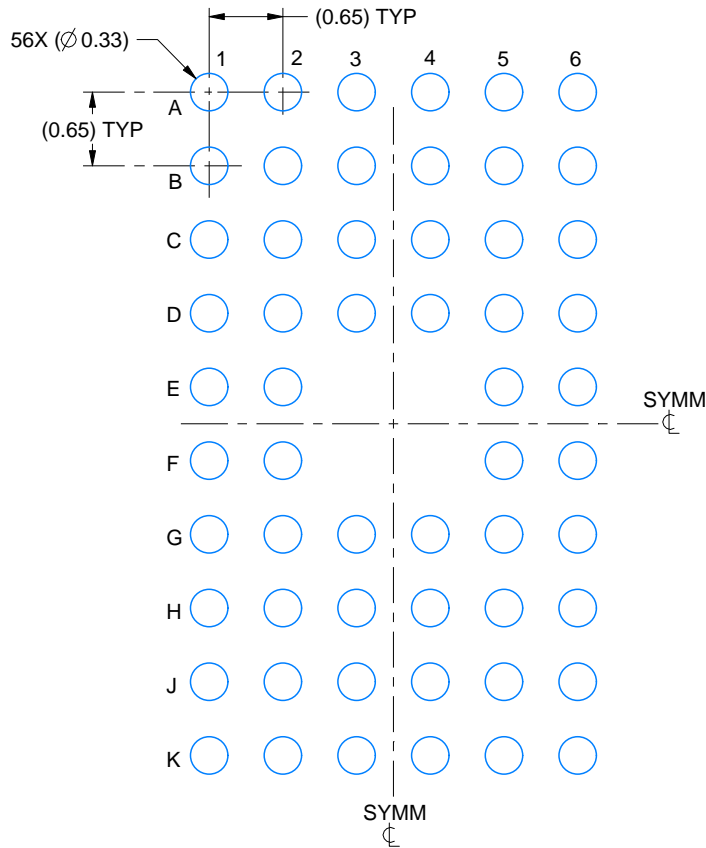
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. No metal in this area, indicates orientation.

# EXAMPLE BOARD LAYOUT

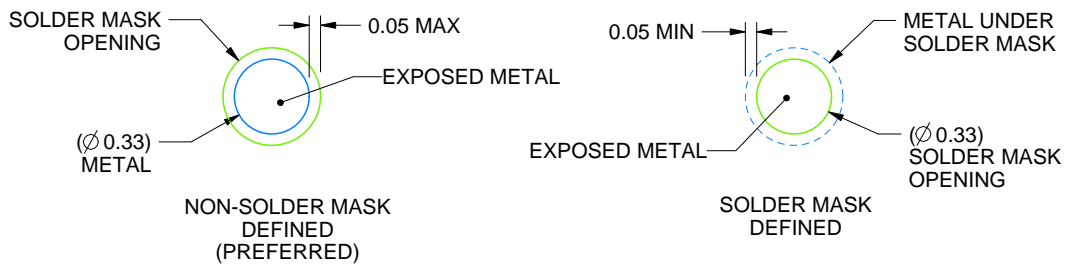
ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

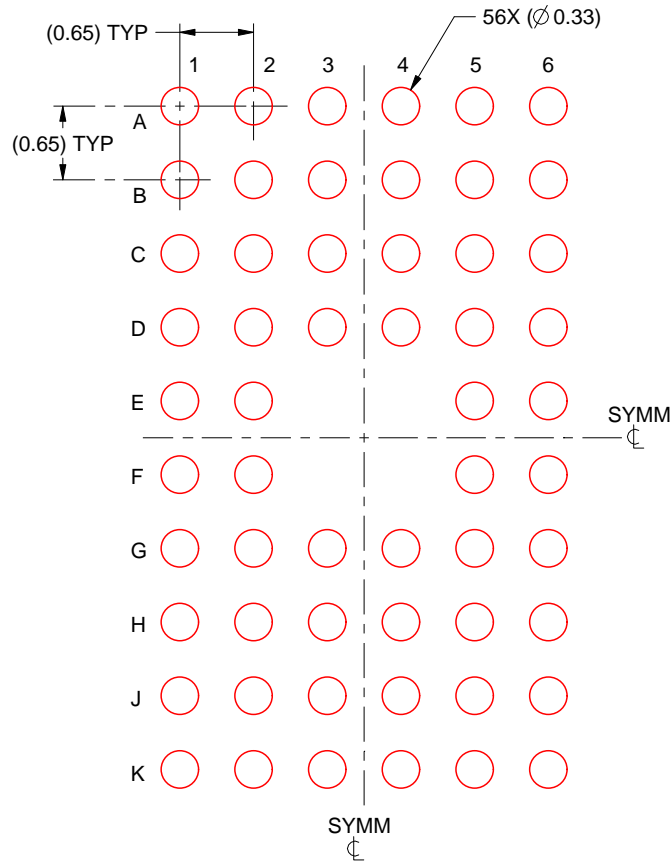
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 ([www.ti.com/lit/spraa99](http://www.ti.com/lit/spraa99)).

# EXAMPLE STENCIL DESIGN

ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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