8-INPUT POSITIVE-NAND GATES

Check for Samples: SN54ALS30A, SN54AS30, SN74ALS30A, SN74AS30

FEATURES

- 8-Input Positive-NAND Gates
- Available in J, DW, N, and FK Packages

DESCRIPTION

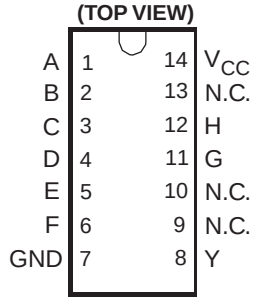
These devices contain an 8-input positive-NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H}$$

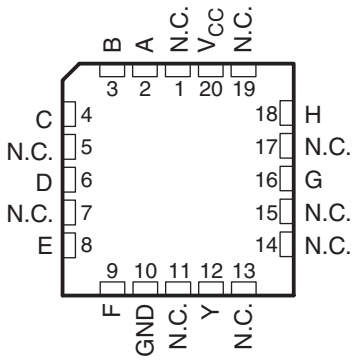
or

$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G}$$

SN54ALS30A, SN54AS30 . . . J PACKAGE
SN74ALS30A, SN74AS30 . . . DW OR N PACKAGE
SN74AS30 . . . DB PACKAGE
(TOP VIEW)



SN54ALS30A, SN54AS30 . . . FK PACKAGE
(TOP VIEW)



N.C. – No internal connection

ORDERING INFORMATION

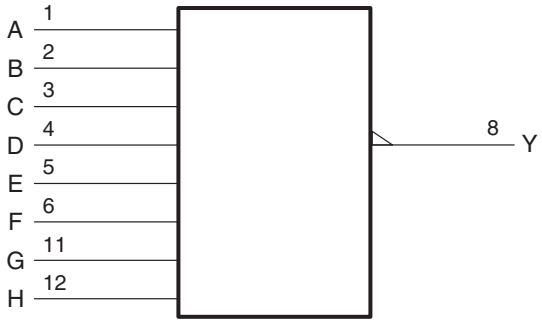
T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS30AN	SN74ALS30AN
			SN74AS30N	SN74AS30N
	SOIC – D	Tube	SN74AS30AD	ALS30A
		Tape and reel	SN74ALS30ADR	
		Tube	SN74AS30D	AS30
		Tape and reel	SN74AS30DR	
	SSOP – DB	Tape and reel	SN74AS30DBR	AS30
–55°C to 125°C	CDIP – J	Tube	SNJ54ALS30AJ	SNJ54ALS30AJ
			SNJ54AS30J	SNJ54AS30J
	LCCC –FK	Tube	SNJ54ALS30AFK	SNJ54ALS30AFK
			SNJ54AS30FK	SNJ54AS30FK

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Table 1. FUNCTION TABLE

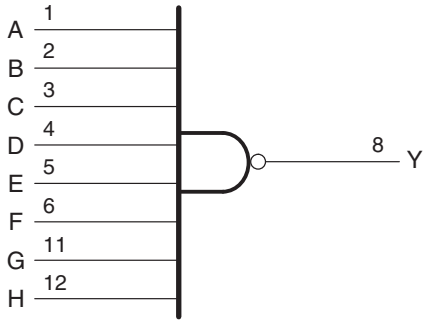
INPUTS A–H	OUTPUT Y
All inputs H	L
One or more inputs L	H

LOGIC SYMBOL



A. This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin number shown are for the D, DB, J, and N packages.

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin number shown are for the D, DB, J, and N packages.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range		–0.5	7	V
θ_{JA}	Package thermal impedance(2)	D package		86	°C/W
		DB package		96	
		N package		80	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8 (1)	V
					0.7 (2)	
I_{OH}	High-level output current	'ALS30A			–0.4	mA
		'AS30			–2	
I_{OL}	Low-level output current	SN54ALS30A			4	mA
		SN74ALS30A			8	
		'AS30			20	
T_A	Operating free-air temperature	SN54ALS30A, SN54AS30	–55		125	°C
		SN74ALS30A, SN74AS30	0		70	

(1) Applies to the 'AS30 and SN74ALS30A across the full operating temperature range, and SN54ALS30A over the temperature range of –55°C to 7°°C.
(2) Applies to the SN54ALS30A over the temperature range of 70°C to 125°C.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP (1)	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA	'ALS30A			–1.5	V
			'AS30				
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	'ALS30A	V_{CC} – 2			V
		I_{OH} = –2 mA	'AS30	V_{CC} – 2			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 4 mA	'ALS30A		0.25	0.4	V
		I_{OL} = 8 mA	SN74ALS30A		0.35	0.5	
		I_{OL} = 20 mA	'AS30		0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V	'ALS30A			–0.1	mA
			'AS30			–0.5	
I_O (2)	V_{CC} = 5.5 V,	V_O = 2.25 V	SN54ALS30A	–20		–112	mA
			SN74ALS30A	–30		–112	
			'AS30	–30		–112	
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V	'ALS30A		0.22	0.36	mA
			'AS30		0.9	1.5	
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V	'ALS30A		0.54	0.9	mA
			'AS30		3	4.9	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted (see Figure 1)

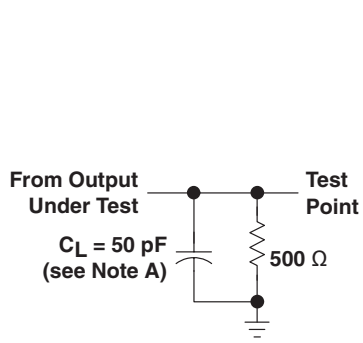
PARAMETER	FROM (INPUT)	TO (OUTPUT)		MIN	MAX	UNIT
t_{PLH}	A, B, C, D, E, F, G, or H	Y	SN54ALS30A	3	15	ns
			SN74ALS30A	3	10	
			SN54AS30	1	5.5	
			SN74AS30	1	5	

SWITCHING CHARACTERISTICS (continued)

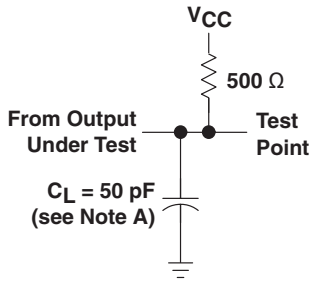
over recommended operating conditions (unless otherwise noted (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		MIN	MAX	UNIT
t_{PHL}	A, B, C, D, E, F, G, or H	Y	SN54ALS30A	3	15	ns
			SN74ALS30A	3	12	
			SN54AS30	1	5	
			SN74AS30	1	4.5	

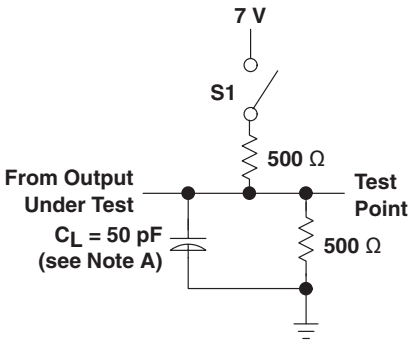
PARAMETER MEASUREMENT INFORMATION



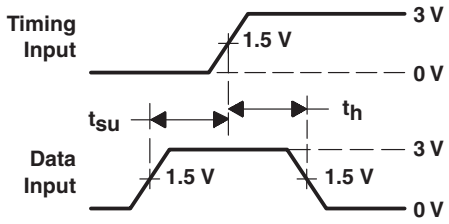
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



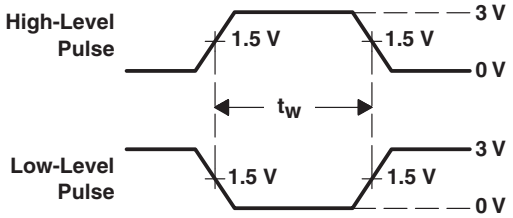
LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



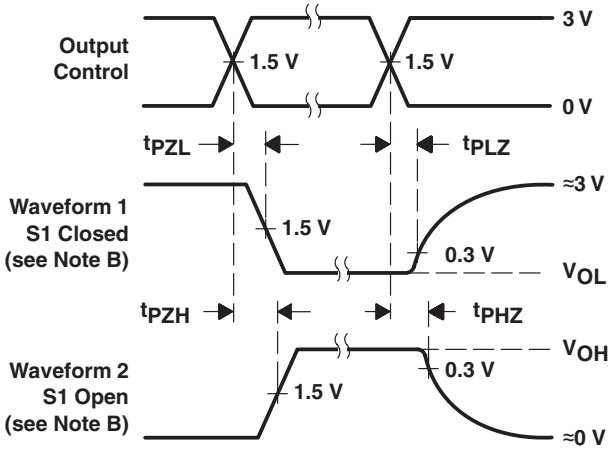
LOAD CIRCUIT FOR 3-STATE OUTPUTS



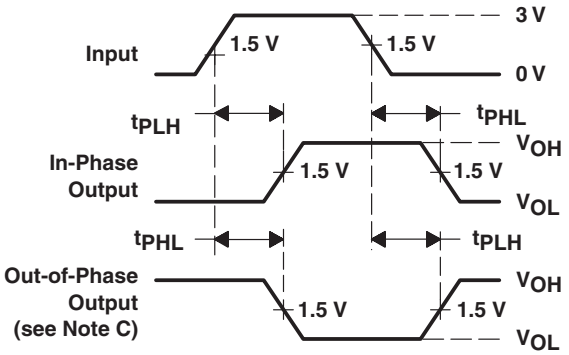
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. When measuring propagation delay items of 3-state outputs, switch S1 is open.

D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.

E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

REVISION HISTORY

Changes from Original (April 2009) to Revision E	Page
• Updated ORDERING INFORMATION table.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-86837012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-86837012A SNJ54ALS30AFK	Samples
5962-8683701DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8683701DA SNJ54ALS30AW	Samples
5962-9755801QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9755801QCA SNJ54AS30J	Samples
JM38510/37004B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/37004B2A	Samples
JM38510/37004BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/37004BCA	Samples
M38510/37004B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/37004B2A	Samples
M38510/37004BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/37004BCA	Samples
SN54ALS30AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54ALS30AJ	Samples
SN74ALS30AD	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS30A	
SN74ALS30ADR	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS30A	
SN74ALS30ADRE4	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS30A	
SN74ALS30AN	NRND	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS30AN	
SN74AS30D	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS30	
SN74AS30DR	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS30	
SN74AS30N	NRND	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS30N	
SNJ54ALS30AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-86837012A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54ALS 30AFK	
SNJ54ALS30AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54ALS30AJ	Samples
SNJ54ALS30AW	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8683701DA SNJ54ALS30AW	Samples
SNJ54AS30J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9755801QC A SNJ54AS30J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ALS30A, SN54AS30, SN74ALS30A, SN74AS30 :

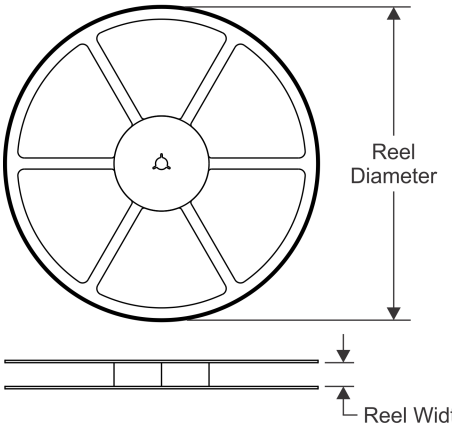
- Catalog: SN74ALS30A, SN74AS30
- Military: SN54ALS30A, SN54AS30

NOTE: Qualified Version Definitions:

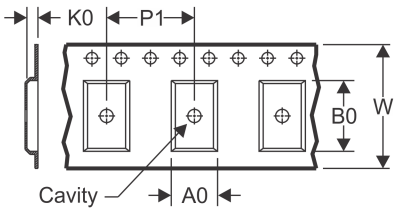
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

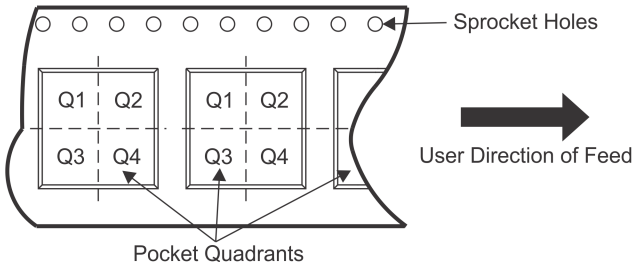


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

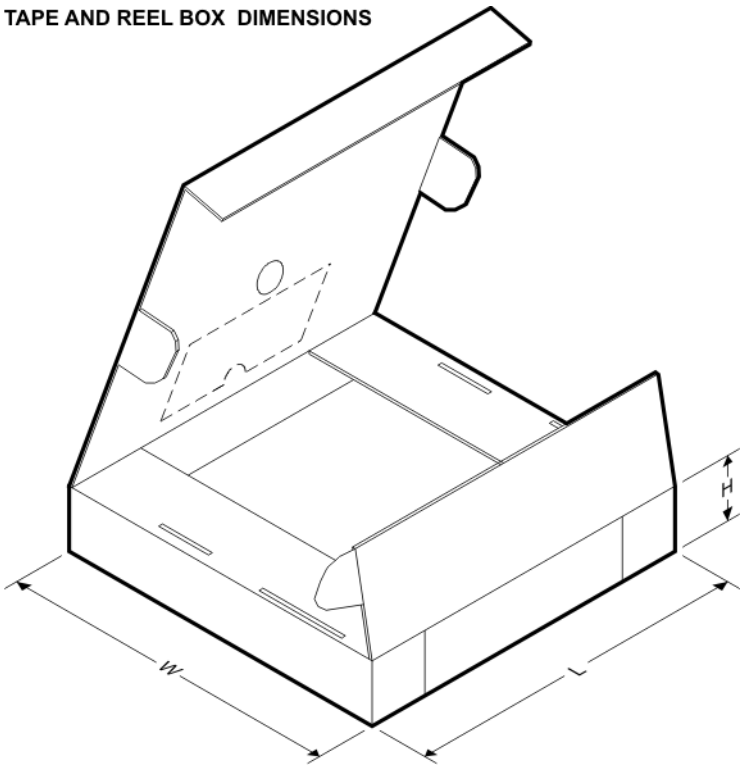
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS30ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AS30DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

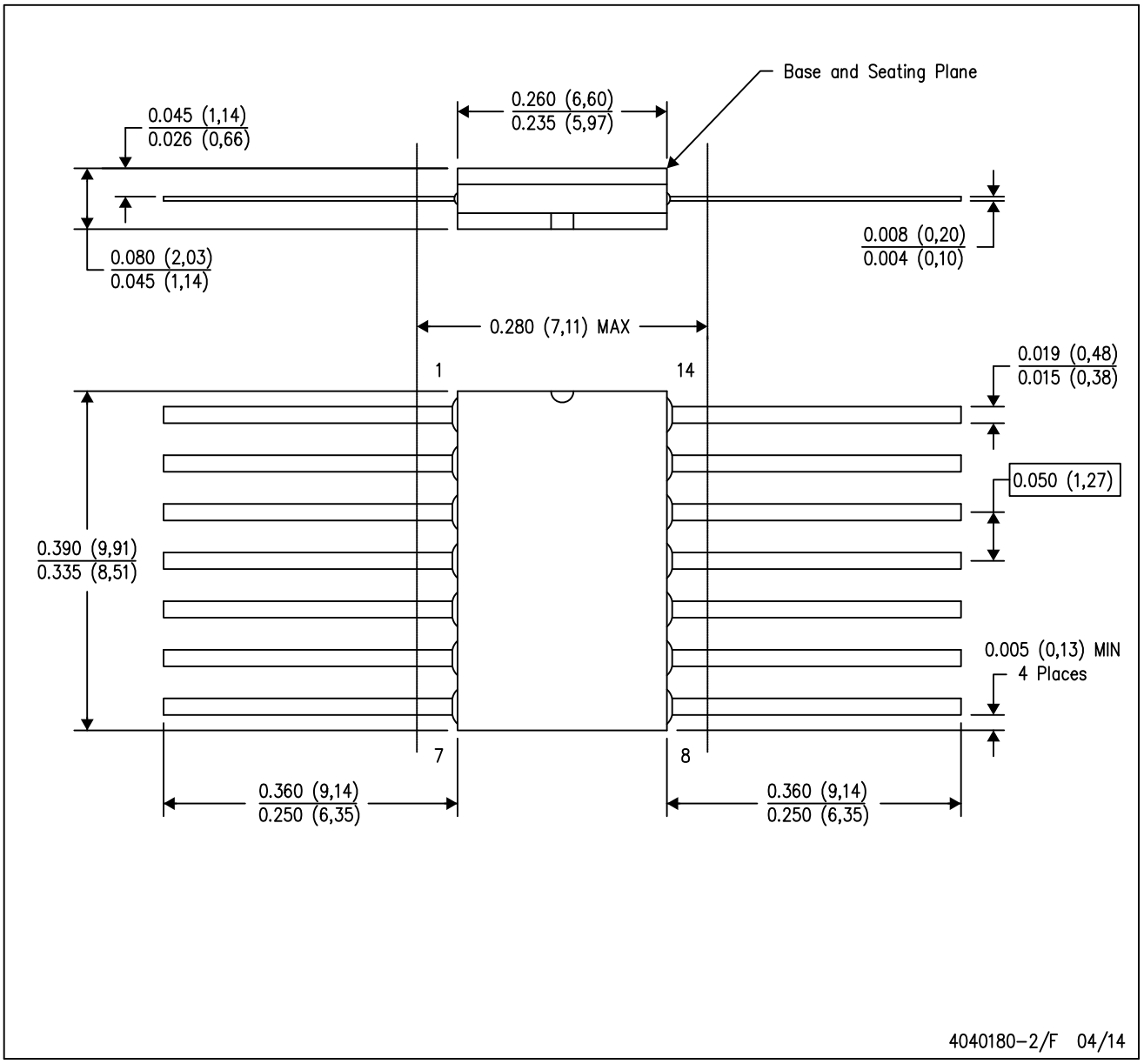
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS30ADR	SOIC	D	14	2500	367.0	367.0	38.0
SN74AS30DR	SOIC	D	14	2500	367.0	367.0	38.0

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

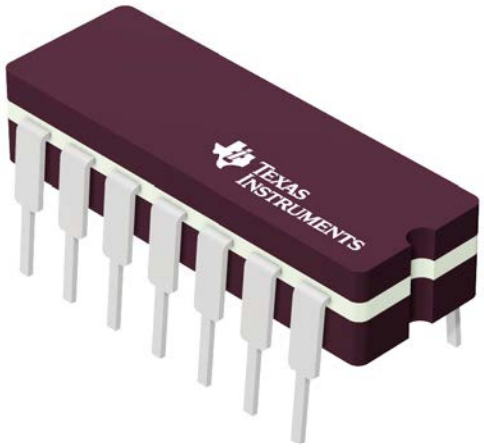


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

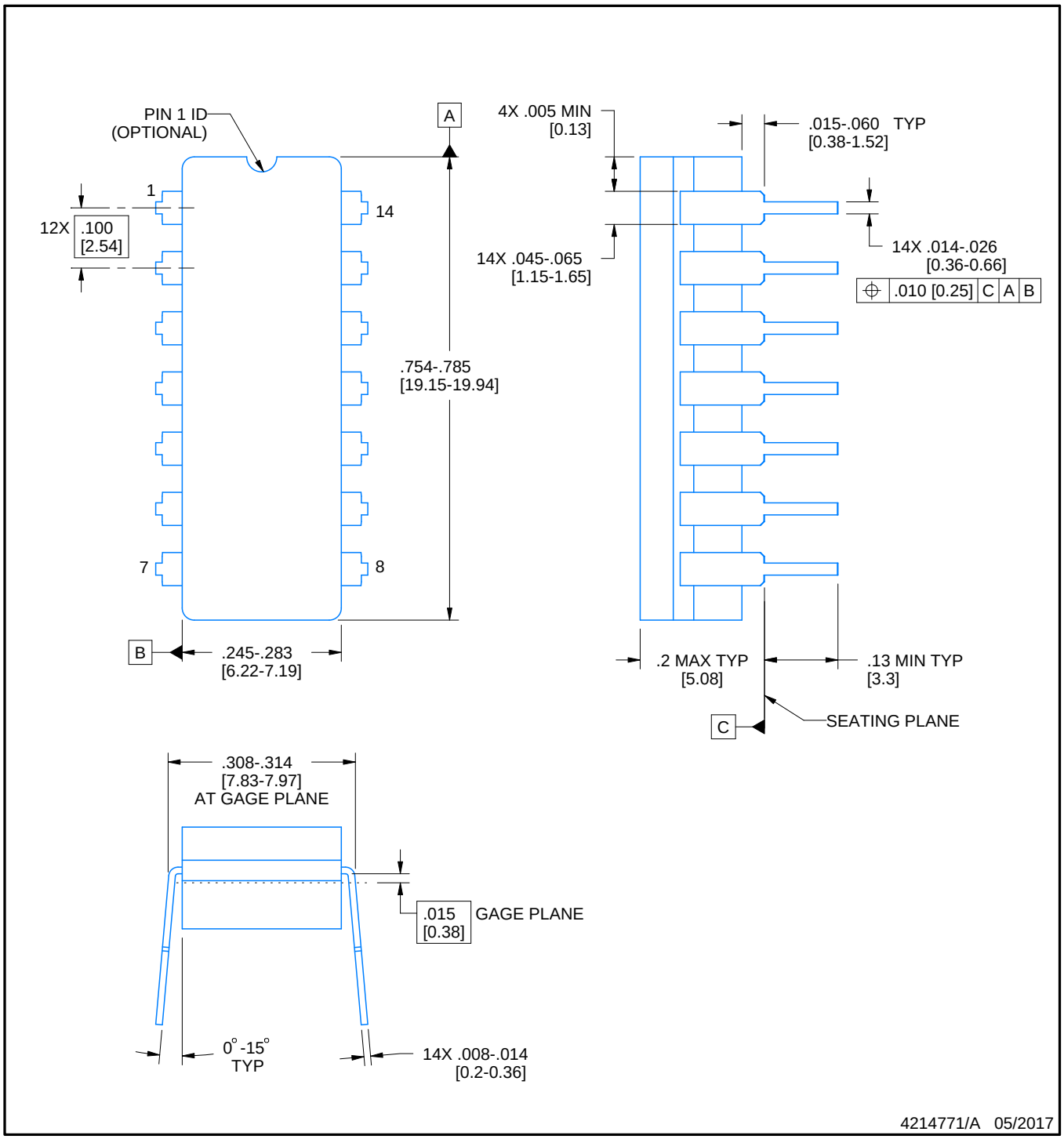
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

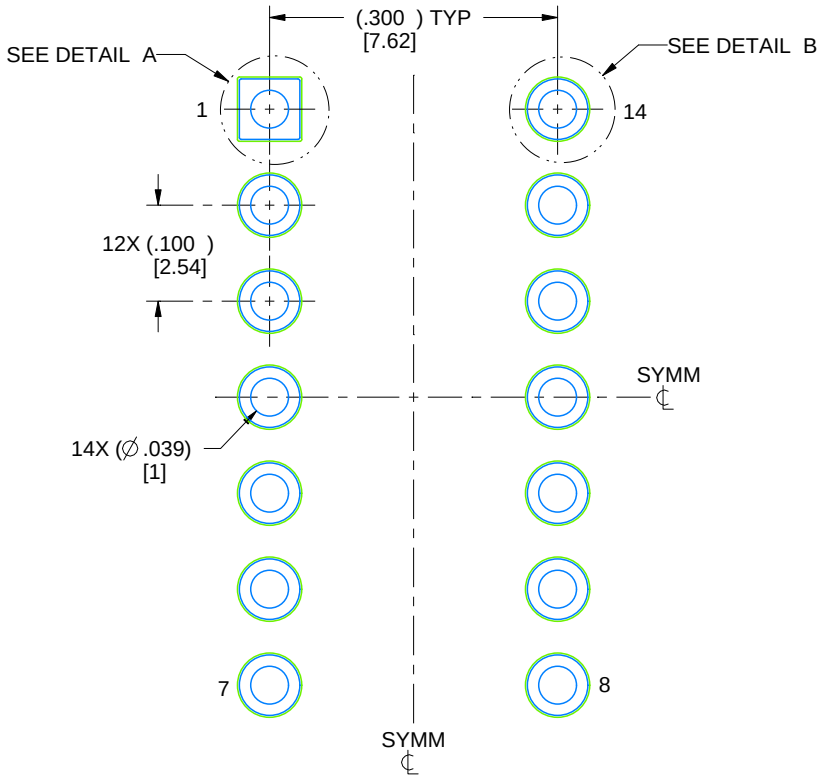
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

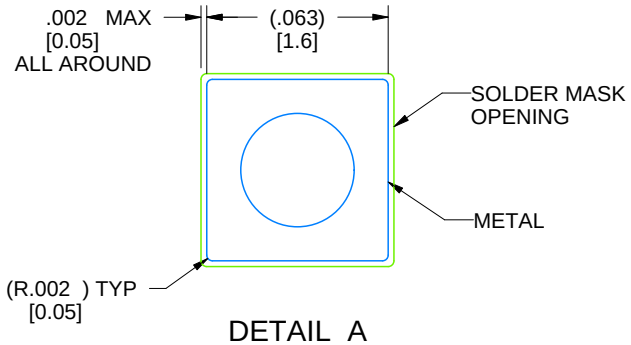
J0014A

CDIP - 5.08 mm max height

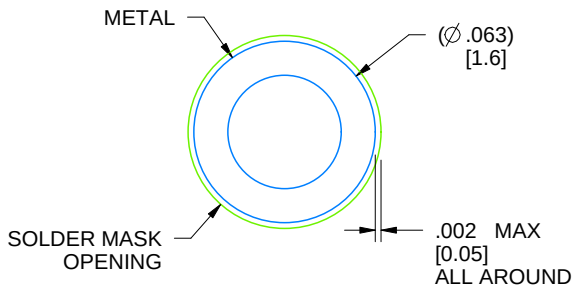
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X

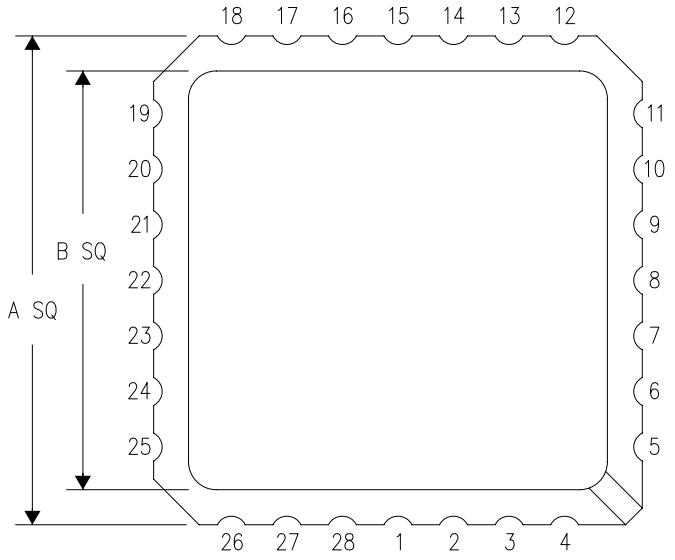


DETAIL B
13X, SCALE: 15X

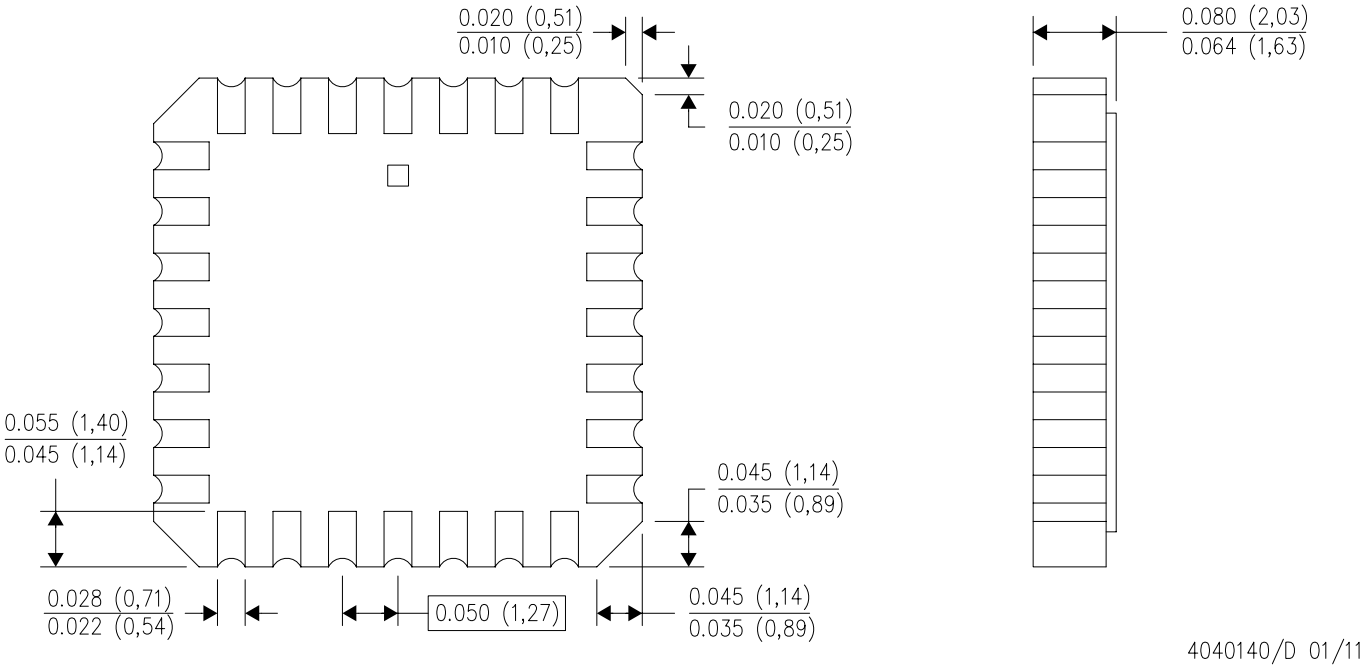
4214771/A 05/2017

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



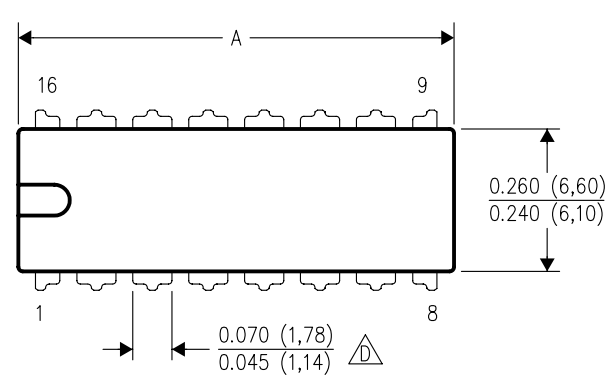
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

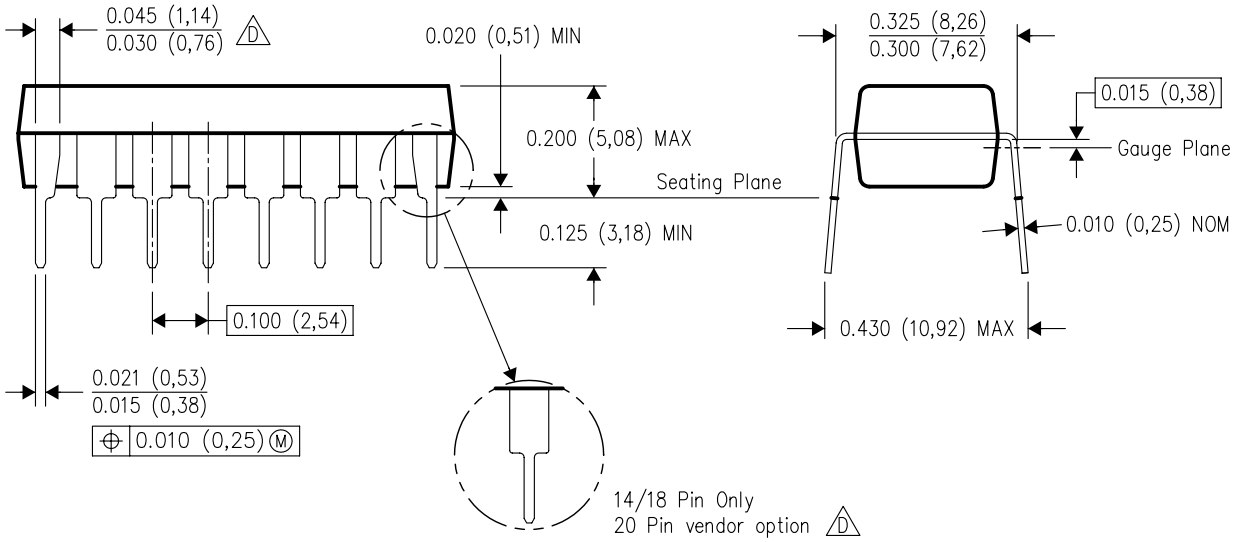
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



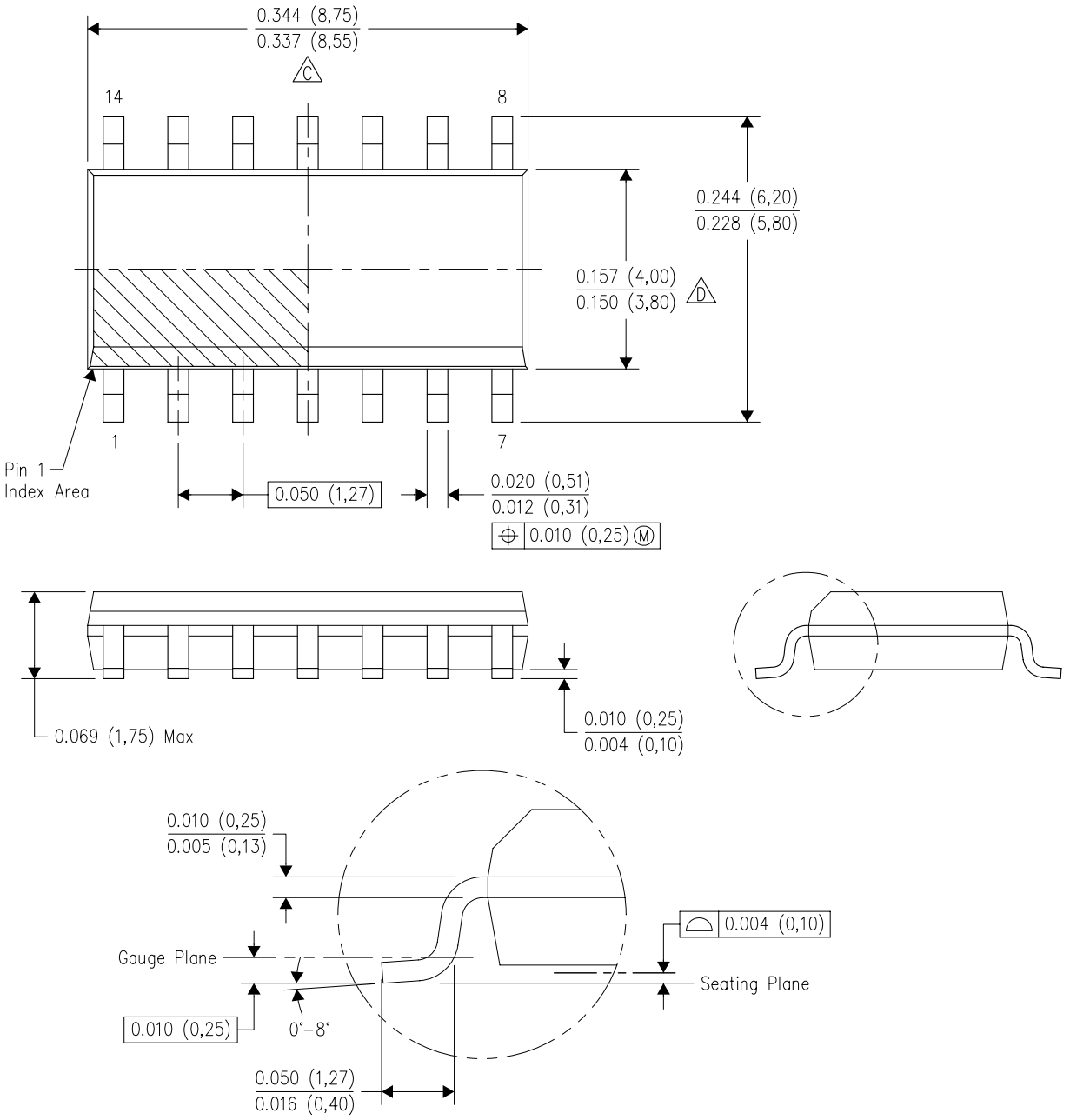
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

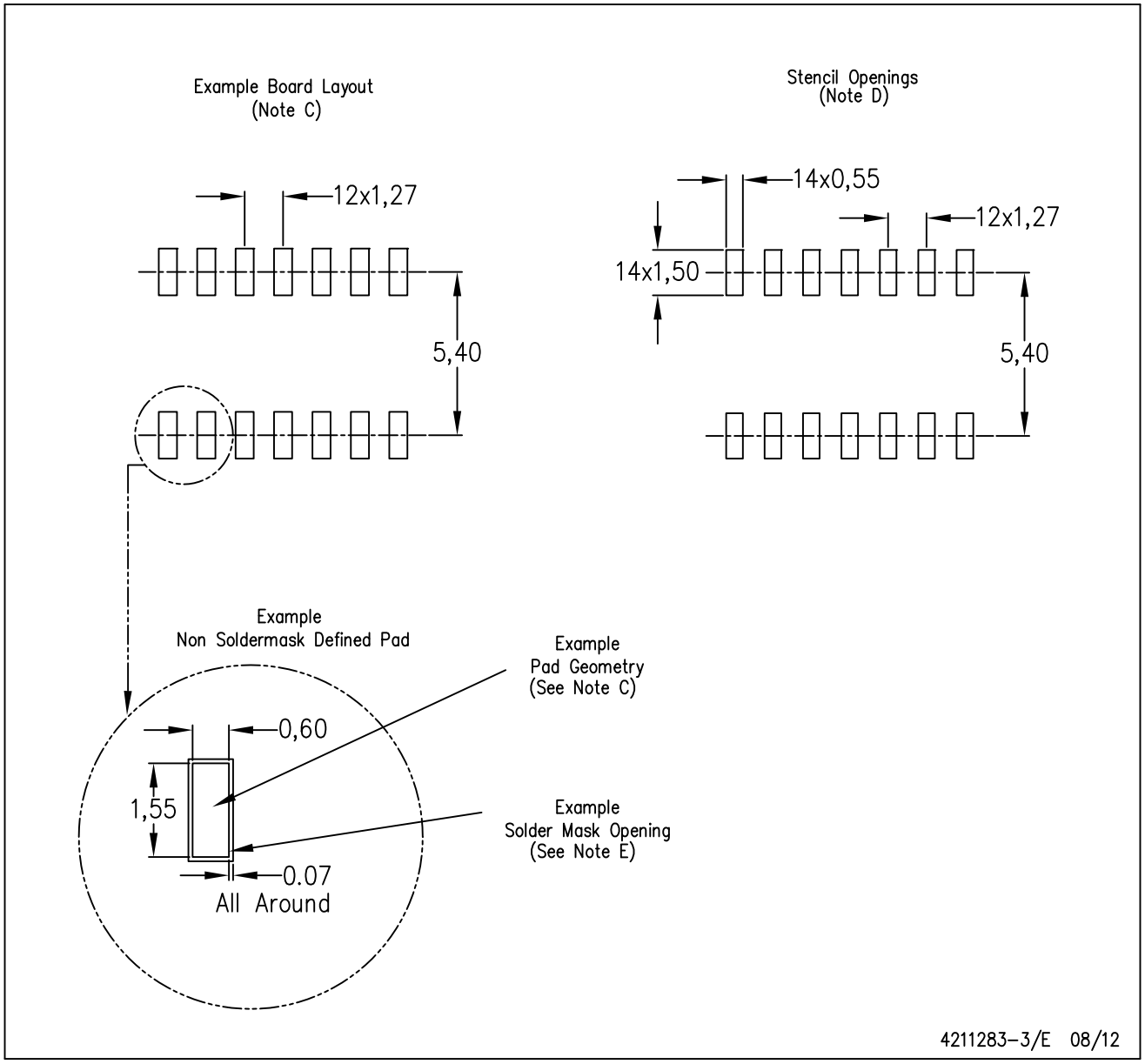
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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