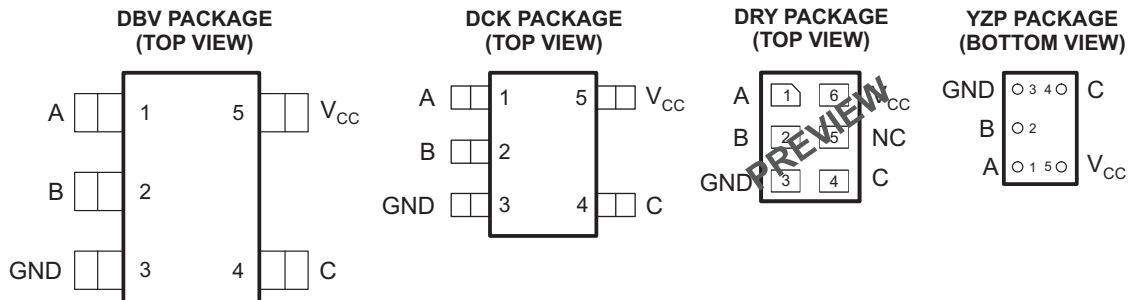


SINGLE BILATERAL ANALOG SWITCH

FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Wide V_{CC} Range of 0.8 V to 2.7 V
- Sub-1-V Operable
- Low Power Consumption, 10- μ A Max I_{CC}
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- High Speed – Max 0.2 ns ($V_{CC} = 1.8$ V, $C_L = 15$ pF)
- Low On-State Impedance – Typically 9 Ω ($V_{CC} = 2.3$ V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.
NC– No internal connection

DESCRIPTION/ORDERING INFORMATION

This single analog switch is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC1G66 can handle both analog and digital signals. The combined AC and DC signal has to be between V_{CC} and GND for it to be transmitted in either direction.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

ORDERING INFORMATION

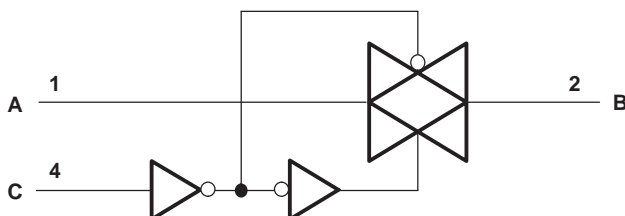
| T _A | PACKAGE ⁽¹⁾⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING ⁽³⁾ |
|----------------|---|--------------|-----------------------|---------------------------------|
| -40°C to 85°C | NanoFree™ W CSP (DSBGA) – YZP (Pb-free) | Reel of 3000 | SN74AUC1G66YZPR | --_U6_ |
| | SON – DRY | Reel of 5000 | SN74AUC1G66DRYR | PREVIEW |
| | SOT (SOT-23) – DBV | Reel of 3000 | SN74AUC1G66DBVR | U66_ |
| | SOT (SC-70) – DCK | Reel of 3000 | SN74AUC1G66DCKR | U6_ |

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (3) DBV/DCK/DRY: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

FUNCTION TABLE

| CONTROL INPUT (C) | SWITCH |
|-------------------|--------|
| L | OFF |
| H | ON |

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-------------------|---|--|-----------------------|------|
| V _{CC} | Supply voltage range | -0.5 | 3.6 | V |
| V _I | Input voltage range ⁽²⁾ | -0.5 | 3.6 | V |
| V _{I/O} | Switch I/O voltage range ⁽²⁾⁽³⁾ | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Control input clamp current | V _I < 0 | -50 | mA |
| I _{I/OK} | I/O port diode current | V _{I/O} < 0 or V _{I/O} > V _{CC} | ±50 | mA |
| I _T | On-state switch current | V _{I/O} = 0 to V _{CC} | ±50 | mA |
| | Continuous current through V _{CC} or GND | | ±100 | mA |
| θ _{JA} | Package thermal impedance ⁽⁴⁾ | DBV package | 206 | °C/W |
| | | DCK package | 252 | |
| | | DRY package | 234 | |
| | | YZP package | 123 | |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|------------------------------------|-----------------------------------|------------------------|------|
| V _{CC} | Supply voltage | 0.8 | 2.7 | V |
| V _{IH} | High-level input voltage | V _{CC} = 0.8 V | V _{CC} | V |
| | | V _{CC} = 1.1 V to 1.95 V | 0.65 × V _{CC} | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | |
| V _{IL} | Low-level input voltage | V _{CC} = 0.8 V | 0 | V |
| | | V _{CC} = 1.1 V to 1.95 V | 0.35 × V _{CC} | |
| | | V _{CC} = 2.3 V to 2.7 V | 0.7 | |
| V _{I/O} | I/O port voltage | 0 | V _{CC} | V |
| V _I | Control input voltage | 0 | 3.6 | V |
| Δt/Δv | Input transition rise or fall rate | | 20 | ns/V |
| T _A | Operating free-air temperature | −40 | 85 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------------|----------------------------------|---|-----------------------|-----------------|-----|--------------------|---------------------|------|
| r _{on} | On-state switch resistance | V _I = V _{CC} or GND, V _C = V _{IH} (see Figure 1) | I _S = 4 mA | 1.65 V | | 10 | 20 | Ω |
| | | | I _S = 8 mA | 2.3 V | | 9 | 15 | |
| r _{on(p)} | Peak on resistance | V _I = V _{CC} to GND, V _C = V _{IH} (see Figure 1) | I _S = 4 mA | 1.65 V | | 32 | 80 | Ω |
| | | | I _S = 8 mA | 2.3 V | | 15 | 20 | |
| I _{S(off)} | Off-state switch leakage current | V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _C = V _{IL} (see Figure 2) | | 2.7 V | | ±1 | ±0.1 ⁽¹⁾ | μA |
| I _{S(on)} | On-state switch leakage current | V _I = V _{CC} or GND, V _C = V _{IH} , V _O = Open (see Figure 3) | | 2.7 V | | ±1 | ±0.1 ⁽¹⁾ | μA |
| I _I | Control input current | V _I = V _{CC} or GND | | 0 to 2.7 V | | | ±5 | μA |
| I _{CC} | Supply current | V _I = V _{CC} or GND, I _O = 0 | | 0.8 V to 2.7 V | | | 10 | μA |
| C _{ic} | Control input capacitance | | | 2.5 V | | 2 | | pF |
| C _{io(off)} | Switch input/output capacitance | | | 2.5 V | | 3.5 | | pF |
| C _{io(on)} | Switch input/output capacitance | | | 2.5 V | | 7 | | pF |

(1) All typical values are at T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 0.8 V | V _{CC} = 1.2 V ± 0.1 V | | V _{CC} = 1.5 V ± 0.1 V | | V _{CC} = 1.8 V ± 0.15 V | | | V _{CC} = 2.5 V ± 0.2 V | | UNIT |
|--------------------------------|-----------------|----------------|-------------------------|------------------------------------|-----|------------------------------------|-----|-------------------------------------|-----|-----|------------------------------------|-----|------|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | TYP | MAX | MIN | MAX | |
| t _{pd} ⁽¹⁾ | A or B | B or A | 0.9 | | 0.3 | | | | | 0.2 | | 0.1 | ns |
| t _{en} | C | A or B | 4.1 | 0.5 | 2.6 | 0.5 | 1.7 | 0.5 | 0.8 | 1.1 | 0.5 | 1 | ns |
| t _{dis} | C | A or B | 5 | 0.7 | 3.6 | 0.5 | 2.6 | 0.5 | 1.7 | 2.9 | 0.5 | 2.2 | ns |

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see [Figure 4](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$ | | | $V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$ | | UNIT |
|----------------|-----------------|----------------|--|-----|-----|---|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}^{(1)}$ | A or B | B or A | 0.3 | | | 0.3 | | ns |
| t_{en} | C | A or B | 0.5 | 1.4 | 2.3 | 0.8 | 1.4 | ns |
| t_{dis} | C | A or B | 0.5 | 1.7 | 2.9 | 0.5 | 1.5 | ns |

- (1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Analog Switch Characteristics

 $T_A = 25^\circ\text{C}$

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | V _{CC} | TYP | UNIT |
|--|--------------|-------------|--|-----------------|------|------|
| Frequency response ⁽¹⁾ (switch ON) | A or B | B or A | C _L = 50 pF, R _L = 600 Ω, f _{in} = sine wave (see Figure 5) | 0.8 V | 60 | MHz |
| | | | | 1.1 V | 60 | |
| | | | | 1.4 V | 80 | |
| | | | | 1.65 V | 120 | |
| | | | | 2.3 V | 170 | |
| | | | C _L = 5 pF, R _L = 50 Ω, f _{in} = sine wave (see Figure 5) | 0.8 V | >500 | |
| | | | | 1.1 V | >500 | |
| | | | | 1.4 V | >500 | |
| | | | | 1.65 V | >500 | |
| | | | | 2.3 V | >500 | |
| Crosstalk (control input to signal output) | C | A or B | C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (square wave) (see Figure 6) | 0.8 V | 9 | mV |
| | | | | 1.1 V | 14 | |
| | | | | 1.4 V | 15 | |
| | | | | 1.65 V | 16 | |
| | | | | 2.3 V | 20 | |
| Feedthrough attenuation ⁽²⁾ (switch OFF) | A or B | B or A | C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave) (see Figure 7) | 0.8 V | -60 | dB |
| | | | | 1.1 V | -60 | |
| | | | | 1.4 V | -60 | |
| | | | | 1.65 V | -60 | |
| | | | | 2.3 V | -60 | |
| | | | C _L = 5 pF, R _L = 50 Ω, f _{in} = 1 MHz (sine wave) (see Figure 7) | 0.8 V | -55 | |
| | | | | 1.1 V | -55 | |
| | | | | 1.4 V | -55 | |
| | | | | 1.65 V | -55 | |
| | | | | 2.3 V | -55 | |
| Sine-wave distortion | A or B | B or A | C _L = 50 pF, R _L = 10 kΩ, f _{in} = 1 kHz (sine wave) (see Figure 8) | 0.8 V | 7.5 | % |
| | | | | 1.1 V | 0.16 | |
| | | | | 1.4 V | 0.04 | |
| | | | | 1.65 V | 0.03 | |
| | | | | 2.3 V | 0.02 | |
| | A or B | B or A | C _L = 50 pF, R _L = 10 kΩ, f _{in} = 10 kHz (sine wave) (see Figure 8) | 0.8 V | 4.2 | |
| | | | | 1.1 V | 0.2 | |
| | | | | 1.4 V | 0.03 | |
| | | | | 1.65 V | 0.02 | |
| | | | | 2.3 V | 0.02 | |

(1) Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads -3 dB.

(2) Adjust f_{in} voltage to obtain 0 dBm at input.

Operating Characteristics

 $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | V _{CC} = 0.8 V | V _{CC} = 1.2 V | V _{CC} = 1.5 V | V _{CC} = 1.8 V | V _{CC} = 2.5 V | UNIT |
|---|-----------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|------|
| | | TYP | TYP | TYP | TYP | TYP | |
| C _{pd} Power dissipation capacitance | f = 10 MHz | 3 | 3 | 3 | 3 | 3 | pF |

PARAMETER MEASUREMENT INFORMATION



Figure 1. On-State Resistance Test Circuit



Figure 2. Off-State Switch Leakage-Current Test Circuit

PARAMETER MEASUREMENT INFORMATION (Continued)

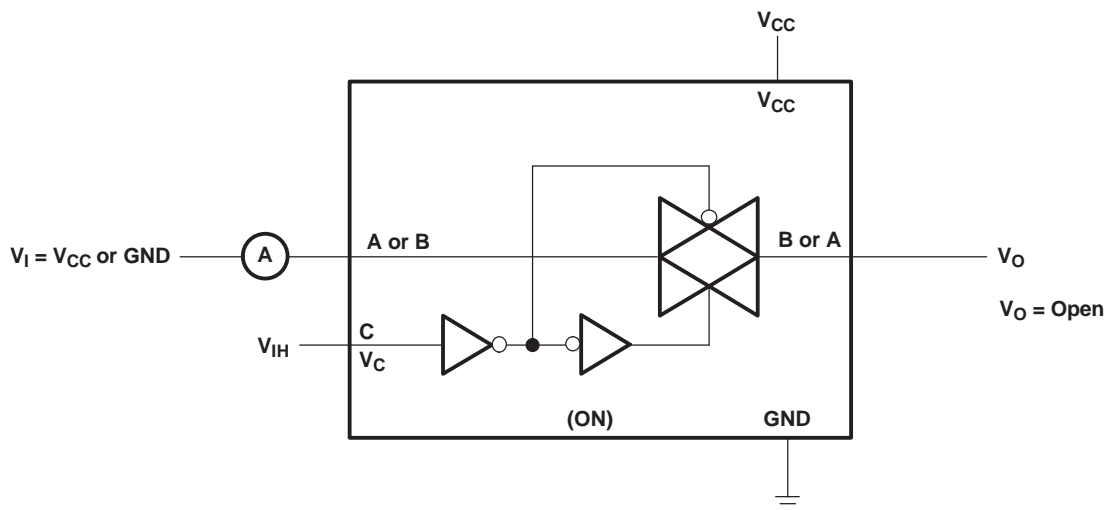


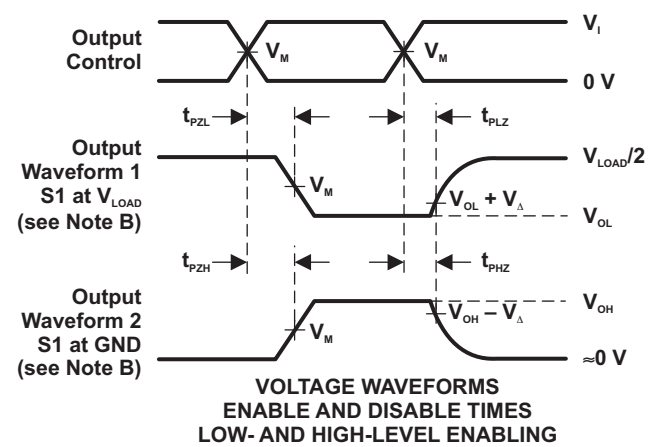
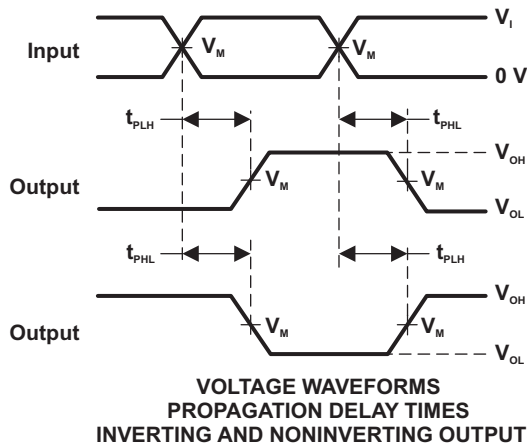
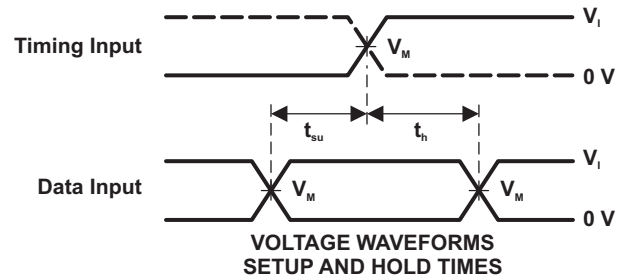
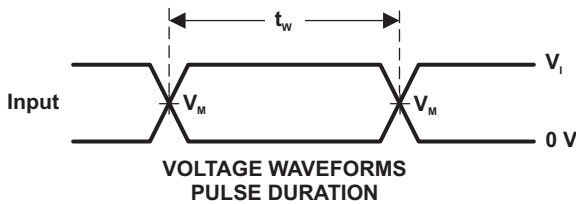
Figure 3. On-State Leakage-Current Test Circuit

PARAMETER MEASUREMENT INFORMATION (Continued)



| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|--------------------|----------|-------------|------------|-------------------|-------|--------------|--------------|
| | V_i | t_i/t_f | | | | | |
| 0.8 V | V_{CC} | ≤ 2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 2 k Ω | 0.1 V |
| 1.2 V \pm 0.1 V | V_{CC} | ≤ 2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 2 k Ω | 0.1 V |
| 1.5 V \pm 0.1 V | V_{CC} | ≤ 2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 2 k Ω | 0.1 V |
| 1.8 V \pm 0.15 V | V_{CC} | ≤ 2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 2 k Ω | 0.15 V |
| 2.5 V \pm 0.2 V | V_{CC} | ≤ 2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 2 k Ω | 0.15 V |
| 1.8 V \pm 0.15 V | V_{CC} | ≤ 2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| 2.5 V \pm 0.2 V | V_{CC} | ≤ 2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, Slew rate ≥ 1 V/ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 4. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (Continued)

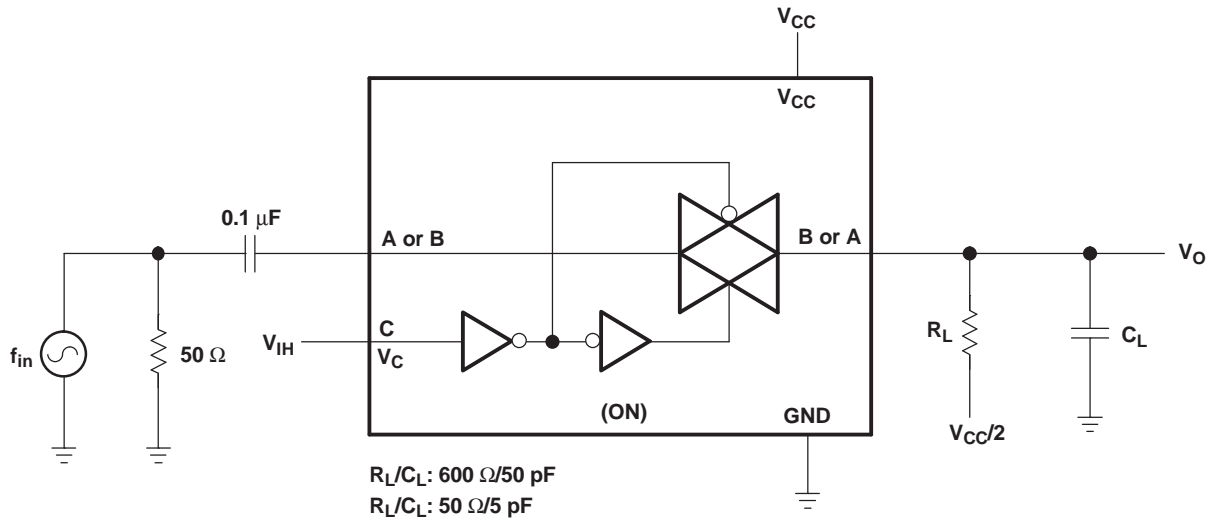


Figure 5. Frequency Response (Switch ON)

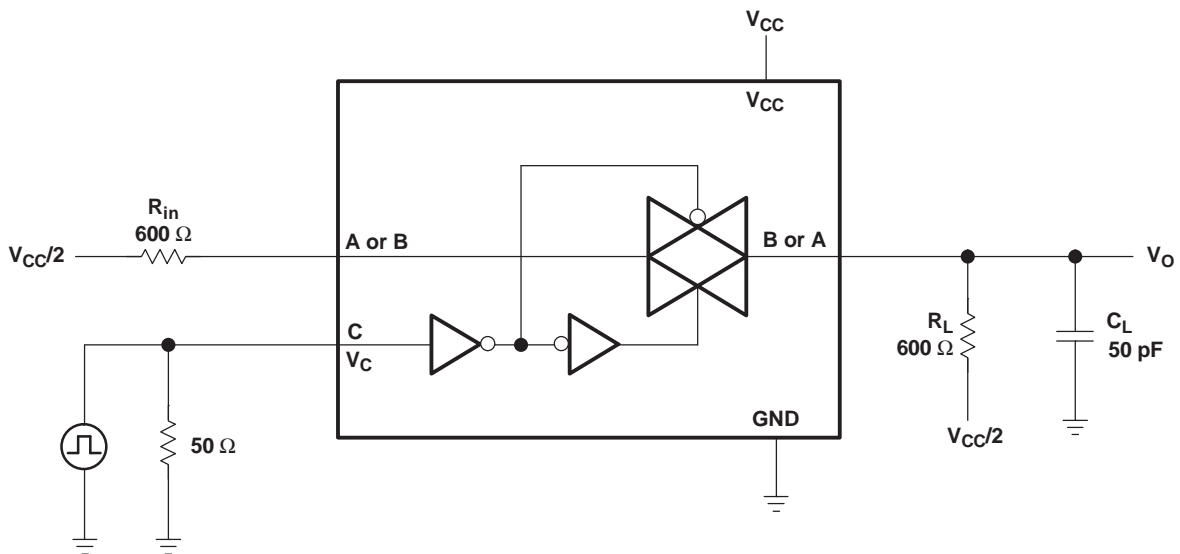


Figure 6. Crosstalk (Control Input – Switch Output)

PARAMETER MEASUREMENT INFORMATION (Continued)

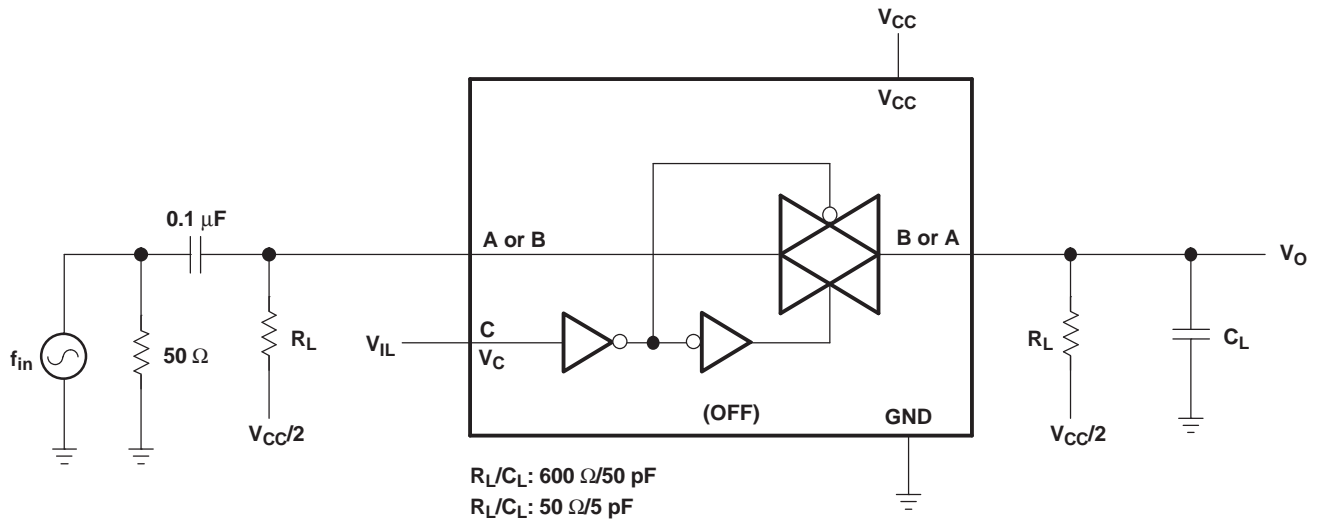


Figure 7. Feedthrough (Switch OFF)

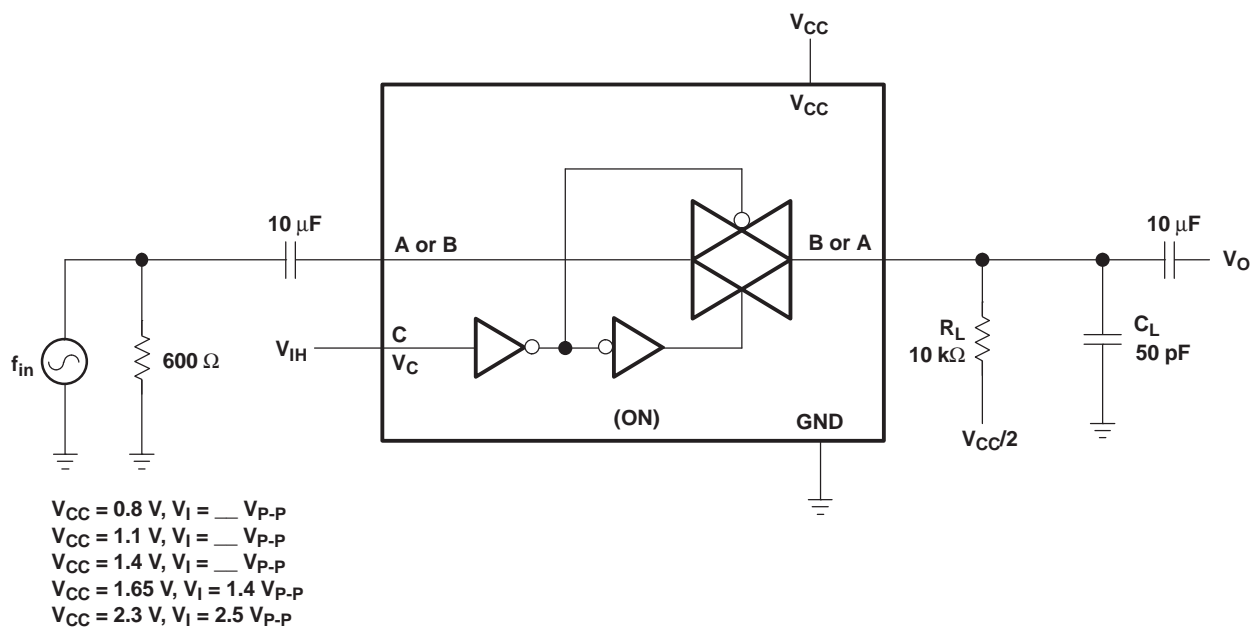


Figure 8. Sine-Wave Distortion

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74AUC1G66DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 85 | (U66F ~ U66R) | Samples |
| SN74AUC1G66DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (U65 ~ U6F ~ U6R) | Samples |
| SN74AUC1G66DCKRE4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (U65 ~ U6F ~ U6R) | Samples |
| SN74AUC1G66YZPR | ACTIVE | DSBGA | YZP | 5 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (U67 ~ U6N) | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AUC1G66DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUC1G66DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUC1G66DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AUC1G66DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AUC1G66YZPR | DSBGA | YZP | 5 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

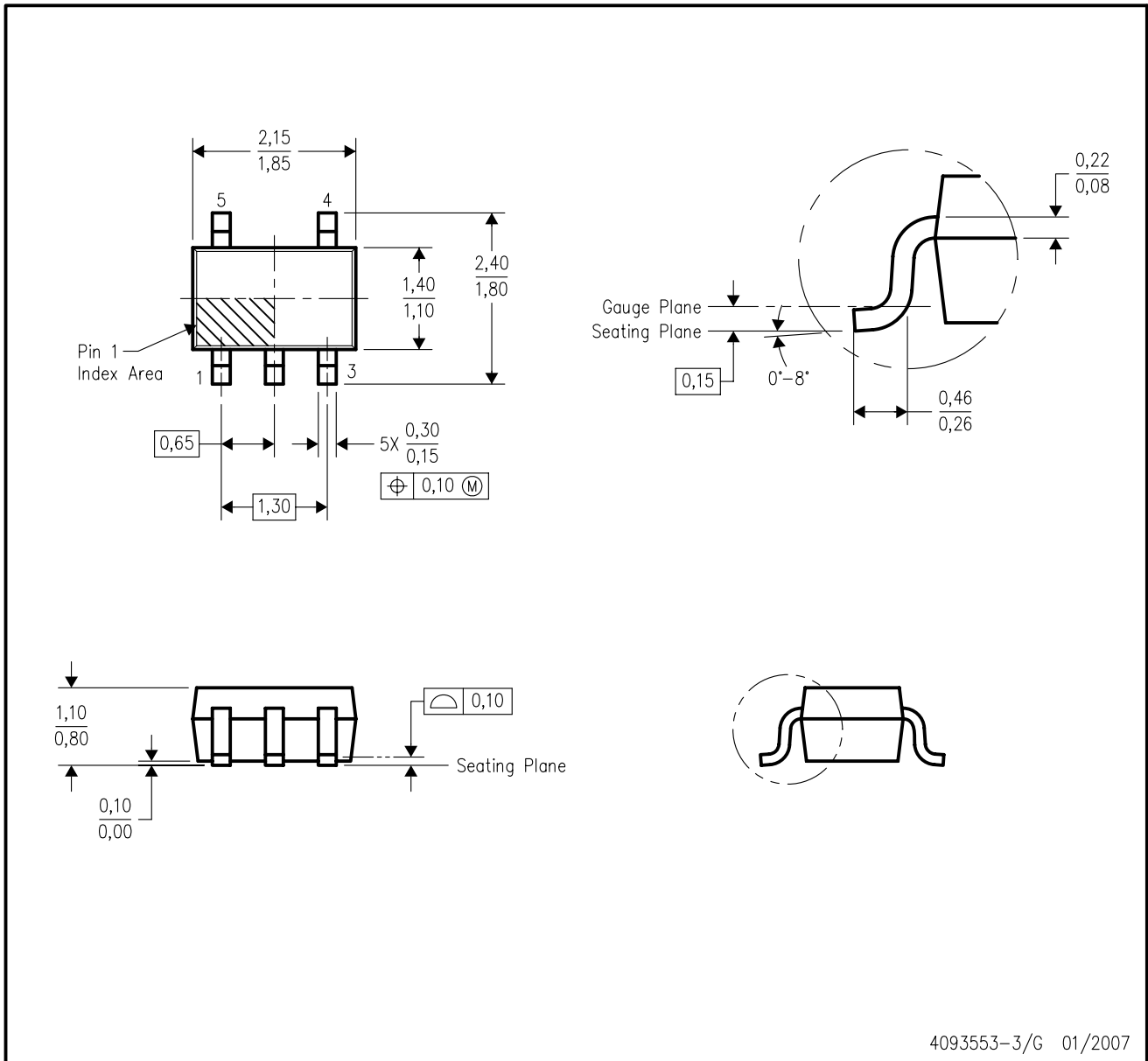
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AUC1G66DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUC1G66DBVR | SOT-23 | DBV | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUC1G66DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUC1G66DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUC1G66YZPR | DSBGA | YZP | 5 | 3000 | 220.0 | 220.0 | 35.0 |

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

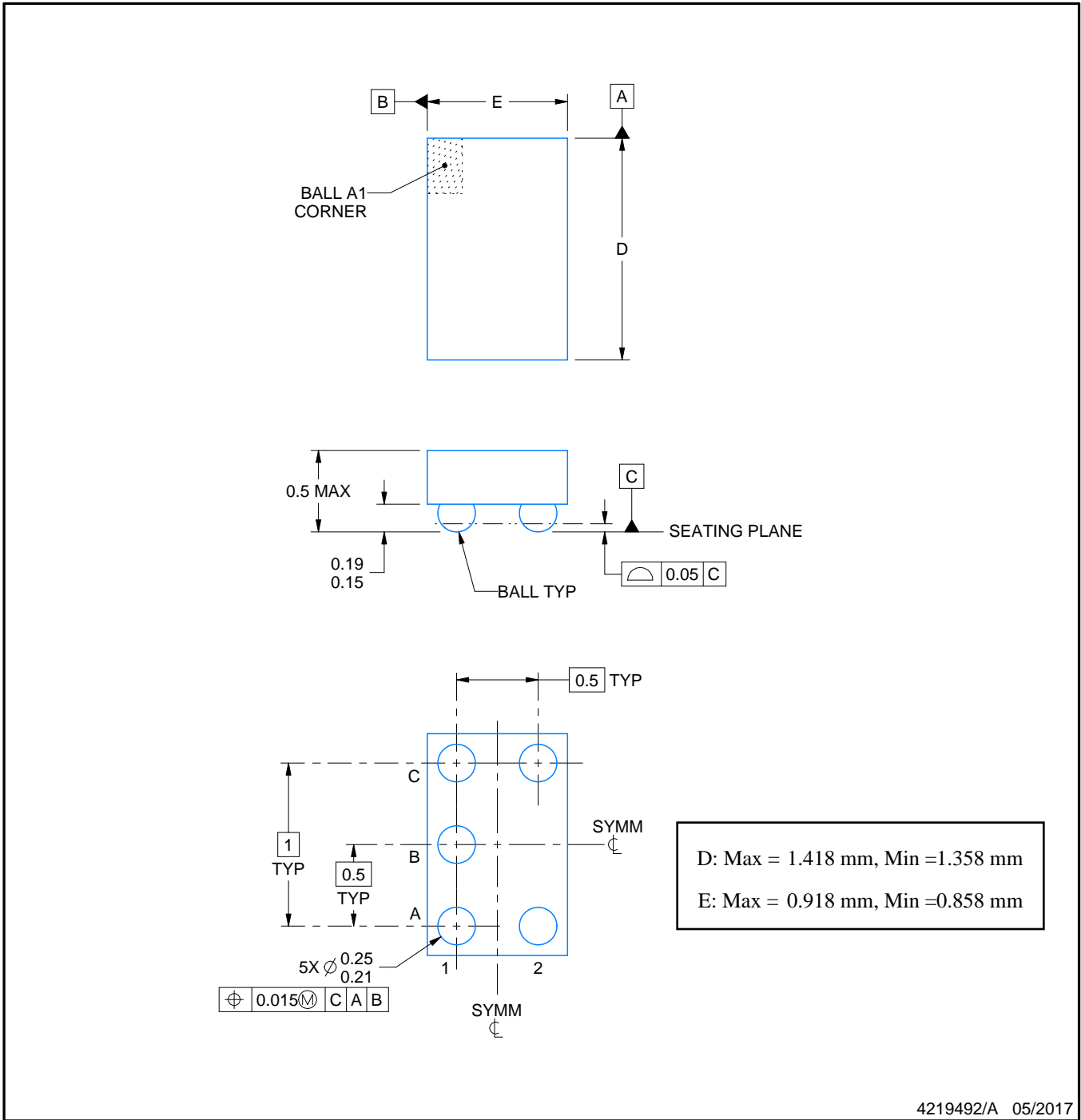
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

GENERIC PACKAGE VIEW

DBV 5

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073253/P

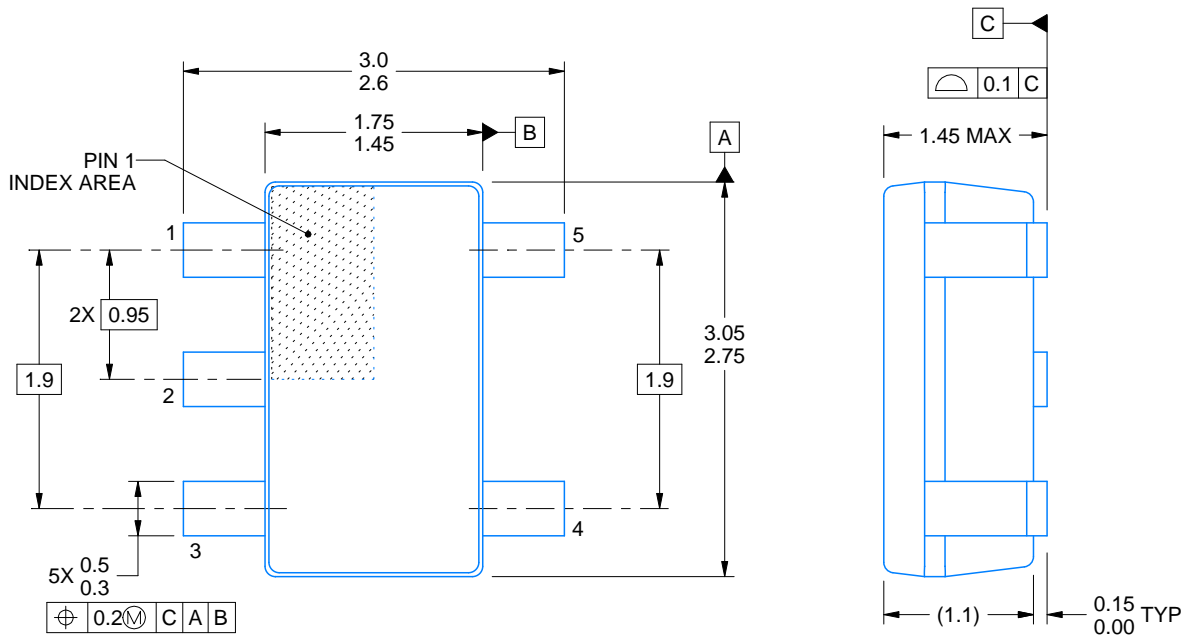
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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