

- Member of the Texas Instruments Widebus+™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Flow-Through Architecture Optimizes PCB Layout

description/ordering information

The SN74CBT32245 provides 32 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as four 8-bit bus switches, two 16-bit bus switches, or one 32-bit bus switch. When output enable (\overline{OE}) is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open and the high-impedance state exists between the two ports.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKE	Tape and reel	SN74CBT32245GKER	BV245
	LFBGA – ZKE (Pb-free)		SN74CBT32245ZKER	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 8-bit bus switch)

INPUT \overline{OE}	FUNCTION
L	A port = B port
H	Disconnect



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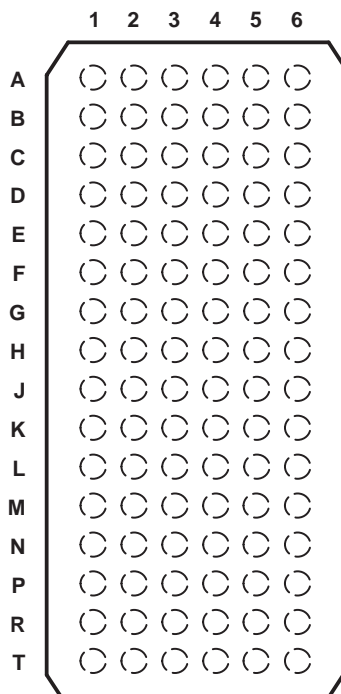
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



SN74CBT32245 32-BIT FET BUS SWITCH

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GKE OR ZKE PACKAGE
(TOP VIEW)

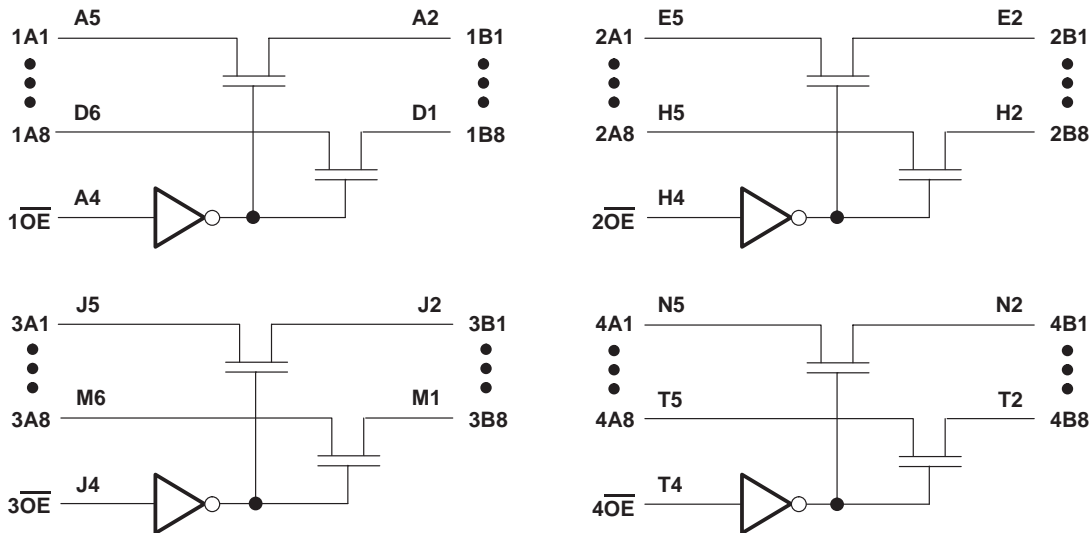


terminal assignments

	1	2	3	4	5	6
A	1B2	1B1	NC	$\overline{1OE}$	1A1	1A2
B	1B4	1B3	GND	GND	1A3	1A4
C	1B6	1B5	V _{CC}	V _{CC}	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
E	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	V _{CC}	V _{CC}	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
H	2B7	2B8	NC	$\overline{2OE}$	2A8	2A7
J	3B2	3B1	NC	$\overline{3OE}$	3A1	3A2
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	V _{CC}	V _{CC}	3A5	3A6
M	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
P	4B4	4B3	V _{CC}	V _{CC}	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
T	4B7	4B8	NC	$\overline{4OE}$	4A8	4A7

NC – No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): GKE/ZKE package	40°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4	5.5	V
V_{IH} High-level control input voltage	2		V
V_{IL} Low-level control input voltage		0.8	V
T_A Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
I_I	$V_{CC} = 5.5$ V, $V_I = 5.5$ V or GND			±5	µA
I_{CC}	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND			6	µA
ΔI_{CC}^{\S}	Control inputs $V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND			3.5	mA
C_i	Control inputs $V_I = 3$ V or 0			3.5	pF
$C_{iO(OFF)}$	$V_O = 3$ V or 0, $\overline{OE} = V_{CC}$			4.5	pF
r_{on}^{\parallel}	$V_{CC} = 4$ V, TYP at $V_{CC} = 4$ V	$V_I = 2.4$ V,		$I_I = 15$ mA	Ω
	$V_{CC} = 4.5$ V	$V_I = 0$		$I_I = 64$ mA	
				$I_I = 30$ mA	
		$V_I = 2.4$ V,		$I_I = 15$ mA	

‡ All typical values are at $V_{CC} = 5$ V (unless otherwise noted), $T_A = 25^\circ\text{C}$.

§ This is the increase in supply current for each input that is at the specified TTL-voltage level, rather than V_{CC} or GND.

∥ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

SN74CBT32245 32-BIT FET BUS SWITCH

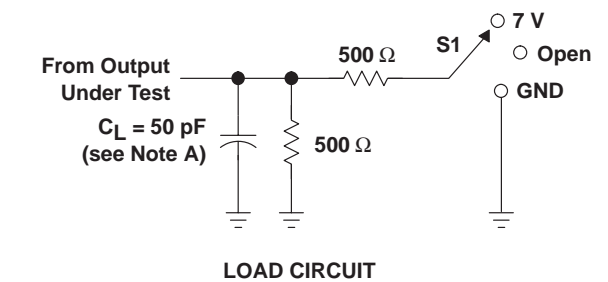
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

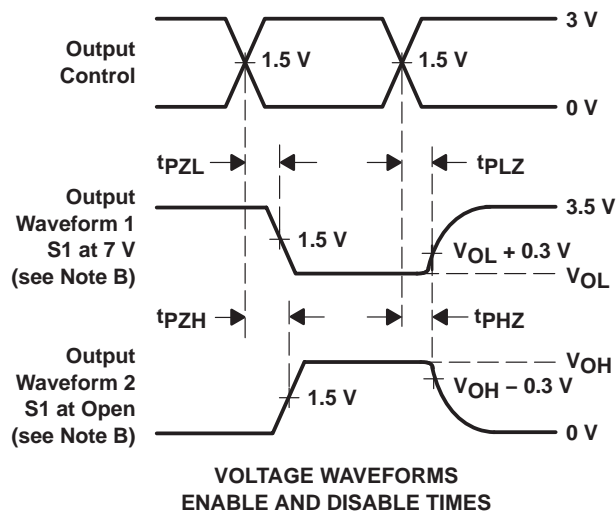
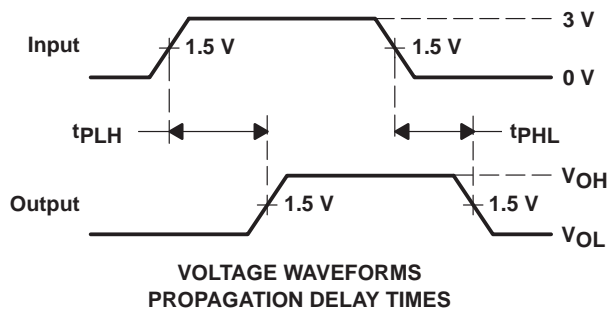
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} †	A or B	B or A	0.35		0.25		ns
t _{en}	\overline{OE}	A or B	6.1		1.2	5.6	ns
t _{dis}	\overline{OE}	A or B	7.5		3.9	7.7	ns

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{pd}	Open
t _{pLZ} /t _{pZL}	7 V
t _{pHZ} /t _{pZH}	Open



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω , t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{pLZ} and t_{pHZ} are the same as t_{dis}.
 - F. t_{pZL} and t_{pZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd}.
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBT32245ZKER	OBSOLETE	LFBGA	ZKE	96		TBD	Call TI	Call TI		BV245	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

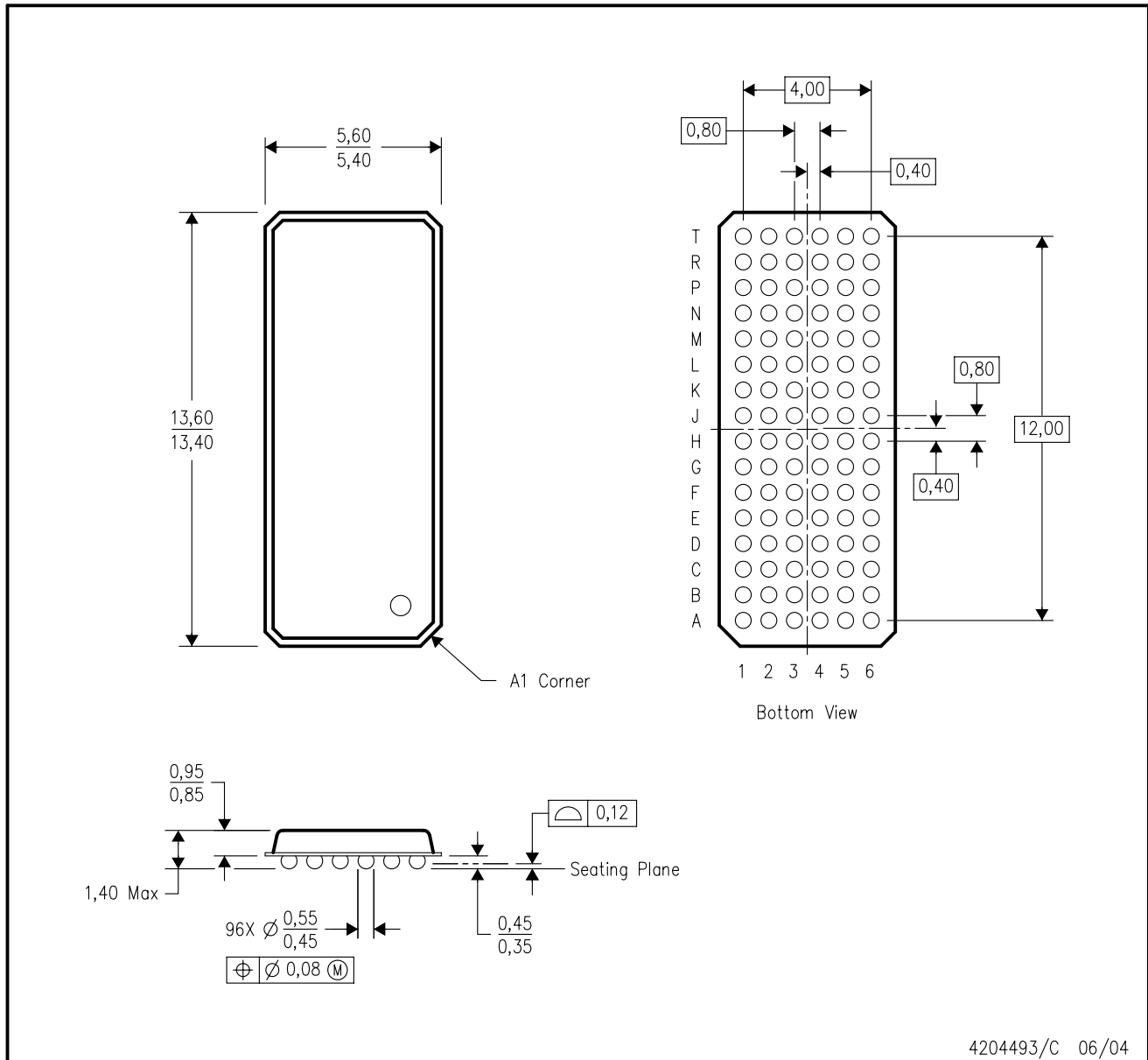
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation CC.
 - D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

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