## SN74CBTK32245 32-BIT FET BUS SWITCH WITH ACTIVE-CLAMP UNDERSHOOT-PROTECTION CIRCUIT

SCDS106E - APRIL 2000 - REVISED SEPTEMBER 2003

- Member of the Texas Instruments Widebus+<sup>TM</sup> Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Active-Clamp Undershoot-Protection Circuit on the I/Os Clamps Undershoots Up To -2 V
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

#### description/ordering information

The SN74CBTK32245 provides 32 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The A and B ports have an active-clamp undershoot-protection circuit. When there is an undershoot, the active-clamp circuit is enabled and current from  $V_{CC}$  is supplied to clamp the output, preventing the pass transistor from turning on.

The device is organized as four 8-bit bus switches, two 16-bit bus switches, or one 32-bit bus switch. When the output-enable  $(\overline{OE})$  input is low, the switch is on and port A is connected to port B. When  $\overline{OE}$  is high, the switch is open and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

TA	PACKAGET	-	ORDERABLE PART NUMBER	TOP-SIDE MARKING
400C to 850C	LFBGA – GKE	Topo and real	SN74CBTK32245GKER	KT245
-40°C to 85°C	LFBGA – ZKE (Pb-free)	Tape and reel	SN74CBTK32245ZKER	K1245

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## FUNCTION TABLE (each 8-bit bus switch)

INPUT OE	FUNCTION
L	A port = B port
Н	Disconnect



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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#### **GKE OR ZKE PACKAGE** (TOP VIEW)

		1	2	3	4	5	6	_
Α	/	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	1
В		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
С		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
D		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
Е		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
F		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
G		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
н		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
J		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
ĸ		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
L		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
М		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
N		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
Р		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
R		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
т		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	,

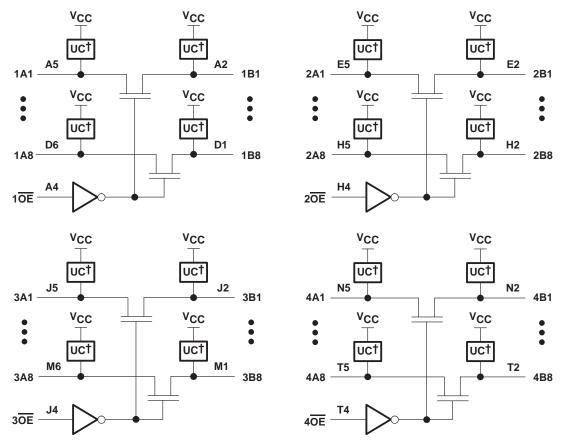
## terminal assignments

	1	2	3	4	5	6
Α	1B2	1B1	NC	10E	1A1	1A2
В	1B4	1B3	GND	GND	1A3	1A4
С	1B6	1B5	Vcc	Vcc	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
Е	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	Vcc	Vcc	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
Н	2B7	2B8	NC	2OE	2A8	2A7
J	3B2	3B1	NC	3OE	3A1	3A2
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	Vcc	Vcc	3A5	3A6
M	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
Р	4B4	4B3	Vcc	Vcc	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
Т	4B7	4B8	NC	4OE	4A8	4A7

NC - No internal connection

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## logic diagram (positive logic)



<sup>†</sup> Undershoot clamp

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, $I_{IK}$ ( $V_{I/O}$ < 0)	–50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2): GKE/ZKE package	40°C/W
Storage temperature range, T <sub>stq</sub>	. −65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



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#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER		TEST CONDITIO	NS	MIN	TYP <sup>†</sup>	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$				-1.2	V
VIKU		$V_{CC} = 5.5 V,$	$0~mA \geq I_{I} \geq -50~mA,$	<del>OE</del> = 5.5 V			-2	V
lį		$V_{CC} = 5.5 V,$	$V_I = 5.5 \text{ V or GND}$				±5	μΑ
l <sub>off</sub>		$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to 5.5 $V$				20	μΑ
ICC		$V_{CC} = 5.5 V,$	$V_I = V_{CC}$ or GND,	IO = 0			6	μΑ
∆lcc <sup>‡</sup>	Control inputs	$V_{CC} = 5.5 V,$	One input at 3.4 V,	Other inputs at V <sub>CC</sub> or GND			3.5	mA
Ci	Control inputs	$V_I = 3 V \text{ or } 0$				3.5		pF
C <sub>io(OFF</sub>	F)	$V_{O} = 3 \text{ V or } 0,$	OE = V <sub>CC</sub>			5.5		pF
		$V_{CC} = 4 \text{ V},$ TYP at $V_{CC} = 4 \text{ V}$	V <sub>I</sub> = 2.4 V,	I <sub>I</sub> = 15 mA		14	20	
r <sub>on</sub> §				I <sub>I</sub> = 64 mA		5	7	Ω
		V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 0	I <sub>I</sub> = 30 mA		5	7	
			V <sub>I</sub> = 2.4 V,	I <sub>I</sub> = 15 mA		8	12	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$  (unless otherwise noted),  $T_A = 25^{\circ}\text{C}$ .

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM	TO	V <sub>CC</sub> = 4 V	V <sub>CC</sub> =	= 5 V 5 V	UNIT
	(INPUT)	(OUTPUT)	MIN MAX	MIN	MAX	
t <sub>pd</sub> ¶	A or B	B or A	0.35		0.25	ns
t <sub>en</sub>	ŌE	A or B	7.4	1.6	4.9	ns
<sup>t</sup> dis	ŌĒ	A or B	7.4	4.2	7.5	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



<sup>‡</sup> This is the increase in supply current for each input that is at the specified TTL-voltage level, rather than V<sub>CC</sub> or GND.

<sup>§</sup> Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

#### undershoot characteristics

 PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Voutu	See Figures 1 and 2, and Table 1		V <sub>OH</sub> -0.3		V

 $<sup>\</sup>dagger$  All typical values are at V<sub>CC</sub> = 5 V (unless otherwise noted), T<sub>A</sub> = 25°C.

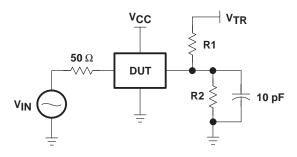


Figure 1. Device Test Setup

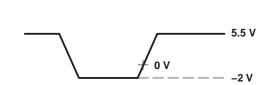


Figure 2. Transient Input Voltage Waveform

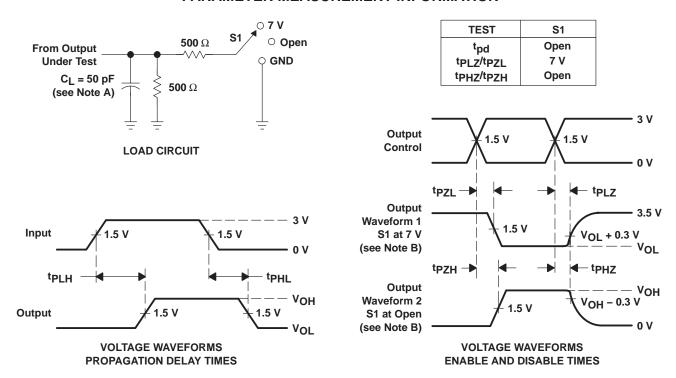
**Table 1. Device Test Conditions** 

PARAMETER	VALUE	UNIT
B port under test <sup>‡</sup>	See Figure 1	
VIN	See Figure 2	V
t <sub>W</sub>	20	ns
t <sub>r</sub>	2	ns
t <sub>f</sub>	2	ns
R1 = R2	100	kΩ
$V_{TR}$	11	V
Vcc	5.5	V

<sup>‡</sup>Other B-port outputs are open

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_{O} = 50 \Omega$ ,  $t_{r} \leq$  2.5 ns.  $t_{f} \leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms





## PACKAGE OPTION ADDENDUM

24-Sep-2015

#### PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBTK32245ZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	KT245	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**PACKAGE MATERIALS INFORMATION** 

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## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

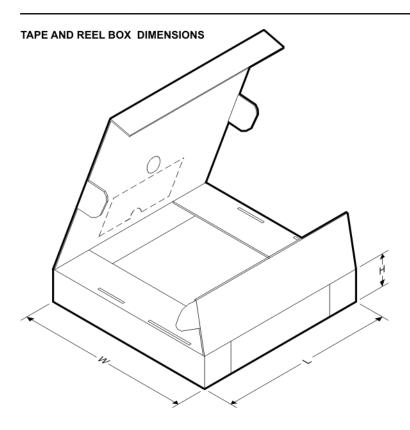
#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTK32245ZKER	LFBGA	ZKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1

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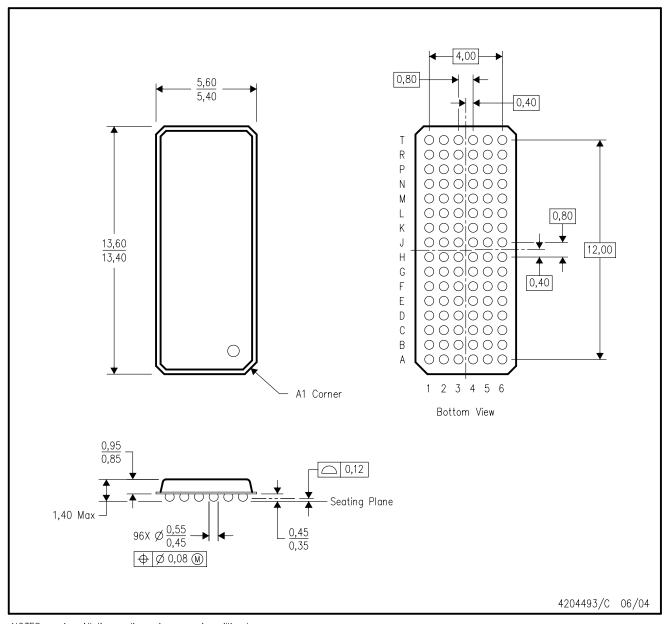


#### \*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
S	N74CBTK32245ZKER	LFBGA	ZKE	96	1000	336.6	336.6	41.3

## ZKE (R-PBGA-N96)

## PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-205 variation CC.
- D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).



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