HEX BUS DRIVERS WITH 3-STATE OUTPUTS

DECEMBER 1983—REVISED MARCH 1988

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Choice of True or Inverting Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

'365A, '367A, 'LS365A, 'LS367A True Outputs '366A, '368A, 'LS366A, 'LS368A Inverting Outputs

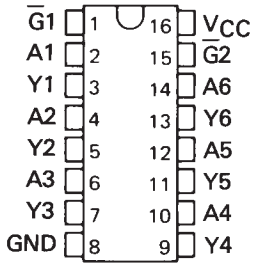
description

These Hex buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus oriented receivers and transmitters. The designer has choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low control) inputs.

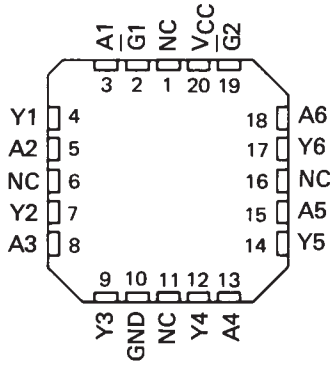
These devices feature high fan-out, improved fan-in, and can be used to drive terminated lines down to 133 ohms.

The SN54365A thru SN54368A and SN54LS365A thru SN54LS368A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74365A thru SN74368A and SN74LS365A thru SN74LS368A are characterized for operation from 0°C to 70°C.

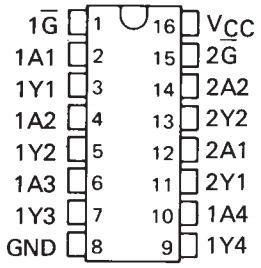
SN54365A, 366A, SN54LS365A, 366A . . . J PACKAGE
SN74365A, 366A . . . N PACKAGE
SN74LS365A, SN74LS366A . . . D OR N PACKAGE
(TOP VIEW)



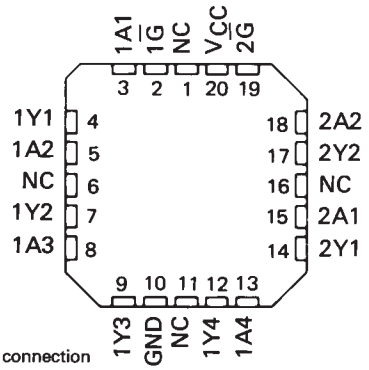
SN54LS365A, SN54LS366A . . . FK PACKAGE
(TOP VIEW)



SN54367A, 368A, SN54LS367A, 368A . . . J PACKAGE
SN74367A, 368A . . . N PACKAGE
SN74LS367A, SN74LS368A . . . D OR N PACKAGE
(TOP VIEW)



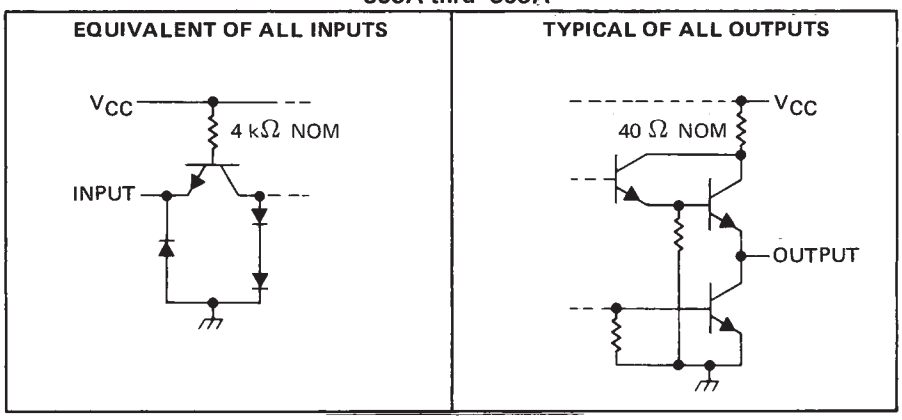
SN54LS367A, SN54LS368A . . . FK PACKAGE
(TOP VIEW)



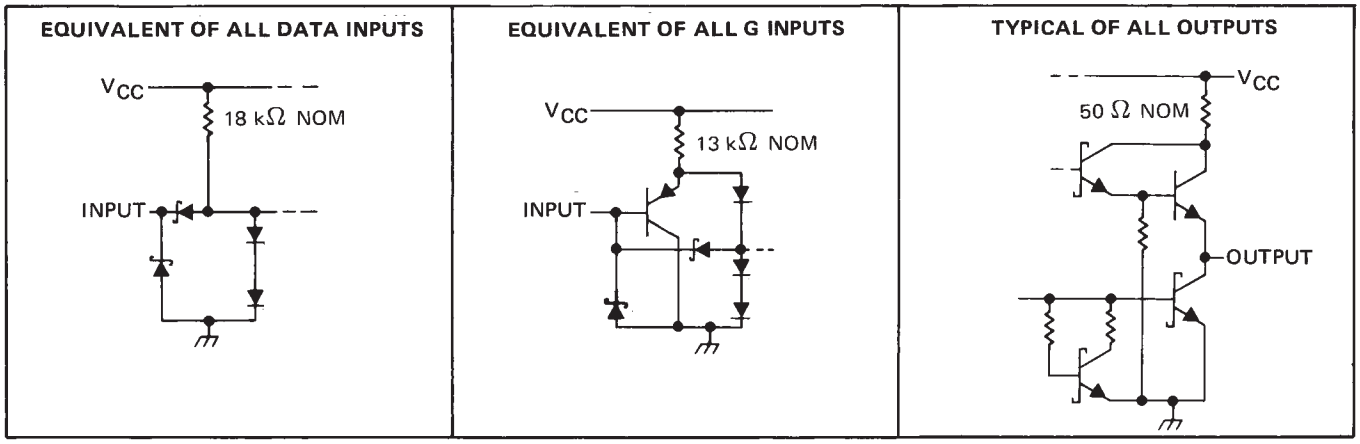
NC – No internal connection

schematics of inputs and outputs

'365A thru '368A

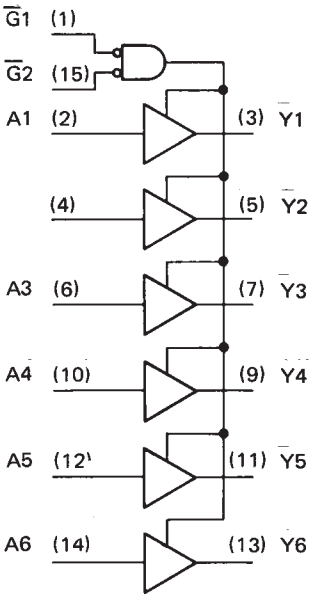


'LS365A thru 'LS368A

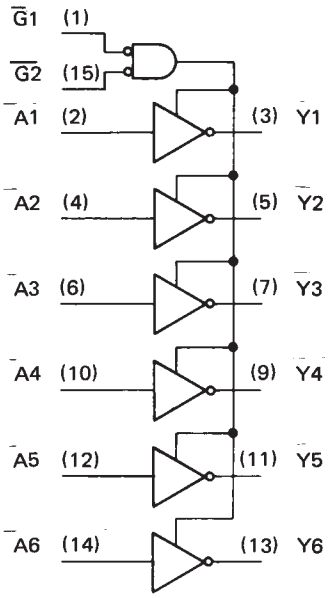


logic diagrams (positive logic)

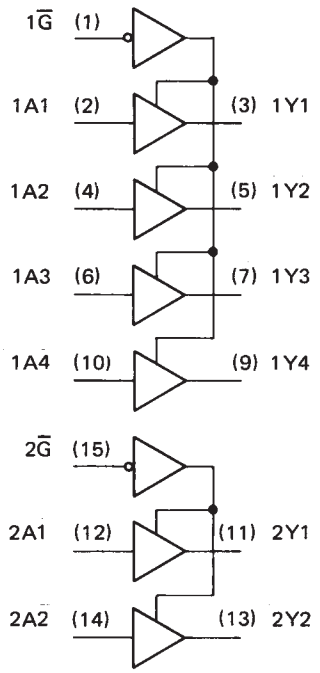
'365A, 'LS365A



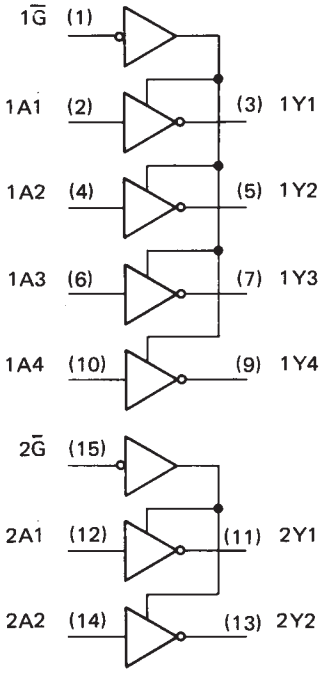
'366A, 'LS366A



'367A, 'LS367A



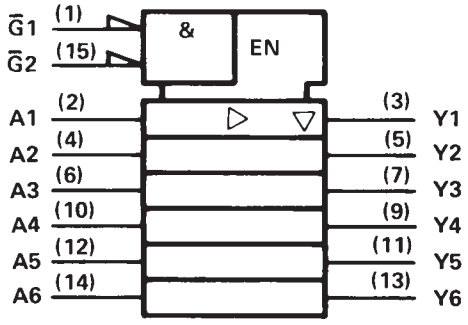
'368A, 'LS368A



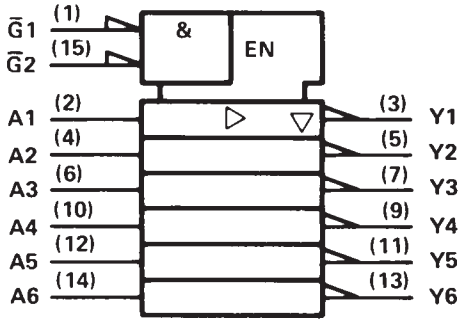
Pin numbers shown are for D, J, and N packages.

logic symbols†

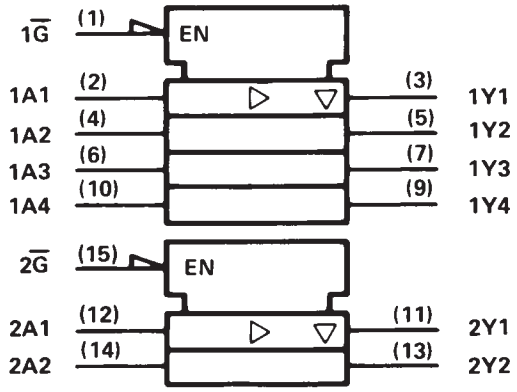
'365A



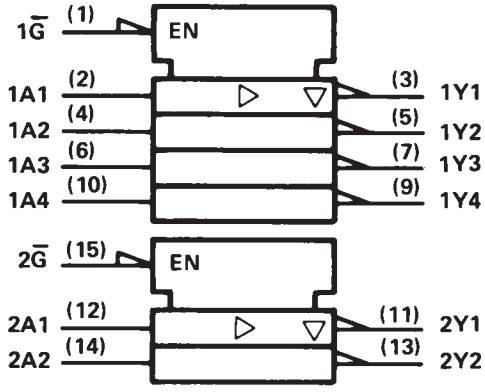
'366A



'367A



'368A



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '365A, '366A, '367A, '368A . . . . . 5.5 V
'LS365A, 'LS366A, 'LS367A, 'LS368A . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54365A SN54367A			SN74365A SN74367A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−5.2	mA
I_{OL}	Low-level output current			32			32	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54365A SN54367A			SN74365A SN74367A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −12 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.3		2.4	3.1		V
V_{OL}		V_{CC} = MIN, I_{OL} = 32 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,			0.4			0.4	V
I_{OZ}		V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,	V_{IL} = 0.8 V,			40			40	μA
		V_{CC} = MAX, V_O = 0.4 V	V_{IH} = 2 V	V_{IL} = 0.8 V,			−40			−40	
I_I		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
I_{IL}	A Inputs	V_{CC} = MAX,	V_I = 0.5 V,	Either $\overline{G}$ input at 2 V			−40			−40	μA
	A Inputs	V_{CC} = MAX,	V_I = 0.4 V,	Both $\overline{G}$ inputs at 0.4 V			−1.6			−1.6	mA
	$\overline{G}$ Inputs	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	
I_{OS}§		V_{CC} = MAX			−40		−130	−40		−130	mA
I_{CC}		V_{CC} = MAX,	Data inputs = 0 V,	Output controls = 4.5 V		65	85		65	85	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	R_L = 400 Ω,	C_L = 50 pF			16	ns
t_{PHL}							22	ns
t_{PZH}							35	ns
t_{PZL}							37	ns
t_{PHZ}			R_L = 400 Ω,	C_L = 5 pF			11	ns
t_{PLZ}							27	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54366A SN54368A			SN74366A SN74368A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−5.2	mA
I_{OL}	Low-level output current			32			32	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54366A SN54368A			SN74366A SN74368A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −12 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.3		2.4	3.1		V
V_{OL}	V_{CC} = MIN, I_{OL} = 32 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,			0.4			0.4	V
I_{OZ}	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,	V_{IL} = 0.8 V,			40			40	μA
	V_{CC} = MAX, V_O = 0.4 V	V_{IH} = 2 V	V_{IL} = 0.8 V,			−40			−40	
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
I_{IL} A Inputs	V_{CC} = MAX,	V_I = 0.5 V,	Either $\overline{G}$ input at 2 V			−40			−40	μA
I_{IL} A Inputs	V_{CC} = MAX,	V_I = 0.4 V,	Both $\overline{G}$ inputs at 0.4 V			−1.6			−1.6	mA
I_{IL} $\overline{G}$ Inputs	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}§	V_{CC} = MAX			−40		−130	−40		−130	mA
I_{CC}	V_{CC} = MAX,	Data inputs = 0 V,	Output controls = 4.5 V,		59	77		59	77	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	R_L = 400 Ω,	C_L = 50 pF			17	ns
t_{PHL}							16	ns
t_{PZH}							35	ns
t_{PZL}							37	ns
t_{PHZ}			R_L = 400 Ω,	C_L = 5 pF			11	ns
t_{PLZ}							27	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54LS365A SN54LS367A			SN74LS365A SN74LS367A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS365A SN54LS367A			SN74LS365A SN74LS367A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA					−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	V_{IL} = MAX,	2.4	3.3		2.4	3.1		V
V_{OL}		V_{CC} = MIN, I_{OL} = 12 mA	V_{IH} = 2 V,	V_{IL} = MAX,		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 24 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,					0.35	0.5	
I_{OZ}		V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,	V_{IL} = MAX,			20			20	μA
		V_{CC} = MAX, V_O = 0.4 V	V_{IH} = 2 V,	V_{IL} = MAX,			−20			−20	
I_I		V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	A Inputs	V_{CC} = MAX,	V_I = 0.5 V,	Either $\overline{G}$ input at 2 V			−20			−20	μA
	A Inputs	V_{CC} = MAX,	V_I = 0.4 V,	Both $\overline{G}$ inputs at 0.4 V			−0.4			−0.4	mA
	$\overline{G}$ Inputs	V_{CC} = MAX,	V_I = 0.4 V				−0.2			−0.2	
I_{OS}§		V_{CC} = MAX			−40		−225	−40		−225	mA
I_{CC}		V_{CC} = MAX,	Data inputs = 0 V,	Output controls = 4.5 V,		14	24		14	24	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	R_L = 667 Ω, C_L = 45 pF		10	16	ns
t_{PHL}					9	22	ns
t_{PZH}					19	35	ns
t_{PZL}					24	40	ns
t_{PHZ}			R_L = 667 Ω, C_L = 5 pF			30	ns
t_{PLZ}						35	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54LS366A SN54LS368A			SN74LS366A SN74LS368A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS366A SN54LS368A			SN74LS366A SN74LS368A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA					−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	V_{IL} = MAX,	2.4	3.3		2.4	3.1		V
V_{OL}		V_{CC} = MIN, I_{OL} = 12 mA	V_{IH} = 2 V,	V_{IL} = MAX,		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 24 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,					0.35	0.5	
I_{OZ}		V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,	V_{IL} = MAX,			20			20	μA
		V_{CC} = MAX, V_O = 0.4 V	V_{IH} = 2 V,	V_{IL} = MAX,			−20			−20	
I_I		V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	A Inputs	V_{CC} = MAX,	V_I = 0.5 V,	Either $\overline{G}$ input at 2 V			−20			−20	uA
		V_{CC} = MAX,	V_I = 0.4 V,	Both $\overline{G}$ inputs at 0.4 V			−0.4			−0.4	mA
	$\overline{G}$ Inputs	V_{CC} = MAX,	V_I = 0.4 V				−0.2			−0.2	
I_{OS}§		V_{CC} = MAX			−40		−225	−40		−225	mA
I_{CC}		V_{CC} = MAX,	Data inputs = 0 V,	Output controls = 4.5 V,		12	21		12	21	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	R_L = 667 Ω, C_L = 45 pF		7	15	ns
t_{PHL}					12	18	ns
t_{PZH}					18	35	ns
t_{PZL}					28	45	ns
t_{PHZ}			R_L = 667 Ω, C_L = 5 pF			32	ns
t_{PLZ}						35	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/32201B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32201B2A	Samples
JM38510/32201BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32201BEA	Samples
JM38510/32201BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32201BEA	Samples
JM38510/32203B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32203B2A	Samples
JM38510/32203B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32203B2A	Samples
JM38510/32203BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32203BEA	Samples
JM38510/32203BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32203BEA	Samples
JM38510/32203BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32203BFA	Samples
JM38510/32203BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32203BFA	Samples
M38510/32201B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32201B2A	Samples
M38510/32201B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32201B2A	Samples
M38510/32201BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32201BEA	Samples
M38510/32201BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32201BEA	Samples
M38510/32203B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32203B2A	Samples
M38510/32203B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32203B2A	Samples
M38510/32203BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32203BEA	Samples
M38510/32203BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32203BEA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
M38510/32203BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32203BFA	Samples
M38510/32203BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32203BFA	Samples
SN54LS365AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS365AJ	Samples
SN54LS365AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS365AJ	Samples
SN54LS366AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS366AJ	Samples
SN54LS366AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS366AJ	Samples
SN54LS367AJ	ACTIVE	CDIP	J	16	25	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS367AJ	Samples
SN54LS367AJ	ACTIVE	CDIP	J	16	25	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS367AJ	Samples
SN54LS368AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS368AJ	Samples
SN54LS368AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS368AJ	Samples
SN74LS365AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS365A	Samples
SN74LS365AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS365A	Samples
SN74LS365ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS365A	Samples
SN74LS365ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS365A	Samples
SN74LS365AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS365AN	Samples
SN74LS365AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS365AN	Samples
SN74LS365ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS365A	Samples
SN74LS365ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS365A	Samples
SN74LS367AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS367A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS367AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS367A	Samples
SN74LS367ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS367A	Samples
SN74LS367ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS367A	Samples
SN74LS367AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS367AN	Samples
SN74LS367AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS367AN	Samples
SN74LS367ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS367AN	Samples
SN74LS367ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS367AN	Samples
SN74LS367ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS367A	Samples
SN74LS367ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS367A	Samples
SN74LS368AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS368A	Samples
SN74LS368AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS368A	Samples
SN74LS368ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS368A	Samples
SN74LS368ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS368A	Samples
SN74LS368AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS368AN	Samples
SN74LS368AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS368AN	Samples
SN74LS368ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS368AN	Samples
SN74LS368ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS368AN	Samples
SN74LS368ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS368A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS368ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS368A	Samples
SNJ54LS365AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 365AFK	Samples
SNJ54LS365AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 365AFK	Samples
SNJ54LS365AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS365AJ	Samples
SNJ54LS365AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS365AJ	Samples
SNJ54LS366AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 366AFK	Samples
SNJ54LS366AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 366AFK	Samples
SNJ54LS366AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS366AJ	Samples
SNJ54LS366AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS366AJ	Samples
SNJ54LS367AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS367AJ	Samples
SNJ54LS367AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS367AJ	Samples
SNJ54LS368AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS368AJ	Samples
SNJ54LS368AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS368AJ	Samples
SNJ54LS368AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS368AW	Samples
SNJ54LS368AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS368AW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54LS365A, SN54LS367A, SN54LS368A, SN74LS365A, SN74LS367A, SN74LS368A :

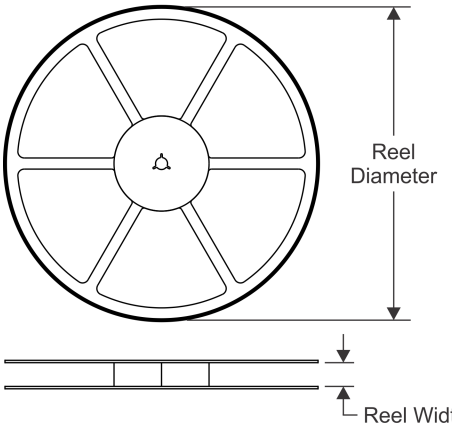
- Catalog: SN74LS365A, SN74LS367A, SN74LS368A
- Military: SN54LS365A, SN54LS367A, SN54LS368A

NOTE: Qualified Version Definitions:

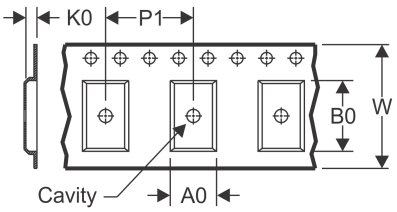
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

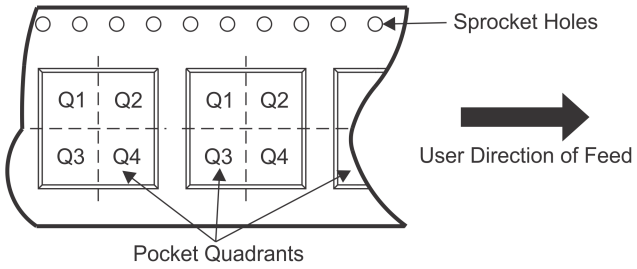


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

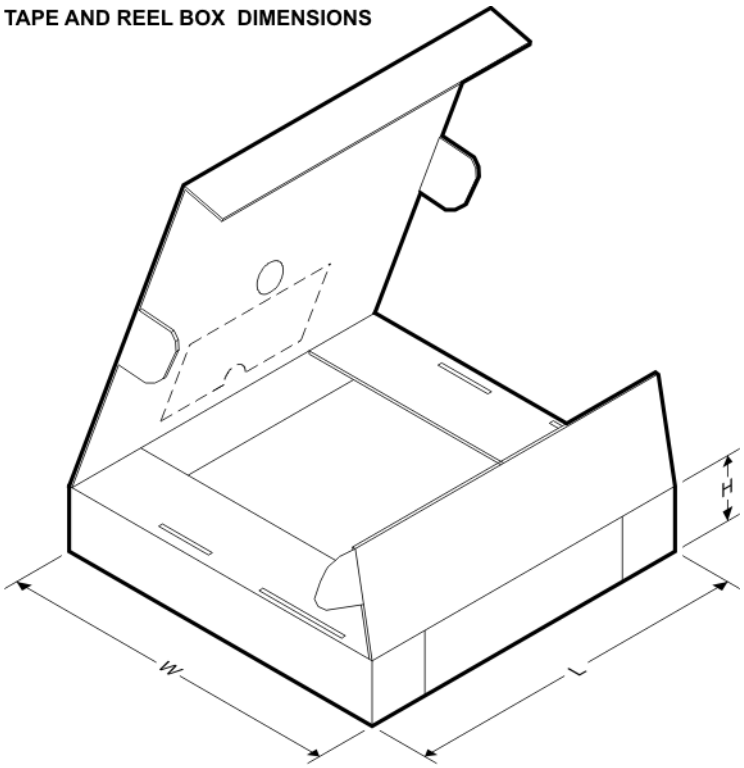
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS365ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS365ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS367ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS368ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

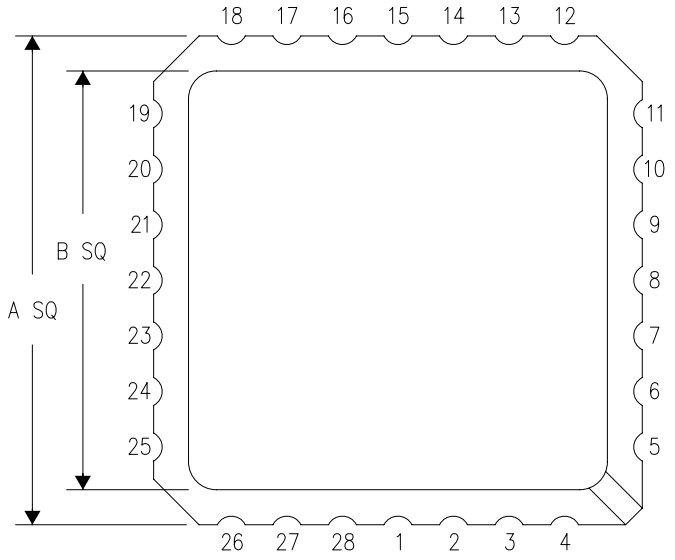


*All dimensions are nominal

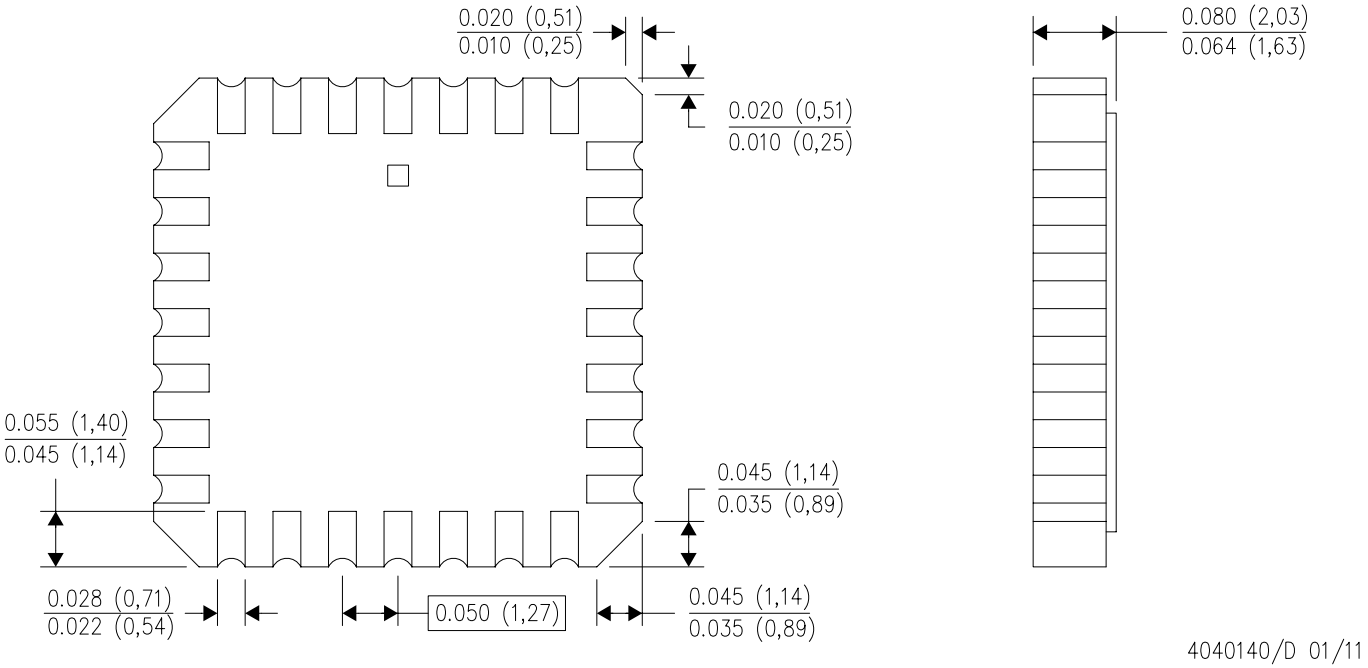
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS365ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS365ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LS367ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS368ANSR	SO	NS	16	2000	367.0	367.0	38.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



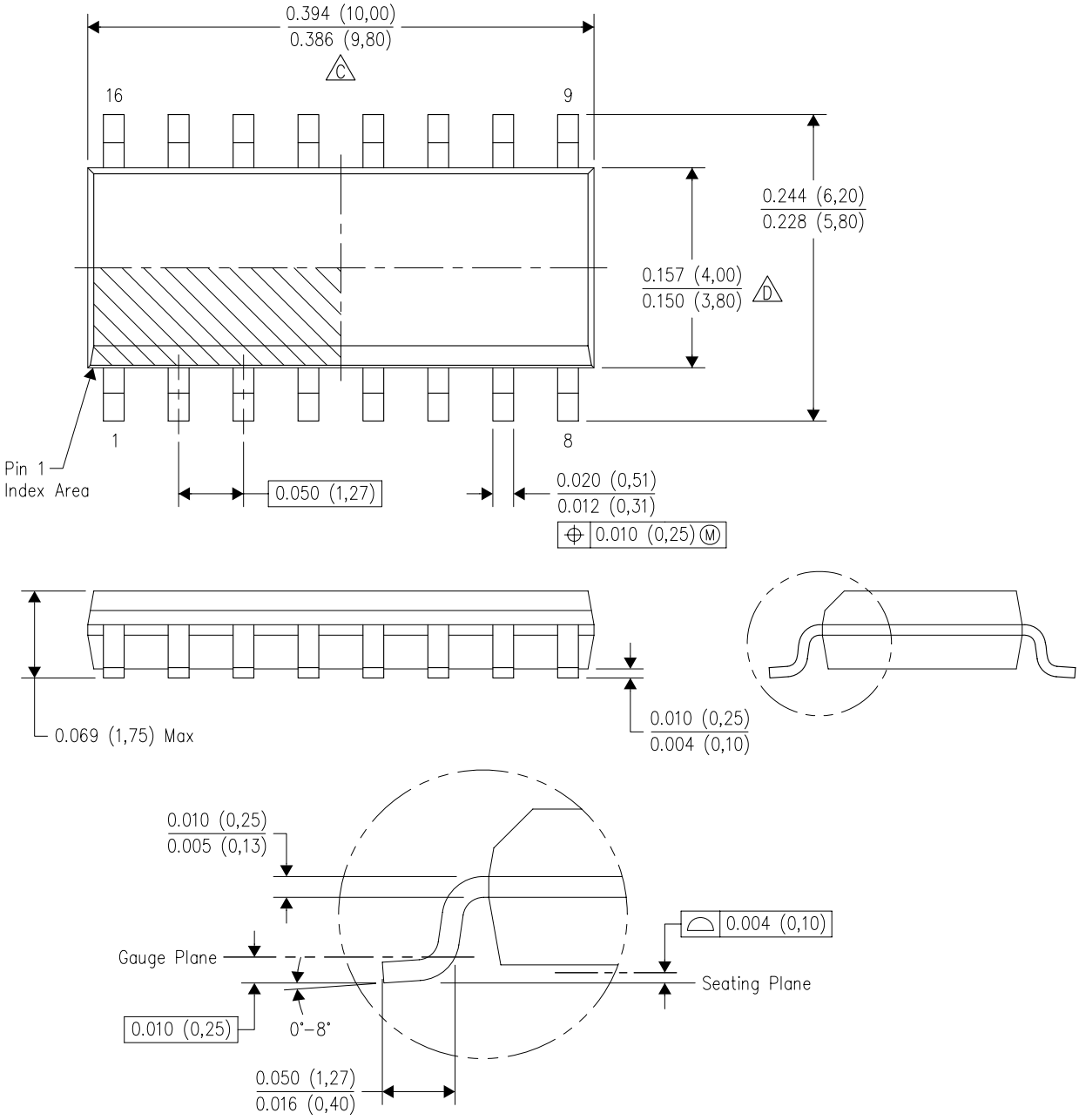
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

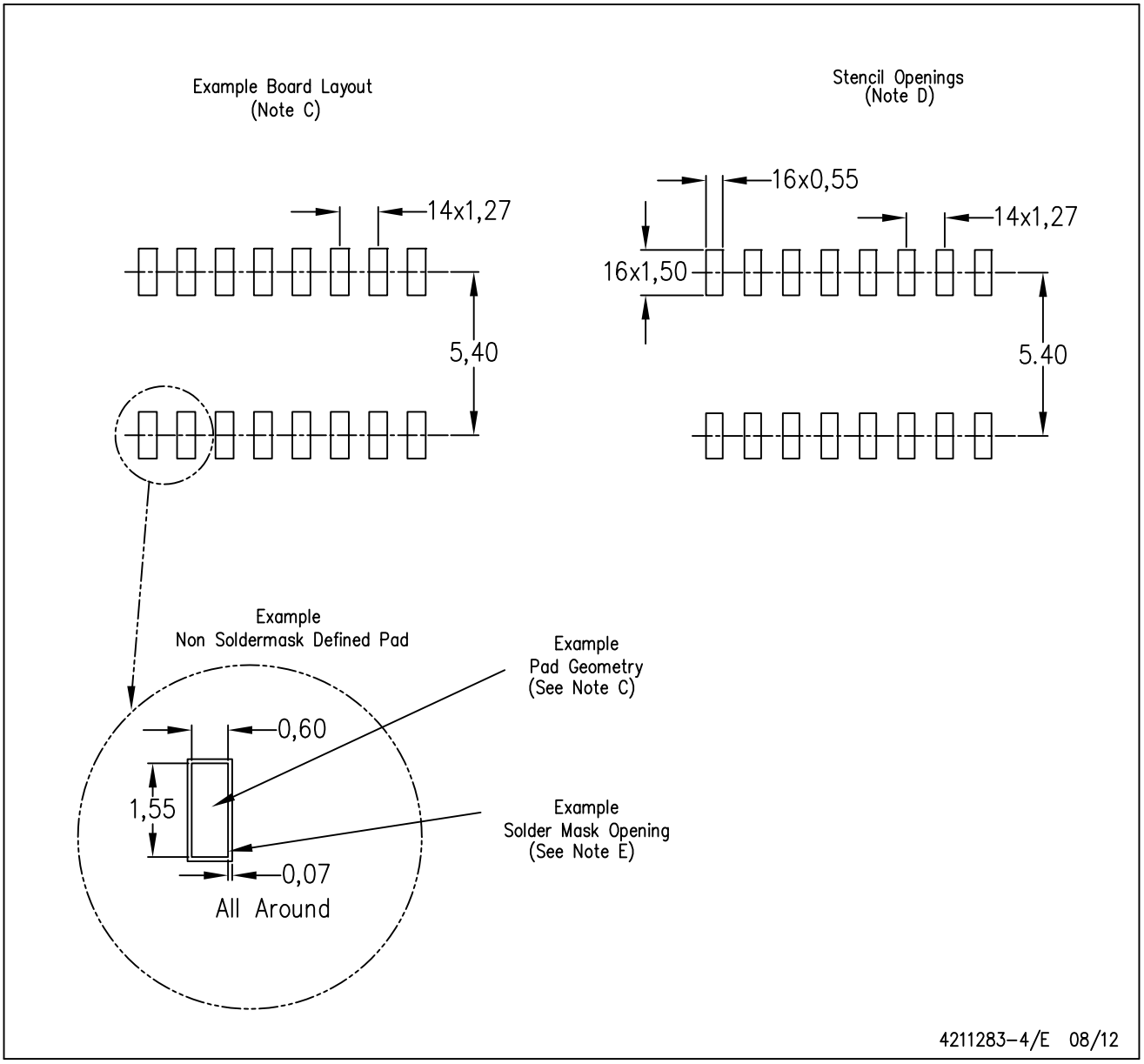
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

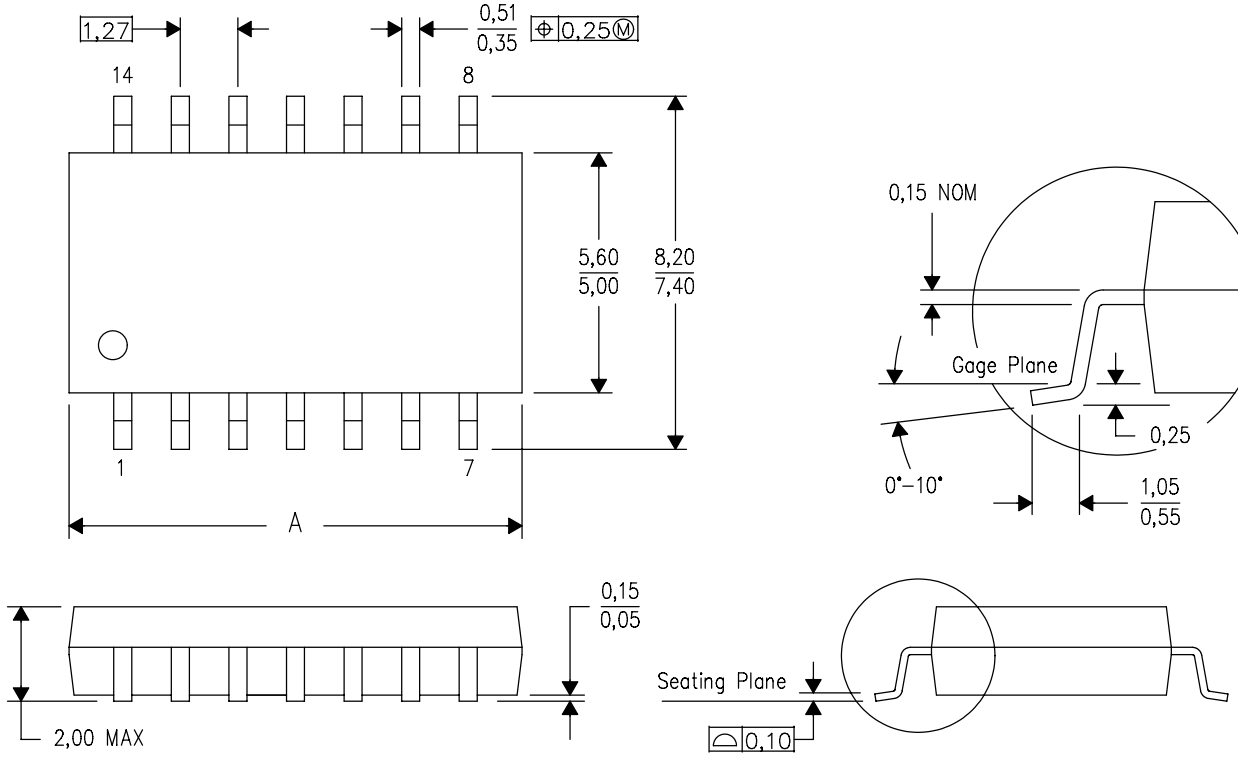


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

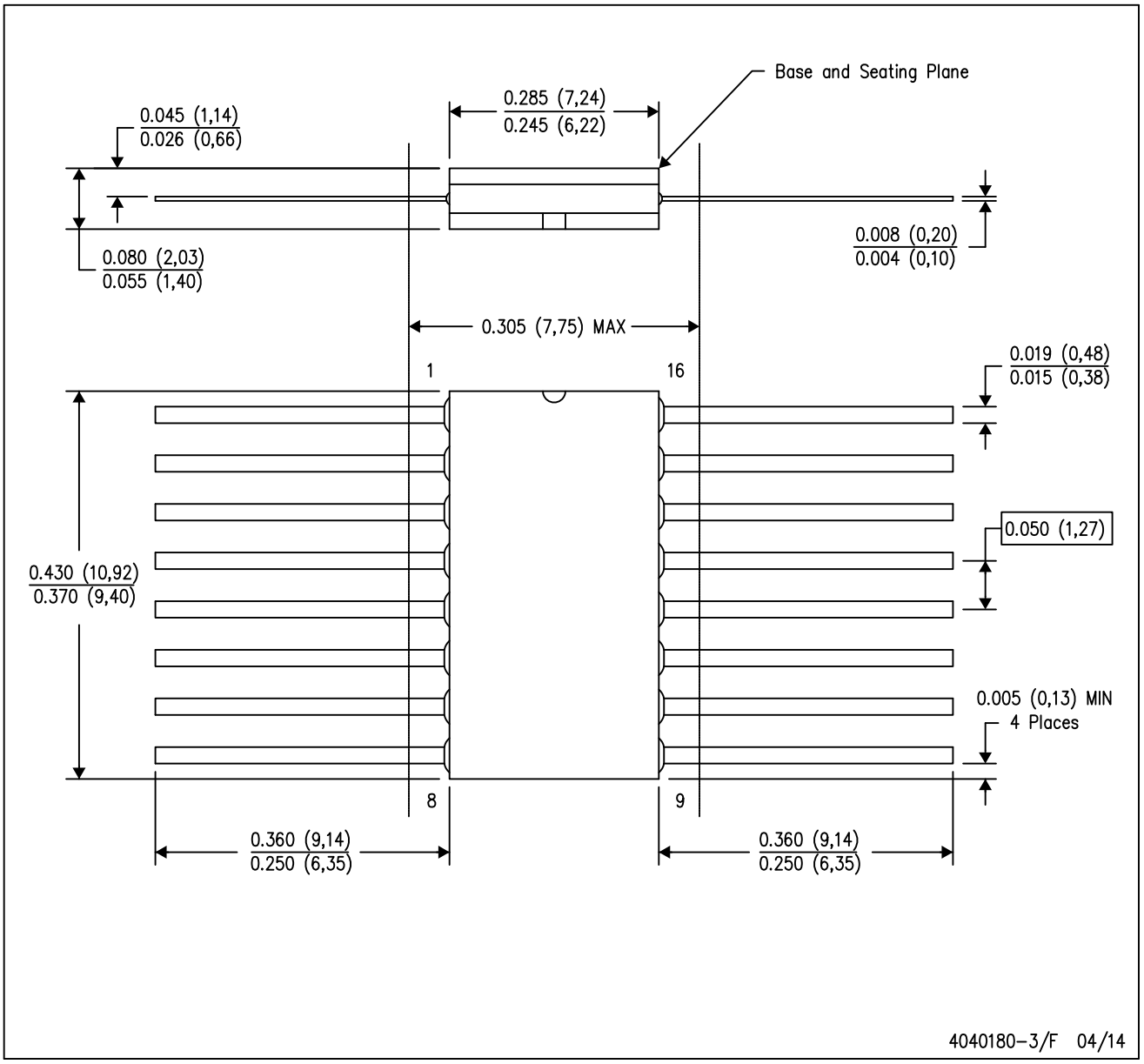


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK

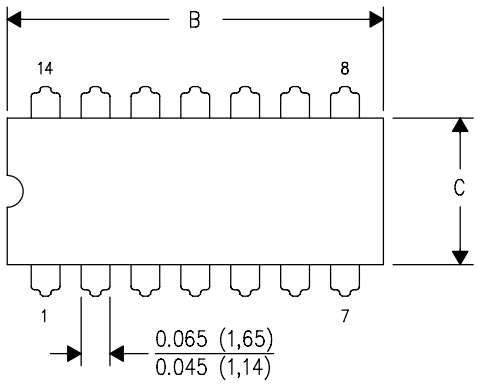


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

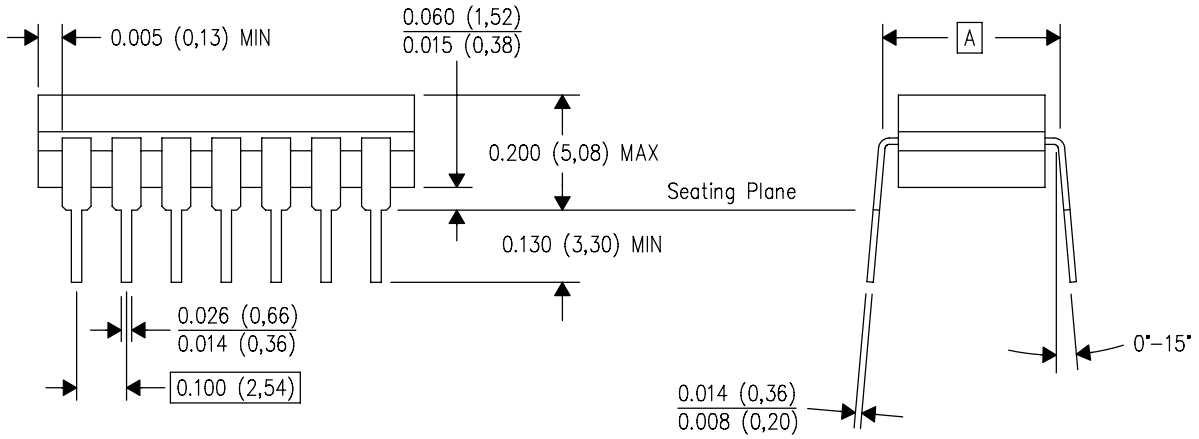
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



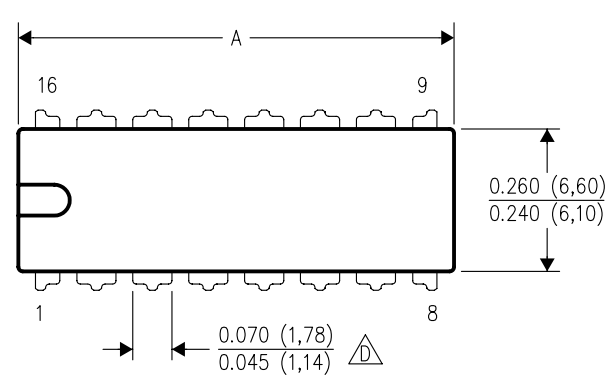
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

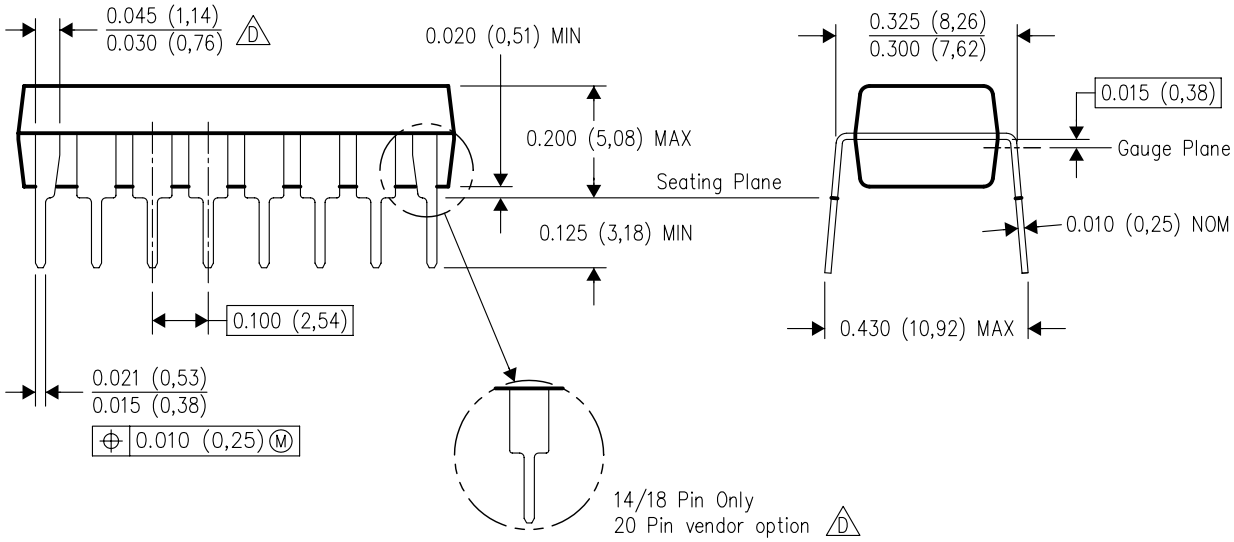
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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