



# SN74LV123A-Q1 Dual Retriggerable Monostable Multivibrator With Schmitt-Trigger Inputs

## 1 Features

- Qualified for Automotive Applications
- Typical  $V_{OLP}$  (Output Ground Bounce)  
<0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  
>2.3 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Voltage Operation on All Ports
- Schmitt-Trigger Circuitry on  $\overline{A}$ , B, and  $\overline{CLR}$  Inputs for Slow Input Transition Rates
- Edge Triggered From Active-High or Active-Low Gated Logic Inputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Retriggerable for Very Long Output Pulses, up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Glitch-Free Power-Up Reset on Outputs
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- Automotive
- Infotainment Systems
- DVD and Blu-ray Players
- GPS Navigation Devices
- Advanced Driver Assistance Systems
- Automotive Body and Lighting

## 3 Description

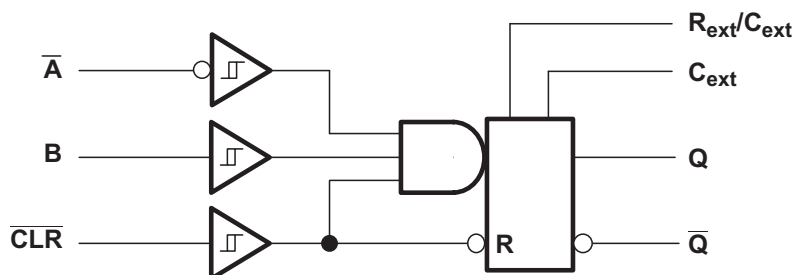
The SN74LV123A-Q1 device is a dual retriggerable monostable multivibrator designed for 2-V to 5.5-V  $V_{CC}$  operation.

**Device Information<sup>(1)</sup>**

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV123A-Q1	TSSOP (16)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Logic Diagram, Each Multivibrator (Positive Logic)**



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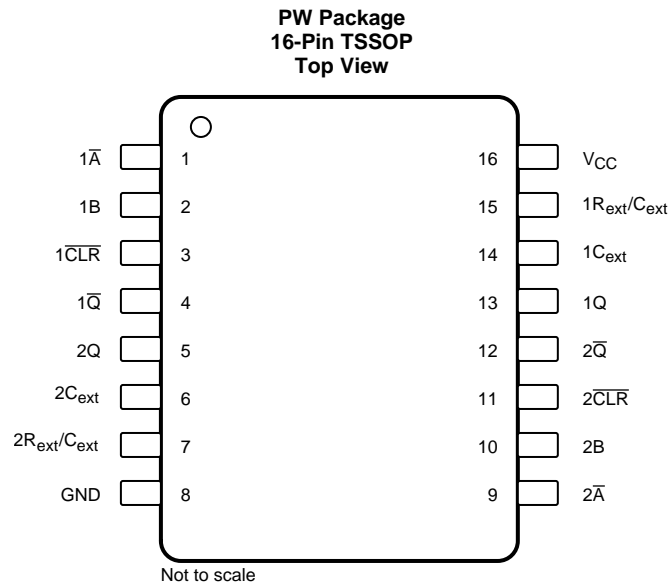
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (December 2012) to Revision F	Page
Deleted 200-V Machine Model (A115-A) from <i>Features</i> .....	1
Added 'Infotainment Systems' application. ....	1
Added 'DVD and Blu-ray Players' application. ....	1
Added 'GPS Navigation Devices' application. ....	1
Added 'Advanced Driver Assistance Systems' application. ....	1
Added 'Automotive Body and Lighting' application. ....	1
Updated the data sheet to meet the new TI data sheet standard .....	1
Deleted <i>Ordering Information</i> table from the data sheet .....	1
Moved extraneous description details to <i>Overview</i> section .....	1
Added <i>Device Information</i> table, <i>ESD Ratings</i> table, <i>Pin Configuration and Functions</i> section, <i>Detailed Description</i> section, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, <i>Receiving Notification of Documentation Updates</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
Added logic diagram for front page image .....	1
Added Operating virtual junction temperature, $T_J$ to <i>Absolute Maximum Ratings</i> table .....	4
Changed Maximum Operating free-air temperature from 105 to 125 .....	5

Changes from Revision D (April 2008) to Revision E	Page
Added <i>Thermal Information</i> table .....	5
Added <i>Caution</i> section describing power-down timing .....	11

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1 $\overline{A}$	I	Channel 1 falling edge trigger input when 1B = L; Hold low for other input methods
2	1B	I	Channel 1 rising edge trigger input when 1 $\overline{A}$ = H; Hold high for other input methods
3	1 $\overline{CLR}$	I	Channel 1 rising edge trigger when 1 $\overline{A}$ = H and 1B = L; Hold high for other input methods; Can cut pulse length short by driving low during output
4	1 $\overline{Q}$	O	Channel 1 inverted output
5	2Q	O	Channel 2 output
6	2C <sub>ext</sub>	—	Channel 2 external capacitor negative connection
7	2R <sub>ext</sub> /C <sub>ext</sub>	—	Channel 2 external capacitor and resistor junction connection
8	GND	—	Ground
9	2 $\overline{A}$	I	Channel 2 falling edge trigger input when 2B = L; Hold low for other input methods
10	2B	I	Channel 2 rising edge trigger input when 2 $\overline{A}$ = H; Hold high for other input methods
11	2 $\overline{CLR}$	I	Channel 2 rising edge trigger when 2 $\overline{A}$ = H and 2B = L; Hold high for other input methods; Can cut pulse length short by driving low during output
12	2 $\overline{Q}$	O	Channel 2 inverted output
13	1Q	O	Channel 1 output
14	1C <sub>ext</sub>	—	Channel 1 external capacitor negative connection
15	1R <sub>ext</sub> /C <sub>ext</sub>	—	Channel 1 external capacitor and resistor junction connection
16	V <sub>CC</sub>	—	Power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage, $V_{CC}$		−0.5	7	V
Input voltage, $V_I$ <sup>(2)</sup>		−0.5	7	V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ <sup>(2)</sup>		−0.5	7	V
Output voltage, $V_O$ $V_O$	In the high or low state <sup>(3)(2)</sup>	−0.5	$V_{CC} + 0.5$	V
	In the power-off state, $V_O$ <sup>(2)</sup>	−0.5	7	V
Input clamp current, $I_{IK}$	$V_I < 0$		−20	mA
Output clamp current, $I_{OK}$	$V_O < 0$		−50	mA
Continuous output current, $I_O$	$V_O = 0$ to $V_{CC}$		±25	mA
Continuous current through $V_{CC}$ or GND			±50	mA
Operating virtual junction temperature, $T_J$			150	°C
Storage temperature, $T_{stg}$		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value is limited to 5.5 V maximum.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$	
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$	
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.3$	
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.3$	
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	−50	μA
		$V_{CC} = 2.3$ V to 2.7 V	−2	mA
		$V_{CC} = 3$ V to 3.6 V	−6	
		$V_{CC} = 4.5$ V to 5.5 V	−12	

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

## Recommended Operating Conditions (continued)

over operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$	50	$\mu\text{A}$
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	2	mA
		$V_{CC} = 3\text{ V to } 3.6\text{ V}$	6	
		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$	12	
$R_{ext}$	External timing resistance	$V_{CC} = 2\text{ V}$	5	k $\Omega$
		$V_{CC} \geq 3\text{ V}$	1	
$C_{ext}$	External timing capacitance	No restriction		pF
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	1		ms/V
$T_A$	Operating free-air temperature	–40	125	$^{\circ}\text{C}$

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74LV123A-Q1	UNIT
		PW (TSSOP)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.2	$^{\circ}\text{C/W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.1	$^{\circ}\text{C/W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	56.3	$^{\circ}\text{C/W}$
$\Psi_{JT}$	Junction-to-top characterization parameter	5.6	$^{\circ}\text{C/W}$
$\Psi_{JB}$	Junction-to-board characterization parameter	55.7	$^{\circ}\text{C/W}$
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	$^{\circ}\text{C/W}$

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$V_{CC}$	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -50\text{ }\mu\text{A}$	2 V to 5.5 V	0.1			V
		$I_{OH} = -2\text{ mA}$	2.3 V	2			
		$I_{OH} = -6\text{ mA}$	3 V	2.48			
		$I_{OH} = -12\text{ mA}$	4.5 V	3.8			
$V_{OL}$	Low-level output voltage	$I_{OL} = 50\text{ }\mu\text{A}$	2 V to 5.5 V			0.1	V
		$I_{OL} = 2\text{ mA}$	2.3 V			0.4	
		$I_{OL} = 6\text{ mA}$	3 V			0.44	
		$I_{OL} = 12\text{ mA}$	4.5 V			0.55	
$I_I$	Input current	$R_{ext}/C_{ext}$ <sup>(1)</sup>	$V_I = 5.5\text{ V or GND}$	5.5 V		$\pm 2.5$	$\mu\text{A}$
		$\overline{A}$ , B, and $\overline{CLR}$	0 V			$\pm 1$	
			0 to 5.5 V			$\pm 1$	
$I_{CC}$	Quiescent current	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			20	$\mu\text{A}$
$I_{CC}$	Supply current, Active state (per circuit)	$V_I = V_{CC}$ or GND, $R_{ext}/C_{ext} = 0.5\text{ }V_{CC}$	3 V			280	$\mu\text{A}$
			4.5 V			650	
			5.5 V			975	
$I_{off}$	Off-state current	$V_I$ or $V_O = 0$ to 5.5 V	0 V			5	$\mu\text{A}$
$C_i$	Input capacitance	$V_I = V_{CC}$ or GND	3.3 V		1.9		pF
			5 V		1.9		

(1) This test is performed with the terminal in the off-state condition.

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## 6.6 Timing Requirements — $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted). See [Figure 1](#) and the circuits in the [Parameter Measurement Information](#) section.

			MIN	NOM <sup>(1)</sup>	MAX	UNIT
t <sub>w</sub>	Pulse duration	CLR	5			ns
		A or B trigger	5			
t <sub>rr</sub>	Pulse retrigger time, R <sub>ext</sub> = 1 kΩ	C <sub>ext</sub> = 100 pF	See <sup>(2)</sup>	76		ns
		C <sub>ext</sub> = 0.01 μF	See <sup>(2)</sup>	1.8		μs

(1)  $T_A = 25^\circ\text{C}$

(2) See retriggering data in the [Application and Implementation](#) section.

## 6.7 Timing Requirements — $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted). See [Figure 1](#) and the circuits in the [Parameter Measurement Information](#) section.

		MIN	NOM <sup>(1)</sup>	MAX	UNIT
t <sub>w</sub>	Pulse duration	$\overline{\text{CLR}}$			ns
		$\overline{\text{A}}$ or B trigger			
t <sub>rr</sub>	Pulse retrigger time, R <sub>ext</sub> = 1 kΩ	C <sub>ext</sub> = 100 pF	See <sup>(2)</sup>	59	ns
		C <sub>ext</sub> = 0.01 μF	See <sup>(2)</sup>	1.5	μs

(1)  $T_A = 25^\circ\text{C}$

(2) See retriggering data in the [Application and Implementation](#) section

## 6.8 Switching Characteristics — $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted). See the circuits in the [Parameter Measurement Information](#) section.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			$T_A = -40\text{ to }+125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	Propagation delay	$\overline{\text{A}}$ or B	Q or $\overline{\text{Q}}$	11.8	24.1		1	27.5	ns
		$\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	10.5	19.3		1	22	
		$\overline{\text{CLR}}$ trigger	Q or $\overline{\text{Q}}$	12.3	25.9		1	29.5	
$t_w$	Duration of pulse at Q and $\overline{\text{Q}}$ outputs	Q or $\overline{\text{Q}}$	$C_L = 50\text{ pF}$ $C_{ext} = 28\text{ pF}$ $R_{ext} = 2\text{ k}\Omega$	182	240			300	ns
			$C_L = 50\text{ pF}$ $C_{ext} = 0.01\text{ }\mu\text{F}$ $R_{ext} = 10\text{ k}\Omega$	90	100	110	90	110	$\mu\text{s}$
			$C_L = 50\text{ pF}$ $C_{ext} = 0.1\text{ }\mu\text{F}$ $R_{ext} = 10\text{ k}\Omega$	0.9	1	1.1	0.9	1.1	ms
$\Delta t_w$	Output pulse-duration variation (Q and $\overline{\text{Q}}$ ) between circuits in same package		$C_L = 50\text{ pF}$	$\pm 1\%$					

## 6.9 Switching Characteristics — $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

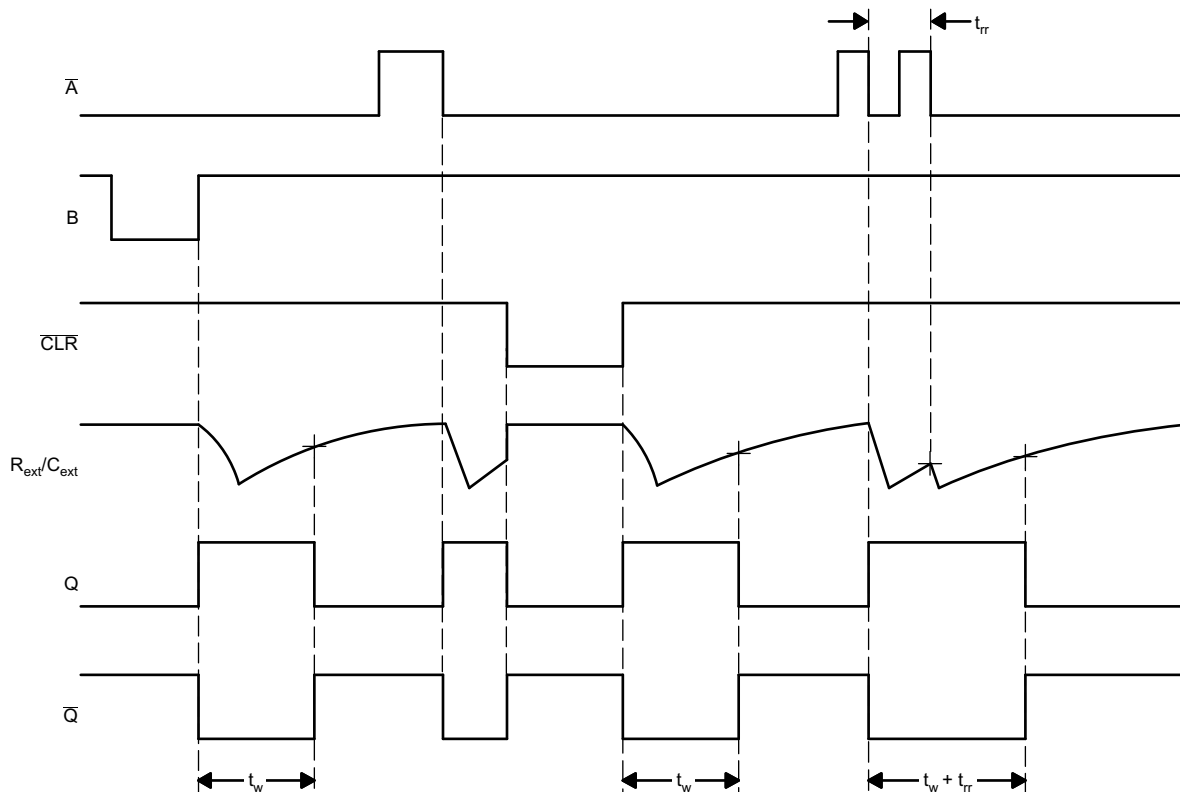
over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted). See the circuits in the [Parameter Measurement Information](#) section.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			$T_A = -40\text{ to }+125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$ Propagation delay	$\overline{A}$ or B	Q or $\overline{Q}$	$C_L = 50\text{ pF}$	8.3	14		1	16	ns
	$\overline{CLR}$	Q or $\overline{Q}$		7.4	11.4		1	13	
	$\overline{CLR}$ trigger	Q or $\overline{Q}$		8.7	14.9		1	17	
$t_w$ Duration of pulse at Q and $\overline{Q}$ outputs		Q or $\overline{Q}$	$C_L = 50\text{ pF}$ $C_{ext} = 28\text{ pF}$ $R_{ext} = 2\text{ k}\Omega$	167	200			240	ns
			$C_L = 50\text{ pF}$ $C_{ext} = 0.01\text{ }\mu\text{F}$ $R_{ext} = 10\text{ k}\Omega$	90	100	110	90	110	$\mu\text{s}$
			$C_L = 50\text{ pF}$ $C_{ext} = 0.1\text{ }\mu\text{F}$ $R_{ext} = 10\text{ k}\Omega$	0.9	1	1.1	0.9	1.1	ms
$\Delta t_w$ Output pulse-duration variation (Q and $\overline{Q}$ ) between circuits in same package			$C_L = 50\text{ pF}$	$\pm 1\%$					

## 6.10 Operating Characteristics

 $T_A = 25^\circ\text{C}$ 

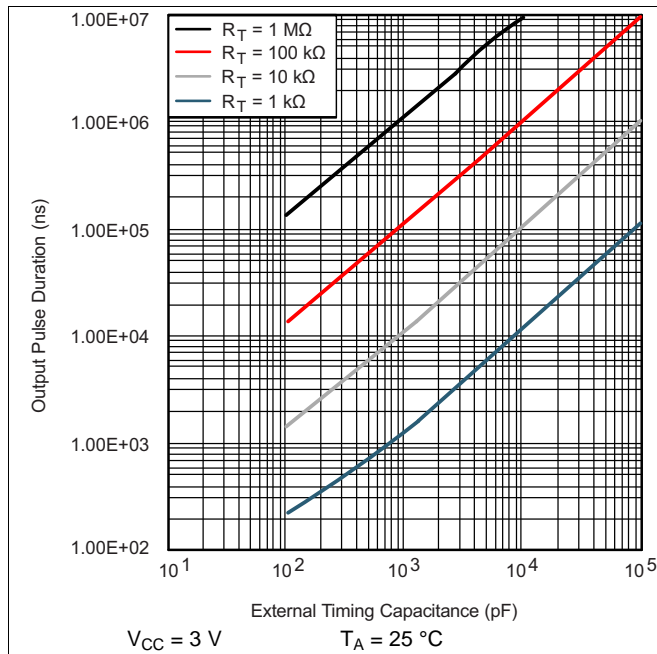
PARAMETER		TEST CONDITIONS		$V_{CC}$	TYP	UNIT
$C_{pd}$ Power dissipation capacitance		$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$		3.3 V	44	pF
				5 V	49	



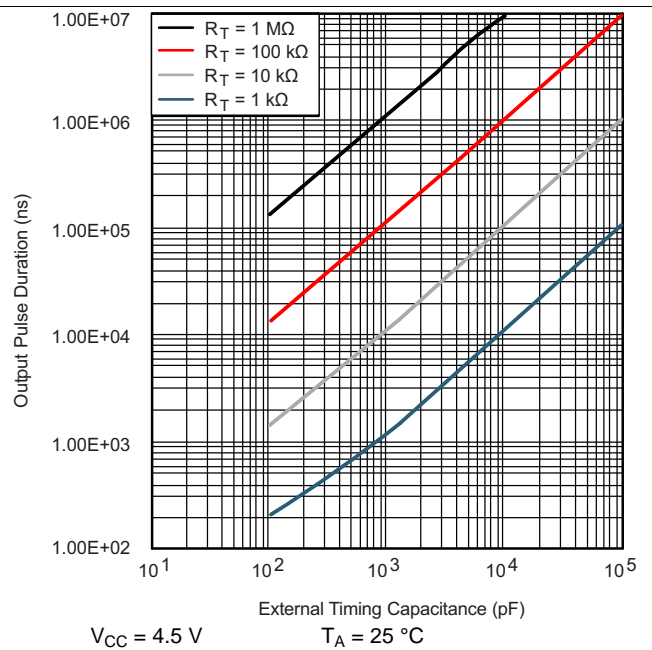
**Figure 1. Input and Output (I/O) Timing Diagram**

## 6.11 Typical Characteristics

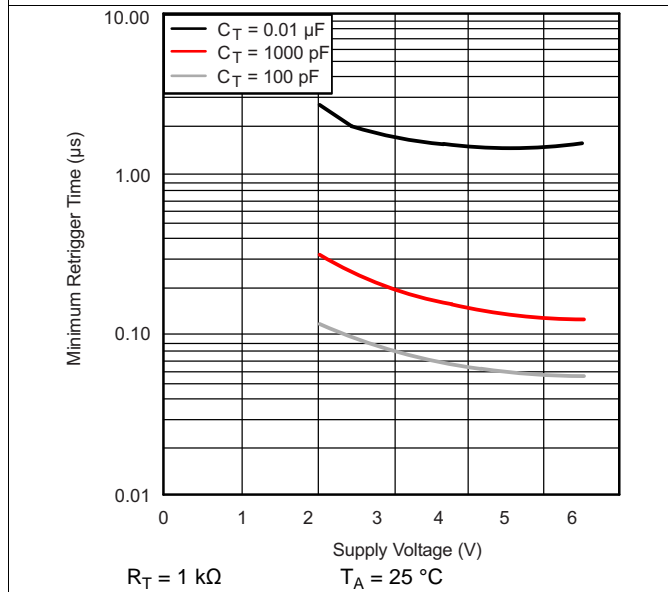
Operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied.



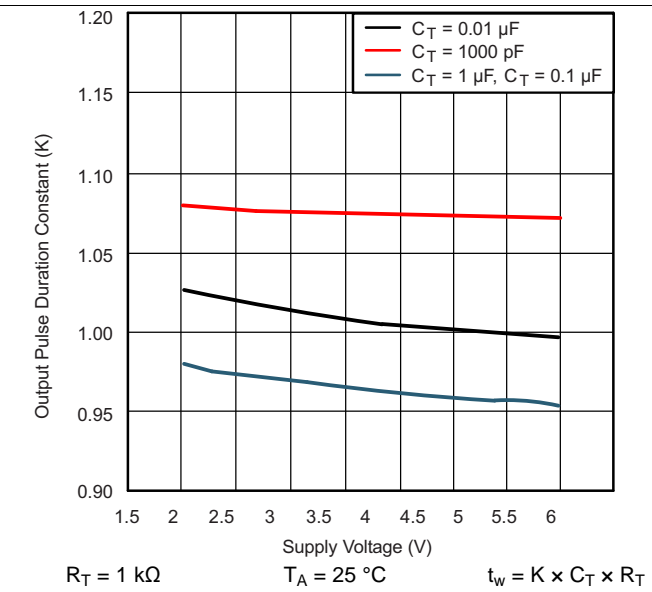
**Figure 2. Output Pulse Duration ( $t_w$ ) vs External Timing Capacitance ( $C_T$ )**



**Figure 3. Output Pulse Duration vs External Timing Capacitance**



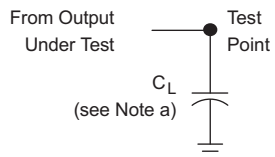
**Figure 4. Minimum Trigger Time ( $t_{tr}$ ) vs  $V_{CC}$  Characteristics**



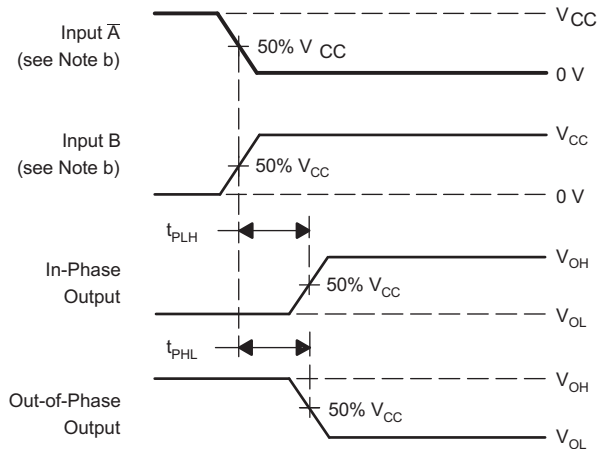
**Figure 5. Output Pulse-Duration Constant vs Supply Voltage**



## 7 Parameter Measurement Information

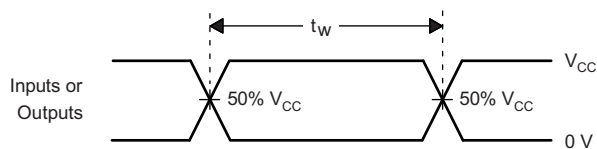


**Figure 6. Load Circuit**

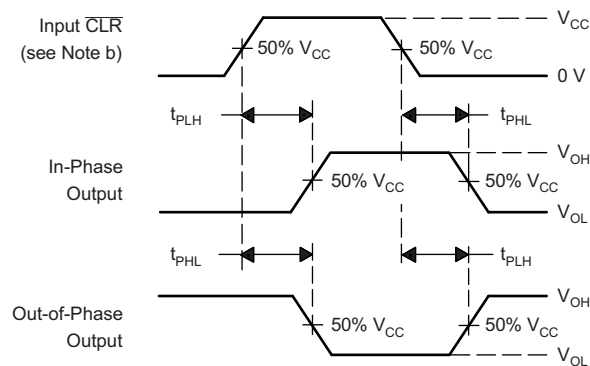


**Figure 8. Voltage Waveforms Delay Times**

- $C_L$  includes probe and jig capacitance.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .
- The outputs are measured one at a time, with one input transition per measurement.



**Figure 7. Voltage Waveforms Pulse Duration**



**Figure 9. Voltage Waveforms Delay Times**

## 8 Detailed Description

### 8.1 Overview

This edge-triggered multivibrator features output pulse-duration control by three methods. In the first method, the  $\overline{A}$  input is low, and the B input goes high. In the second method, the B input is high, and the  $\overline{A}$  input goes low. In the third method, the  $\overline{A}$  input is low, the B input is high, and the clear ( $\overline{CLR}$ ) input goes high.

The output pulse duration is programmable by selecting external resistance and capacitance values. The external timing capacitor must be connected between  $C_{ext}$  and  $R_{ext}/C_{ext}$  (positive) and an external resistor connected between  $R_{ext}/C_{ext}$  and  $V_{CC}$ . Connect an external variable resistance between  $R_{ext}/C_{ext}$  and  $V_{CC}$  to obtain variable pulse durations. The output pulse duration also can be reduced by taking  $\overline{CLR}$  low.

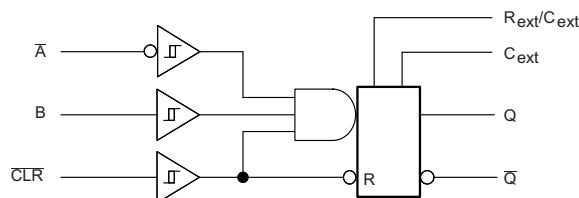
Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The  $\overline{A}$ , B, and  $\overline{CLR}$  inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

When triggered, the basic pulse duration can be extended by retriggering the gated low-level-active ( $\overline{A}$ ) or high-level-active (B) input. Pulse duration may be reduced by taking  $\overline{CLR}$  low. The input-output timing diagram (Figure 1) shows pulse control by retriggering the inputs and early clearing.

The Q outputs are in the low state, and the  $\overline{Q}$  outputs are in the high state during power up. The outputs are glitch free, without applying a reset pulse.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, which prevents damaging current backflow through the device when it is powered down.

### 8.2 Functional Block Diagram



**Figure 10. Logic Diagram, Each Multivibrator (Positive Logic)**

### 8.3 Feature Description

The SN74LV123A operates over a wide supply range from 2 V to 5.5 V. The propagation delay has a maximum of 11 ns at 5-V supply. The typical output ground bounce is less than 0.8 V at 3.3-V supply and 25°C. The typical output  $V_{OH}$  undershoot is greater than 2.3 V at 3.3-V supply and 25°C.

These parts support mixed-mode voltage operation on all ports.

Schmitt-trigger circuitry on the  $\overline{A}$ , B, and  $\overline{CLR}$  inputs allow for slow input transition rates and noisy input signals.

This device can be configured for rising or falling edge triggering.

This device supports partial-power-down mode operation.

This device is retriggerable for very long output pulses up to 100% duty cycle.

The clear signal overrides an output pulse and terminates it early.

Glitch-free power-up reset on outputs.

## Feature Description (continued)







### 8.3.1 Power-Down Considerations

Large values of  $C_{ext}$  can cause problems when powering down the SN74LV123A-Q1 devices because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor can discharge from  $V_{CC}$  through the protection diodes at pin 2 or pin 14. Current through the input protection diodes must be limited to 30 mA; therefore, the turn-off time of the  $V_{CC}$  power supply must not be faster than  $t = V_{CC} \times C_{ext} / 30 \text{ mA}$ . For example, if  $V_{CC} = 5 \text{ V}$  and  $C_{ext} = 15 \text{ pF}$ , the  $V_{CC}$  supply must turn off no faster than  $t = (5 \text{ V}) \times (15 \text{ pF}) / 30 \text{ mA} = 2.5 \text{ ns}$ . Usually, this is not a problem because power supplies are heavily filtered and cannot discharge at this rate. The SN74LV123A-Q1 devices can sustain damage when a more rapid decrease of  $V_{CC}$  to zero occurs. Use external clamping diodes to avoid this possibility.

## 8.4 Device Functional Modes

Table 1 shows the functional modes for each monostable multivibrator in the SN74LV123A-Q1.

**Table 1. Function Table  
(Each Multivibrator)**

INPUTS			OUTPUTS	
$\overline{\text{CLR}}$	$\overline{\text{A}}$	B	Q	$\overline{\text{Q}}$
L	X	X	L	H
X	H	X	L <sup>(1)</sup>	H <sup>(1)</sup>
X	X	L	L <sup>(1)</sup>	H <sup>(1)</sup>
H	L	↑		
H	↓	H		
↑	L	H		

- (1) These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

## 9 Application and Implementation

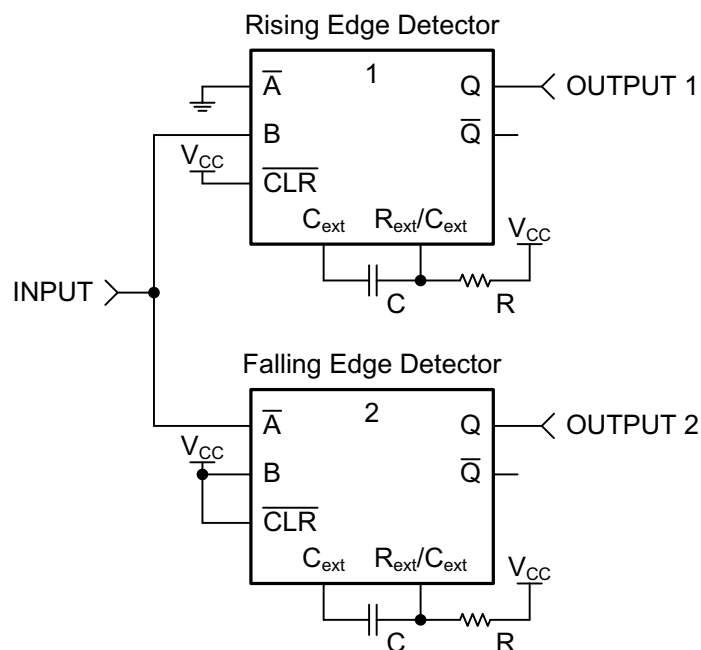
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SNx4LV123A device is a dual monostable multivibrator. It can be configured for many pulse width outputs and rising or falling-edge triggering. The application shown here could be used to signal separate interruptable inputs on a microcontroller when an input had a rising or falling edge.

### 9.2 Typical Application



**Figure 11. Simplified Application Schematic**

#### 9.2.1 Design Requirements

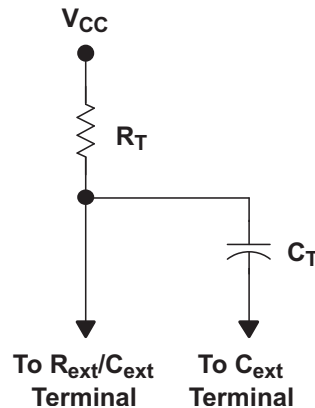
### NOTE

To prevent malfunctions due to noise, connect a high-frequency capacitor between  $V_{CC}$  and GND, and keep the wiring between the external components and  $C_{ext}$  and  $R_{ext}/C_{ext}$  terminals as short as possible.

##### 9.2.1.1 Output Pulse Duration

The output pulse duration,  $t_w$ , is determined primarily by the values of the external capacitance ( $C_T$ ) and timing resistance ( $R_T$ ). The timing components are connected as shown in [Figure 12](#).

## Typical Application (continued)



**Figure 12. Timing-Component Connections**

If  $C_T$  is  $\geq 1000$  pF and  $K = 1.0$ , the pulse duration is given by [Equation 1](#):

$$t_w = K \times R_T \times C_T$$

where

- $t_w$  = pulse duration in ns
- $R_T$  = external timing resistance in k $\Omega$
- $C_T$  = external capacitance in pF
- $K$  = multiplier factor

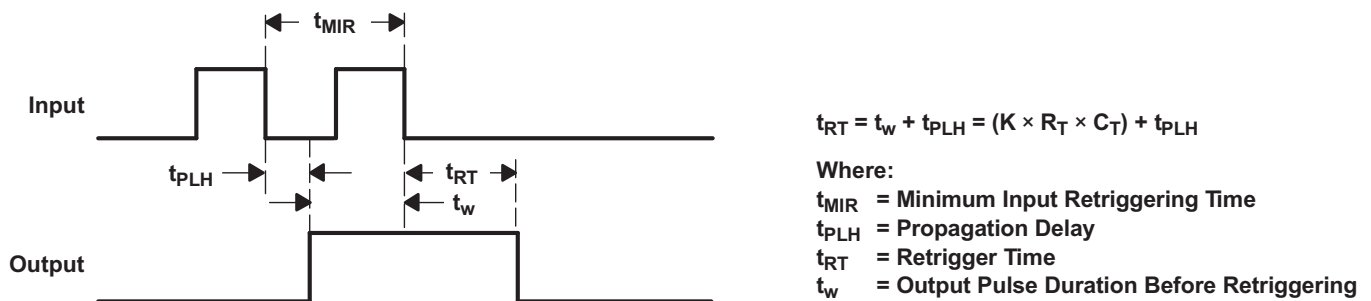
(1)

if  $C_T$  is  $< 1000$  pF,  $K$  can be determined from [Figure 5](#)

[Equation 1](#) and [Figure 16](#) can be used to determine values for pulse duration, external resistance, and external capacitance.

### 9.2.1.2 Retriggering Data

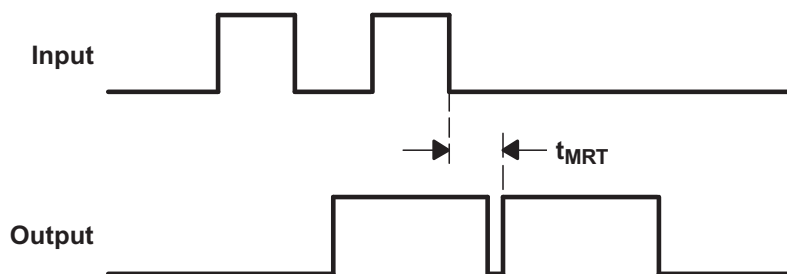
The minimum input retriggering time ( $t_{MIR}$ ) is the minimum time required after the initial signal before retriggering the input. After  $t_{MIR}$ , the device retriggers the output. Experimentally, it also can be shown that to retrigger the output pulse, the two adjacent input signals must be  $t_{MIR}$  apart, where  $t_{MIR} = 0.30 \times t_w$ . The retrigger pulse duration is calculated as shown in [Figure 13](#).



**Figure 13. Retrigger Pulse Duration**

The minimum value from the end of the input pulse to the beginning of the retriggered output must be approximately 15 ns to ensure a retriggered output (see [Figure 14](#)).

## Typical Application (continued)



$t_{MRT}$  = Minimum Time Between the End of the Second Input Pulse and the Beginning of the Retriggered Output

$t_{MRT} = 15 \text{ ns}$

**Figure 14. Input and Output Requirements**

### 9.2.2 Detailed Design Procedure

- Timing requirements:
  - The pulse width must be long enough to be read by the desired output system, but short enough so that the output pulse completes prior to the next trigger event. It is recommended to make the output pulse just 10% longer than the minimum required for the output system.
- Recommended input conditions:
  - Slow or noisy inputs are allowed on  $\overline{A}$ , B, and  $\overline{CLR}$  due to Schmitt-trigger input circuitry.
  - Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in [Recommended Operating Conditions](#).
- Recommended output conditions:
  - Load currents must not exceed the values listed in [Absolute Maximum Ratings](#).

## Typical Application (continued)

### 9.2.3 Application Curves

Operation of the devices at these or any other conditions beyond those indicated under <sup>(1)</sup> is not implied.

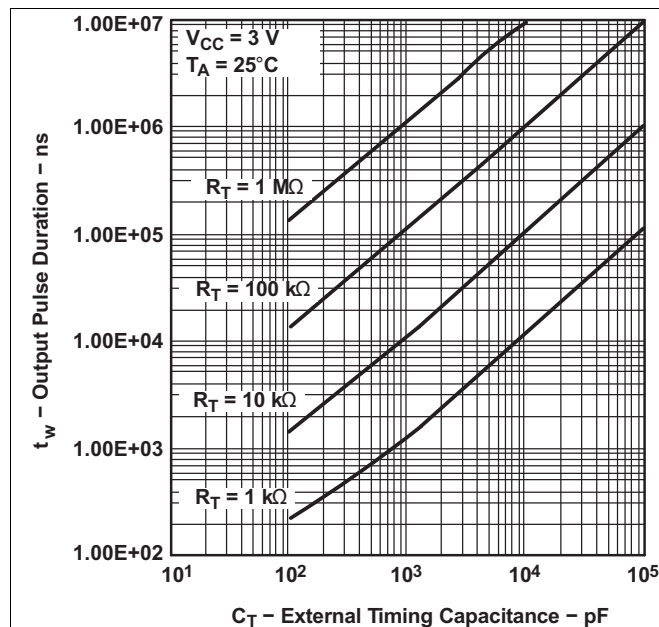


Figure 15. Output Pulse Duration vs. External Timing Capacitance

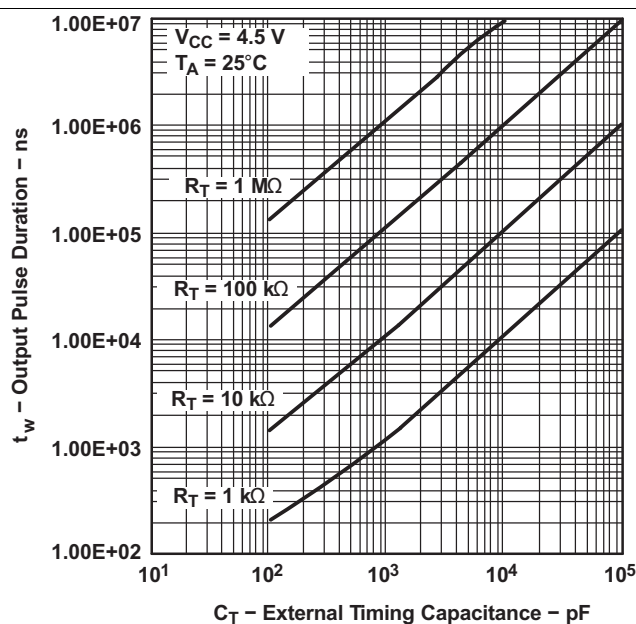


Figure 16. Output Pulse Duration vs. External Timing Capacitance

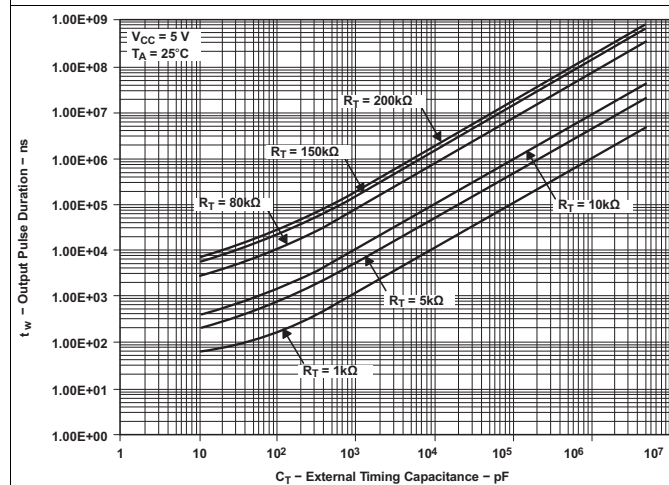


Figure 17. Output Pulse Duration vs External Timing Capacitance

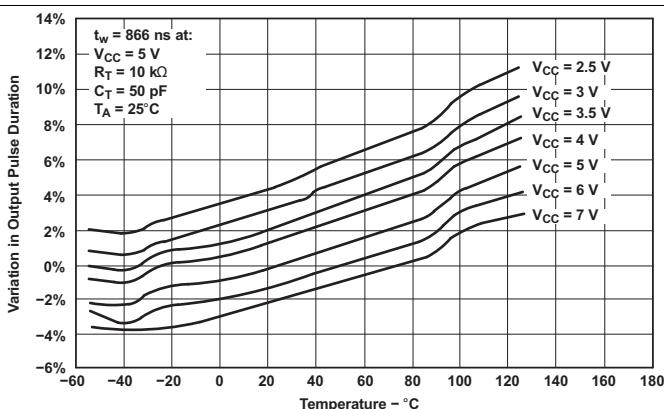


Figure 18. Variations in Output Pulse Duration vs Temperature

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

## 10 Power Supply Recommendations

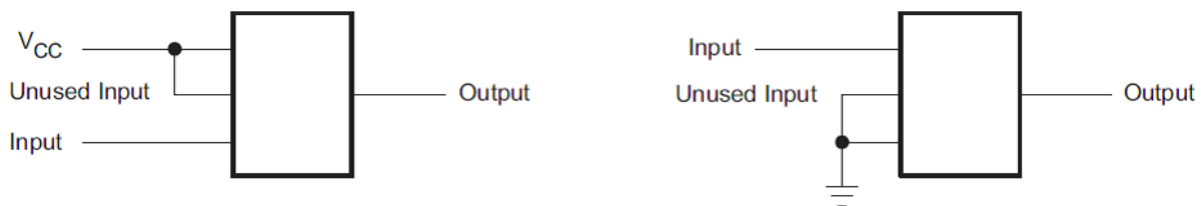
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) . Each  $V_{CC}$  terminal must have a good bypass capacitor to prevent power disturbance. TI recommends a 0.1- $\mu$ F capacitor for devices with a single supply. If there are multiple  $V_{CC}$  terminals, then TI recommends a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

## 11 Layout

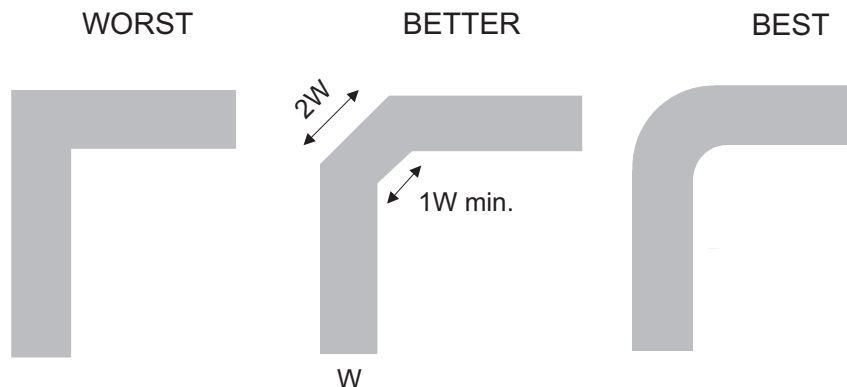
### 11.1 Layout Guidelines

Inputs must never float when using multiple bit logic devices. In many cases, functions or parts of functions of digital logic devices are unused. For example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever makes more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver.

### 11.2 Layout Example



**Figure 19. Layout Recommendation**



**Figure 20. Trace Example**



## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV123ATPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123AQ	<a href="#">Samples</a>
SN74LV123ATPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV123AQ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LV123A-Q1 :**

- Catalog : [SN74LV123A](#)
- Enhanced Product : [SN74LV123A-EP](#)

**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV123ATPW RG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV123ATPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV123ATPWRG4Q1	TSSOP	PW	16	2000	853.0	449.0	35.0
SN74LV123ATPWRQ1	TSSOP	PW	16	2000	853.0	449.0	35.0



4220204/A 02/2017

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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