SN74LVC112A Dual Negative-Edge-Triggered J-K Flip-Flop With Clear And Preset

1 Features

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.8 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 3000-V Human-Body Model
  - 200-V Machine Model
  - 1500-V Charged-Device Model

2 Applications

- Servers
- PCs
- Notebooks
- Network switches
- Toys
- I/O Expanders
- Electronic Points of Sale

3 Description

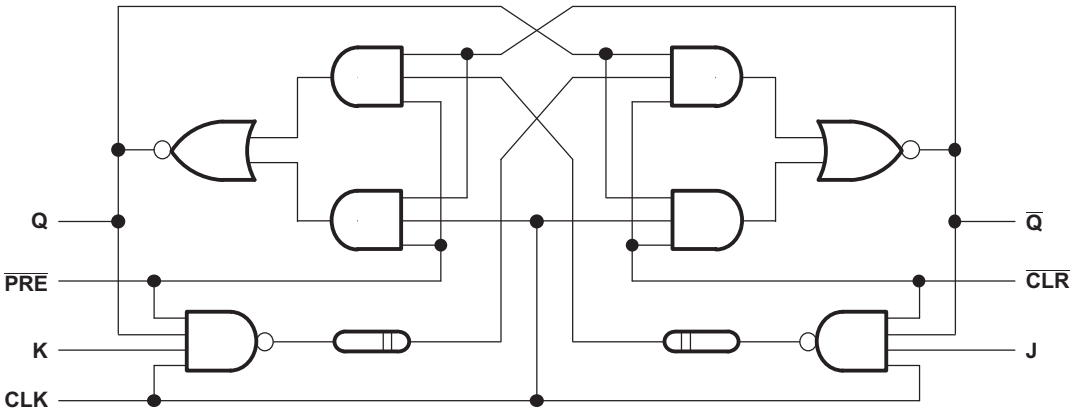
This dual negative-edge-triggered J-K flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC112A	SSOP (16)	6.50 mm x 5.30 mm
	TSSOP (16)	5.00 mm x 4.40 mm
	TVSOP (16)	3.60 mm x 4.40 mm
	SOP (16)	10.20 mm x 5.30 mm
	SOIC (16)	9.00 mm x 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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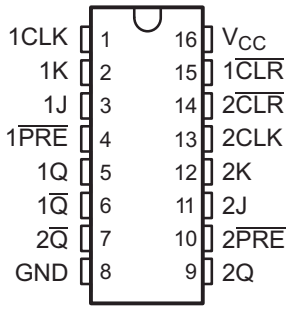
5 Revision History

Changes from Revision L (August 2004) to Revision M **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table. ... 1
- Changed MAX operating temperature to 125°C in *Recommended Operating Conditions* table. ... 5
- Added –40°C to 125°C temperature range to *Electrical Specifications* table. ... 6
- Added *Timing Requirements* table for –40°C to 125°C temperature range. ... 6
- Added *Switching Characteristics* table for –40°C to 125°C temperature range. ... 7

6 Pin Configuration and Functions

D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	1CLK	I	1 Clock
2	1K	I	1K Input
3	1J	I	1J Input
4	1$\overline{\text{PRE}}$	I	1 Preset
5	1Q	O	1Q Output. Pull low to set 1Q high and 1$\overline{\text{Q}}$ low upon power-up.
6	1$\overline{\text{Q}}$	O	1$\overline{\text{Q}}$ Output
7	2$\overline{\text{Q}}$	O	2$\overline{\text{Q}}$ Output
8	GND	—	Ground Pin
9	2Q	O	2Q Output
10	2$\overline{\text{PRE}}$	I	2 Preset
11	2J	I	2J Input. Pull low to set 2Q high and 2$\overline{\text{Q}}$ low upon power-up.
12	2K	I	2K Input
13	2CLK	I	2 Clock
14	2$\overline{\text{CLR}}$	I	2 Clear
15	1$\overline{\text{CLR}}$	I	1 Clear. Pull low to set 2Q low and 2$\overline{\text{Q}}$ high upon power-up.
16	V_{CC}	—	Power Pin. Pull low to set 1Q low and 1$\overline{\text{Q}}$ high upon power-up.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)		–0.5	6.5	V
V_O	Output voltage range(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

7.4 Thermal Information

THERMAL METRIC(1)		SN74LVC112A					UNIT
		D	DB	DGV	NS	PW	
		24 PINS					
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.6	107.1	129.0	90.7	122.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.9	59.6	52.1	48.3	51.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	44.8	54.4	62.0	49.4	64.4	
ψ_{JT}	Junction-to-top characterization parameter	14.7	20.5	6.5	14.6	6.7	
ψ_{JB}	Junction-to-board characterization parameter	44.5	53.8	61.3	49.1	63.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	TYP(1)	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –100 µA	1.65 V to 3.6 V	V_{CC} – 0.2			V_{CC} – 0.2		V_{CC} – 0.2		V
	I_{OH} = –4 mA	1.65 V	1.2			1.2		1.2		
	I_{OH} = –8 mA	2.3 V	1.7			1.7		1.7		
	I_{OH} = –12 mA	2.7 V	2.2			2.2		2.2		
		3 V	2.4			2.4		2.4		
	I_{OH} = –24 mA	3 V	2.2			2.2		2.2		
V_{OL}	I_{OL} = 100 µA	1.65 V to 3.6 V			0.2		0.2		0.2	V
	I_{OL} = 4 mA	1.65 V			0.45		0.45		0.45	
	I_{OL} = 8 mA	2.3 V			0.7		0.7		0.7	
	I_{OL} = 12 mA	2.7 V			0.4		0.4		0.4	
	I_{OL} = 24 mA	3 V			0.55		0.55		0.55	
I_I	V_I = 5.5 V or GND	3.6 V			±5		±5		±5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			10		10		10	µA
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500		500		500	µA
C_i	V_I = V_{CC} or GND	3.3 V		4.5						pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

7.6 Timing Requirements, –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			120		150		150		150	MHz
t_w	Pulse duration, CLK high or low		4.2		3.3		3.3		3.3		ns
t_{su}	Setup time	Data before CLK↓	5.8		3.2		3.1		2.3		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	5		2.8		2.4		1.1		
t_h	Hold time, data after CLK↓		6.2		4.4		2.5		0.7		ns

7.7 Timing Requirements, –40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			120		150		150		150	MHz
t_w	Pulse duration, CLK high or low		4.1		3.3		3.3		3.3		ns
t_{su}	Setup time	Data before CLK↓	6		3.2		3.1		2.3		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	5		2.8		2.4		1.1		
t_h	Hold time, data after CLK↓		6.2		4.7		2.5		0.7		ns

7.8 Switching Characteristics, –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	TYP	MAX	
f_{max}			150		150		150		150			MHz
t_{pd}	$\overline{CLR}$ or $\overline{PRE}$	Q or $\overline{Q}$		5.9		4.1		5.5	1	3.4	4.8	ns
	CLK			5.6		4		7.1	1	3.5	5.9	

7.9 Switching Characteristics, –40°C to 125°C

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	TYP	MAX	
f_{max}			120		150		150		150			MHz
t_{pd}	$\overline{CLR}$ or $\overline{PRE}$	Q or $\overline{Q}$		6.2		4		6	1	3.4	5.3	ns
	CLK			6.2		4.1		7.6	1	3.5	6.4	

7.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	See (1)	See (1)	24	pF

(1) This information was not available at the time of publication.

7.11 Typical Characteristics

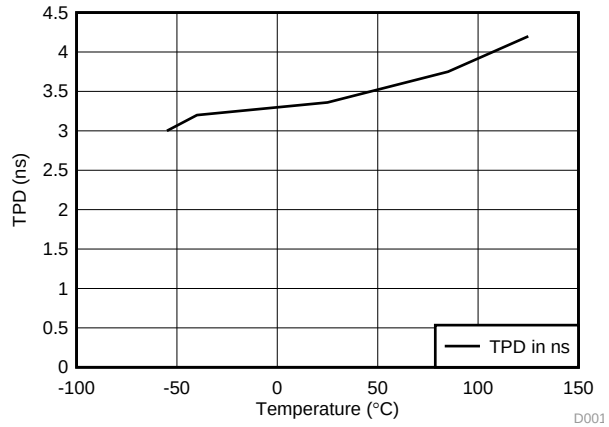


Figure 1. TPD vs Temperature

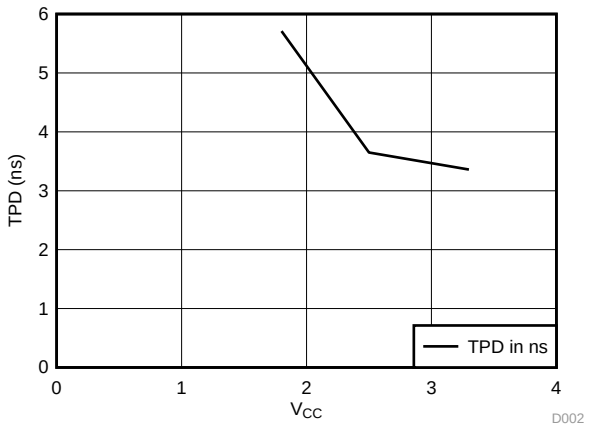
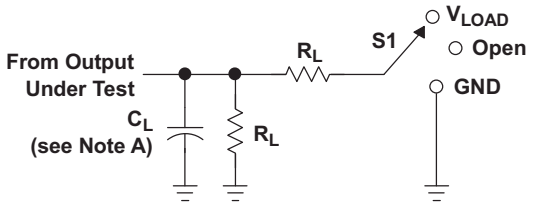


Figure 2. TPD vs V_{CC} at 25°C

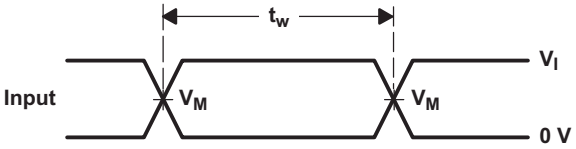
8 Parameter Measurement Information



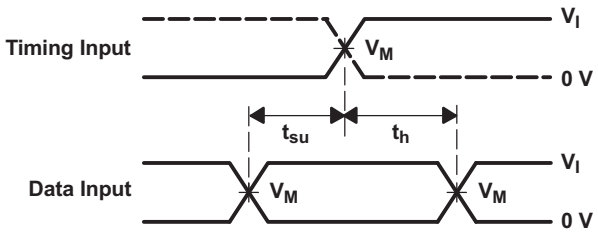
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

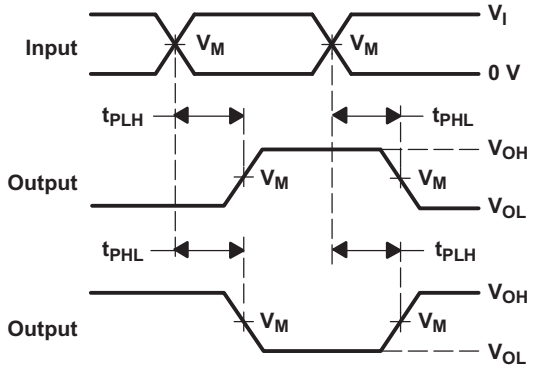
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



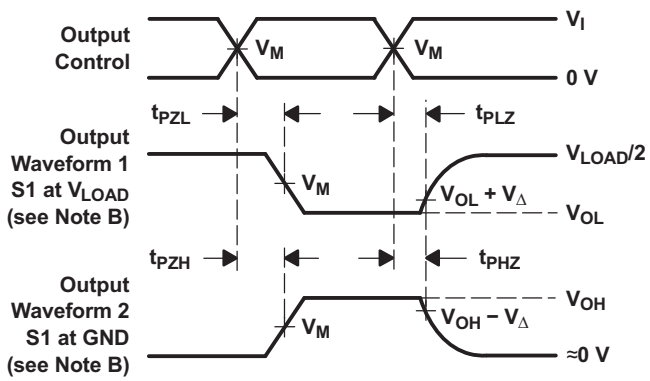
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

This dual negative-edge-triggered J-K flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and K inputs meeting the setup-time requirements is transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and K inputs can be changed without affecting the levels at the outputs. The SN74LVC112A can perform as a toggle flip-flop by tying J and K high.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

9.2 Functional Block Diagram

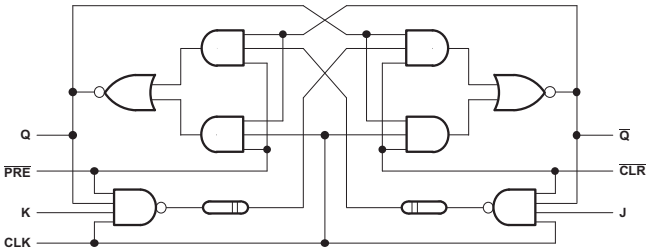


Figure 4. Logic Diagram, Each Flip-Flop (Positive Logic)

9.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65 V to 3.6 V
- Allows down voltage translation
  - Inputs accept voltages to 5.5 V
- I_{off} feature
  - Allows voltages on the inputs and outputs when V_{CC} is 0 V

9.4 Device Functional Modes

Table 1. Function Table

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H(1)	H(1)
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

(1) The output levels in this configuration may not meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it does not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

10 Application and Implementation

10.1 Application Information

SN74LVC112A is a high-drive CMOS device that can be used for a multitude of bus interface type applications where the data needs to be retained or latched. It can produce 24 mA of drive current at 3.3 V, making it Ideal for driving multiple outputs and good for high-speed applications up to 150 MHz. The inputs are 5.5-V tolerant allowing it to translate down to V_{CC}.

10.2 Typical Application

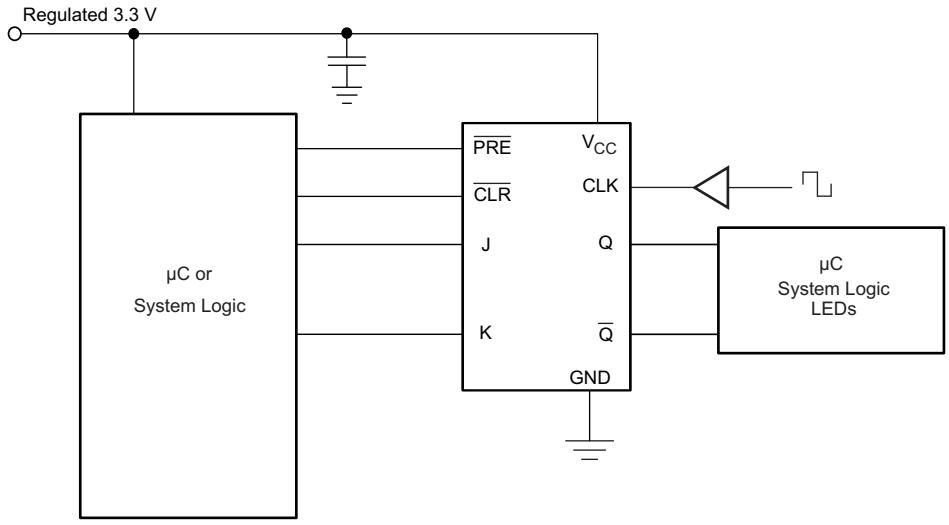


Figure 5. Typical Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in the *Recommended Operating Conditions* table.
   - For specified High and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend Output Conditions
   - Load currents should not exceed 50 mA per output and 100 mA total for the part.
   - Outputs should not be pulled above V_{CC}.

Typical Application (continued)

10.2.3 Application Curves

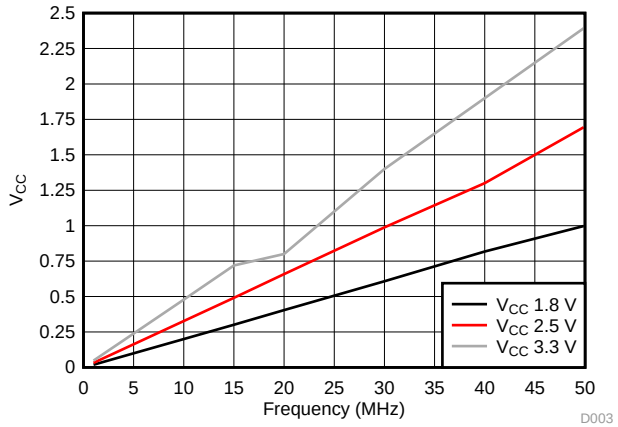


Figure 6. I_{CC} vs Frequency

11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 7 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver..

12.2 Layout Example

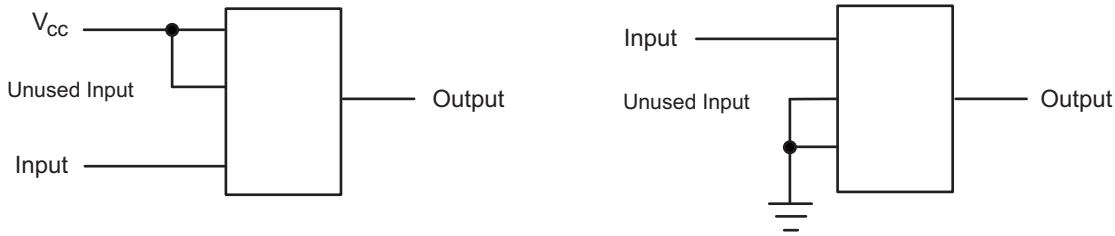


Figure 7. Layout Diagram

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC112AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC112A	Samples
SN74LVC112ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC112A	Samples
SN74LVC112ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC112A	Samples
SN74LVC112ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC112A	Samples
SN74LVC112ADGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC112A	Samples
SN74LVC112ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC112A	Samples
SN74LVC112ADT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC112A	Samples
SN74LVC112ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC112A	Samples
SN74LVC112APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC112A	Samples
SN74LVC112APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC112A	Samples
SN74LVC112APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC112A	Samples
SN74LVC112APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC112A	Samples
SN74LVC112APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC112A	Samples
SN74LVC112APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC112A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

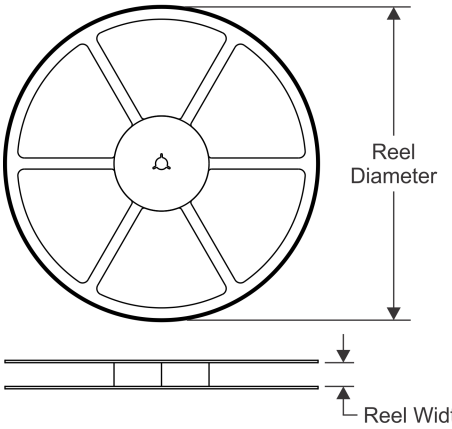
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

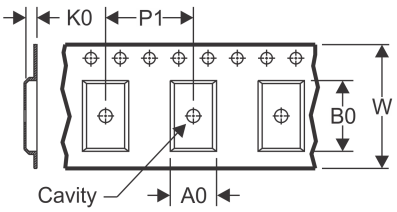
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

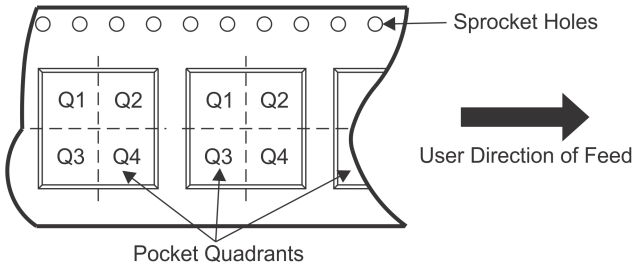


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

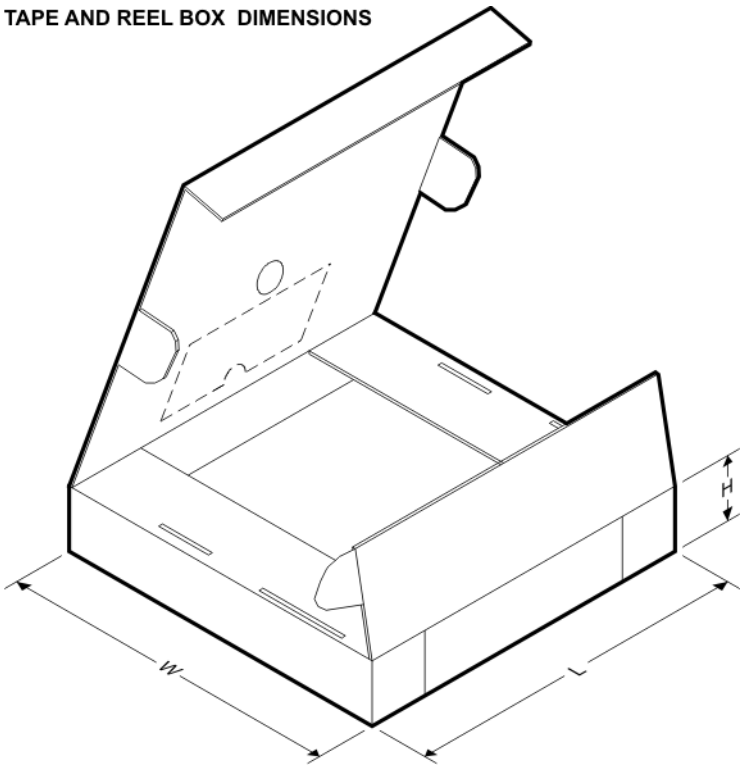
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC112ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LVC112ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVC112ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC112ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC112APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC112APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

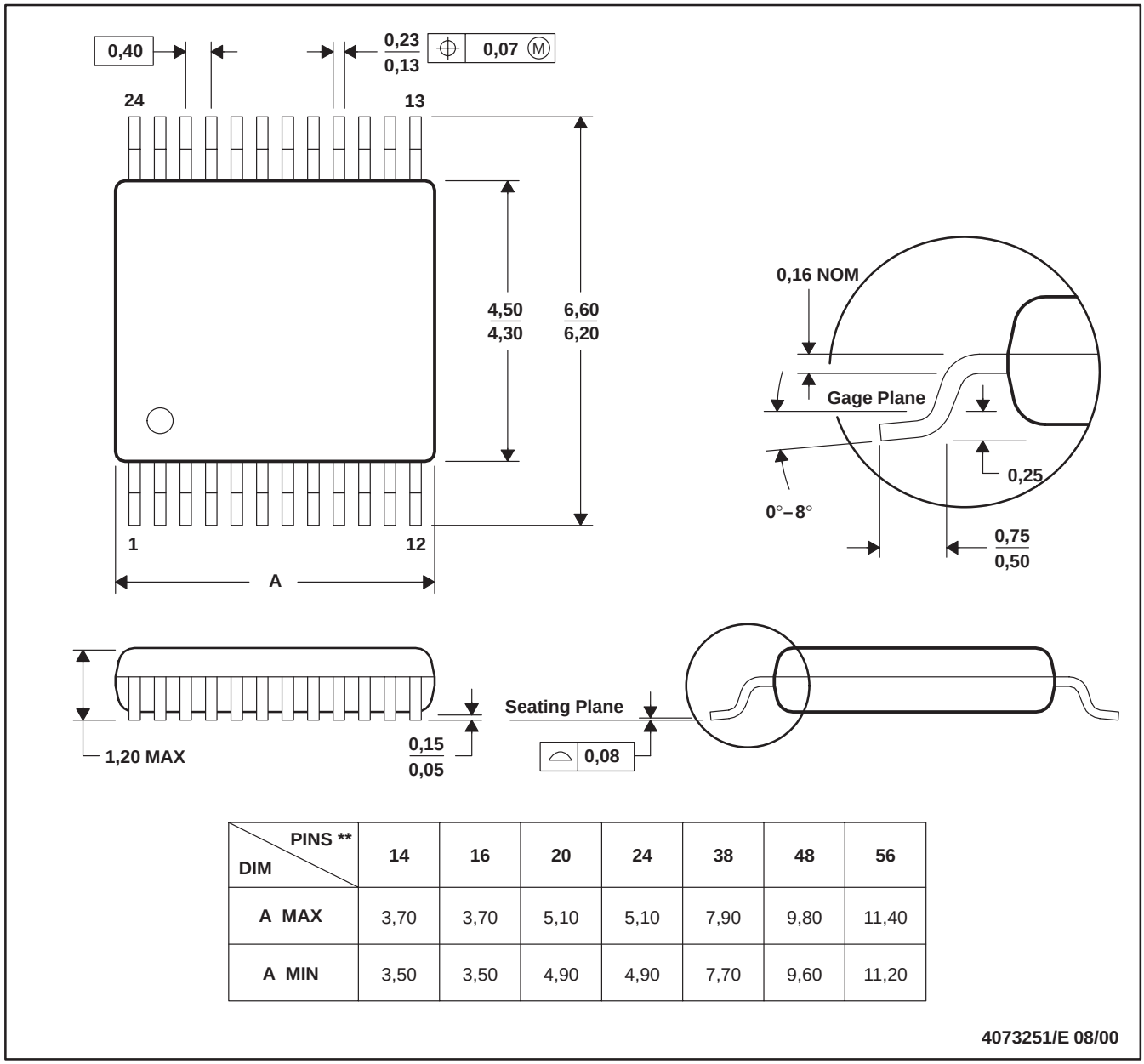


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC112ADBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN74LVC112ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74LVC112ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LVC112ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LVC112APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LVC112APWT	TSSOP	PW	16	250	367.0	367.0	35.0

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

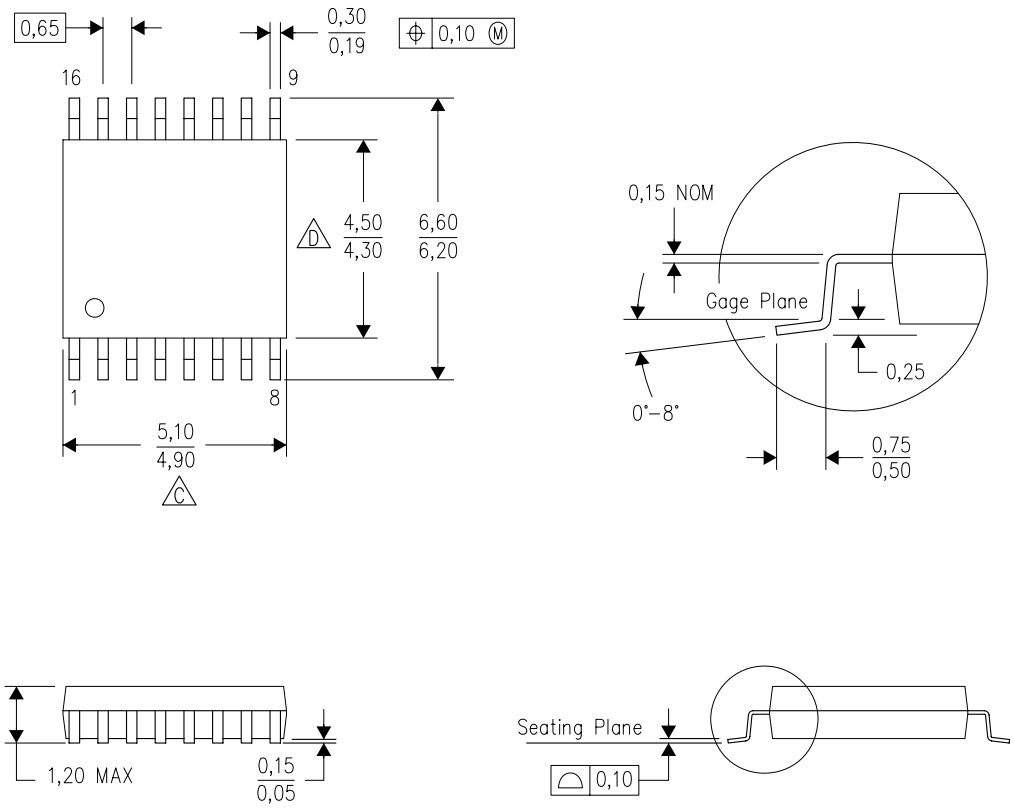


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

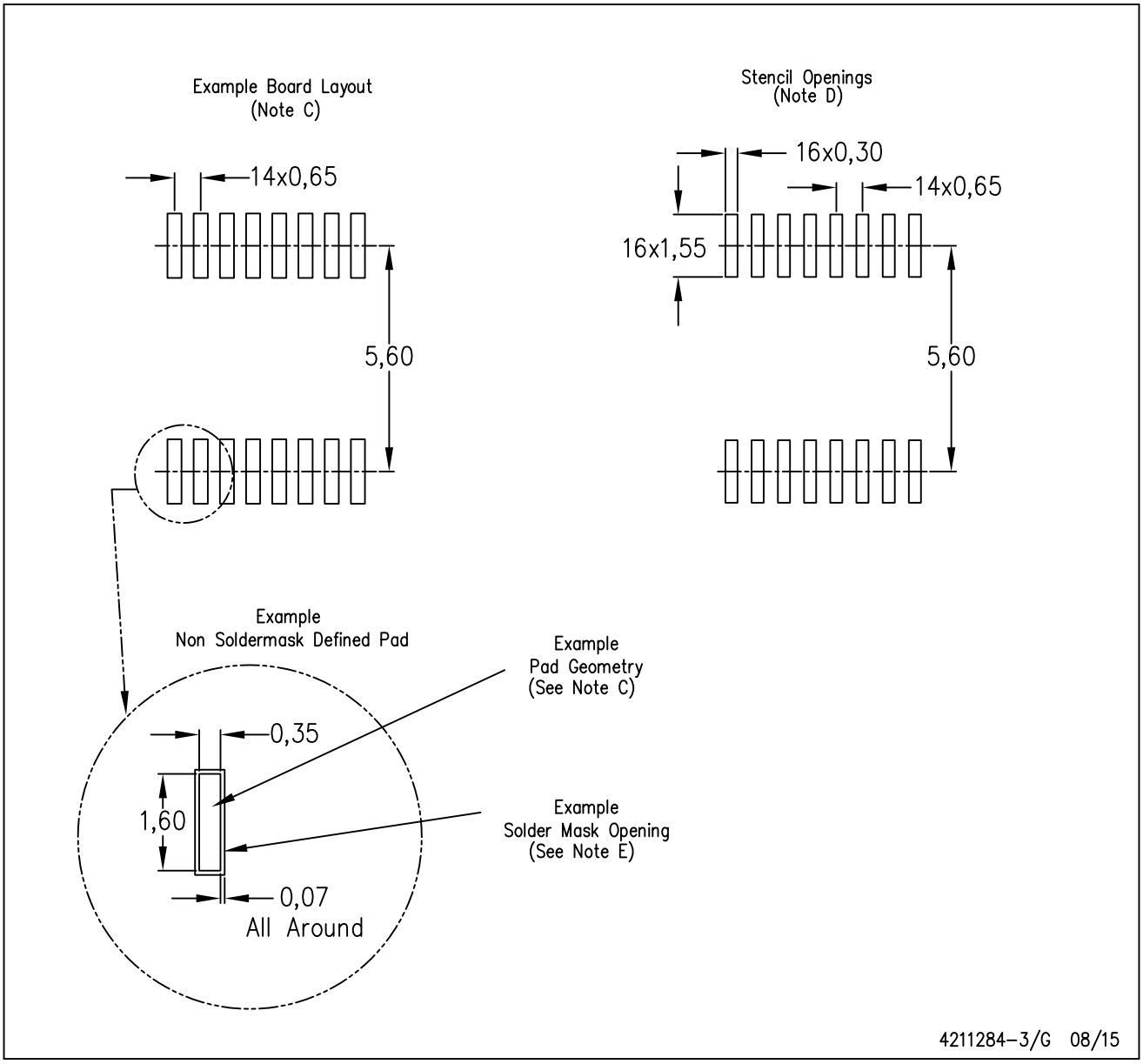
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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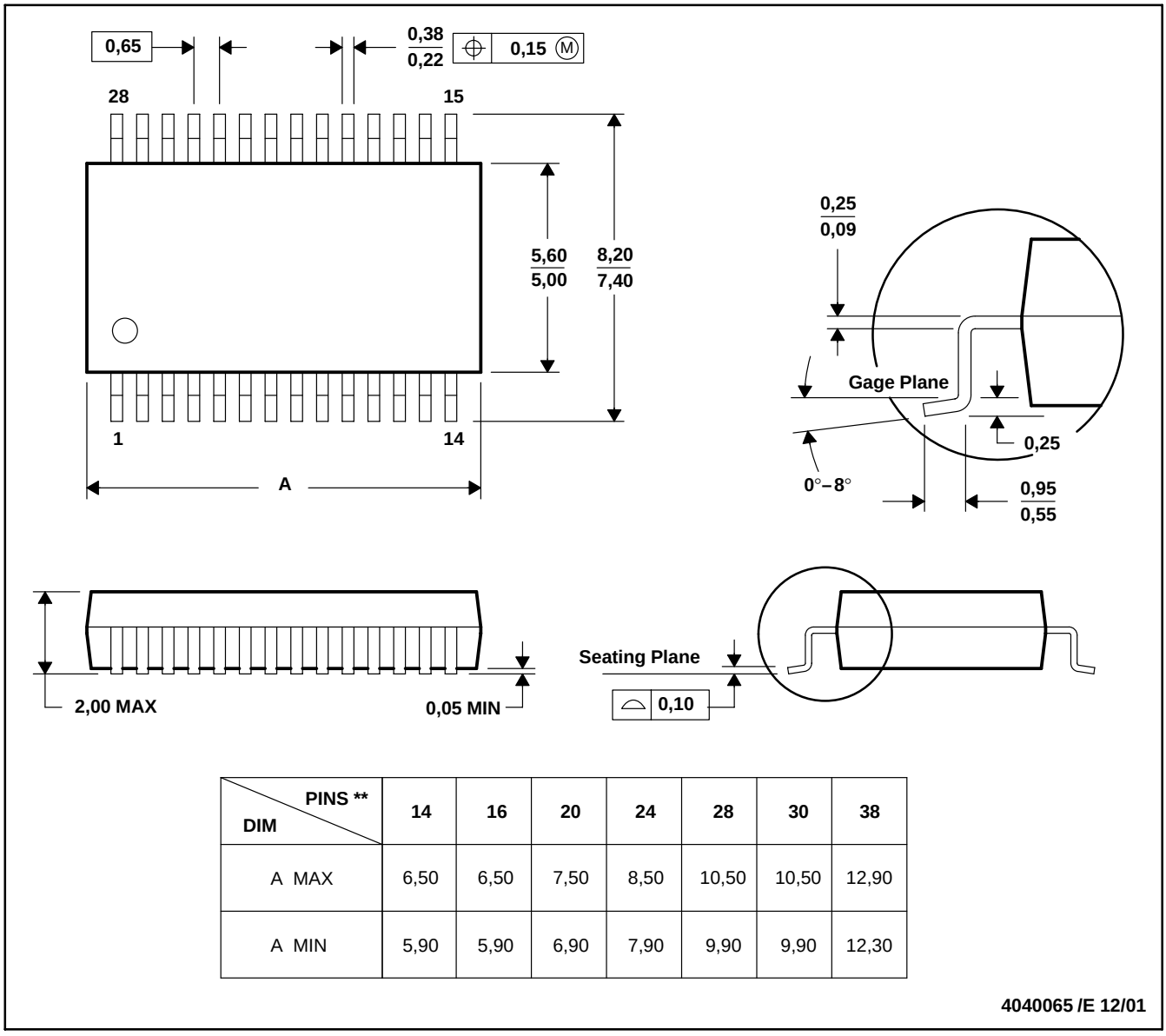
DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

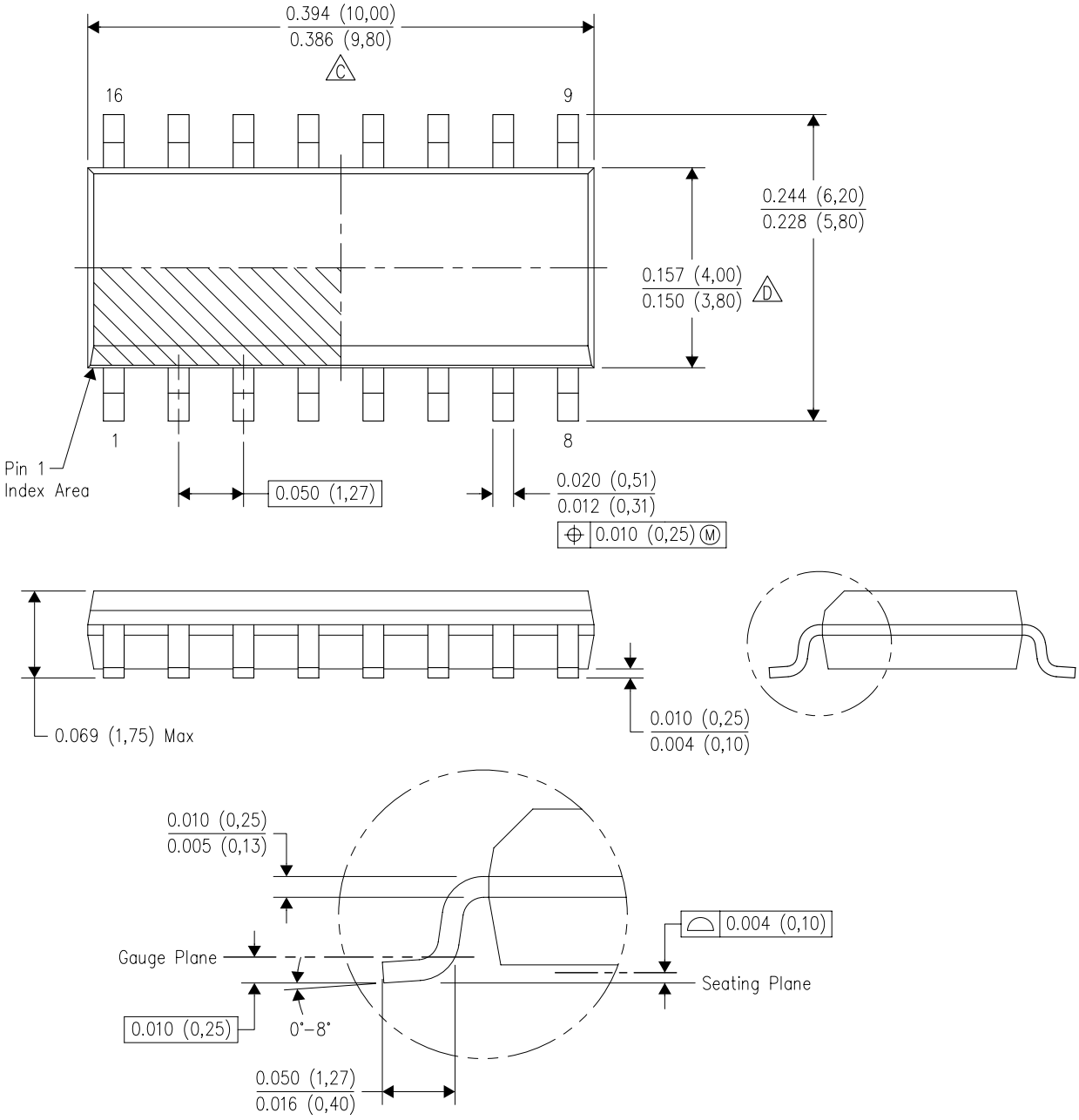


DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

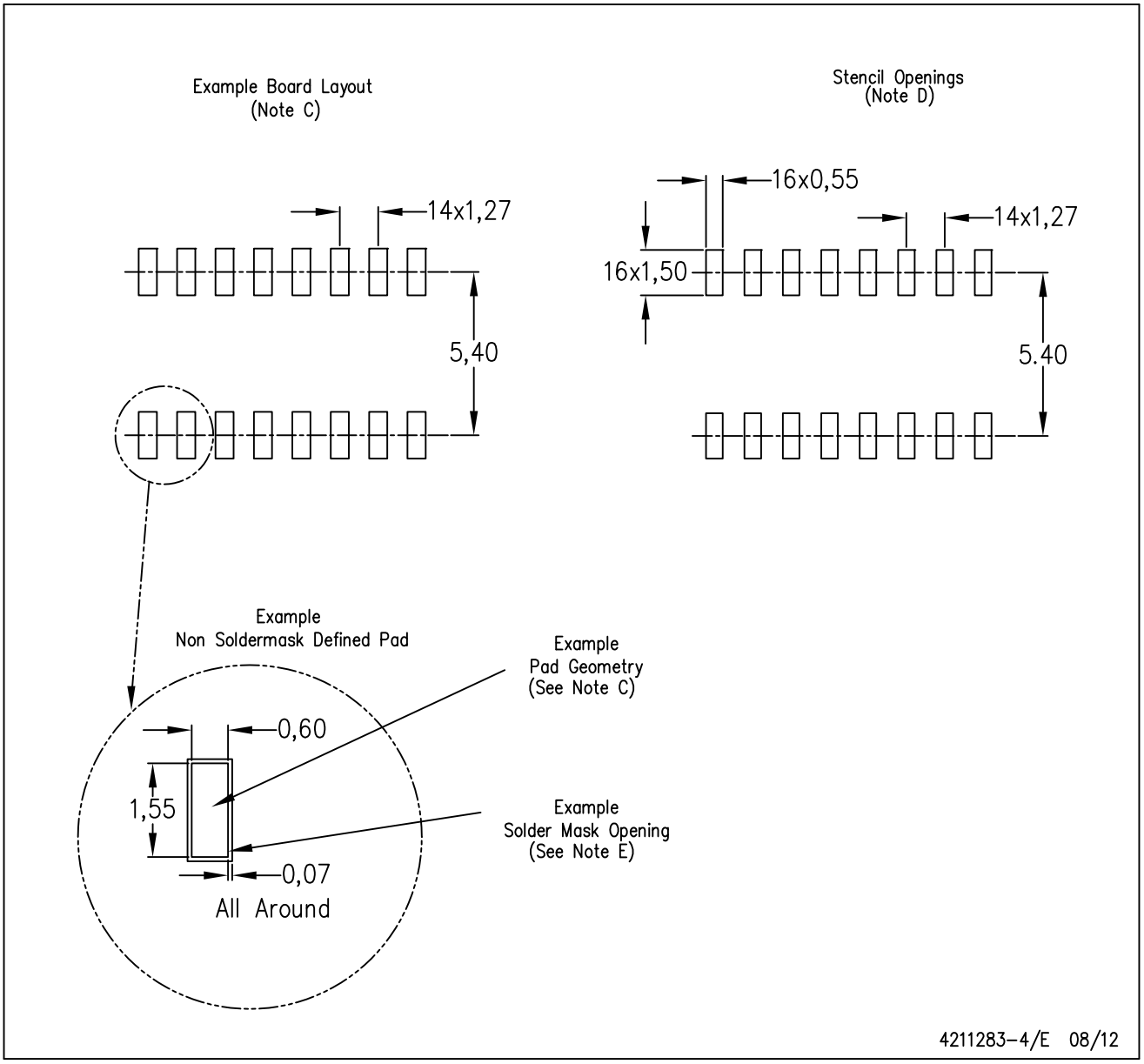
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

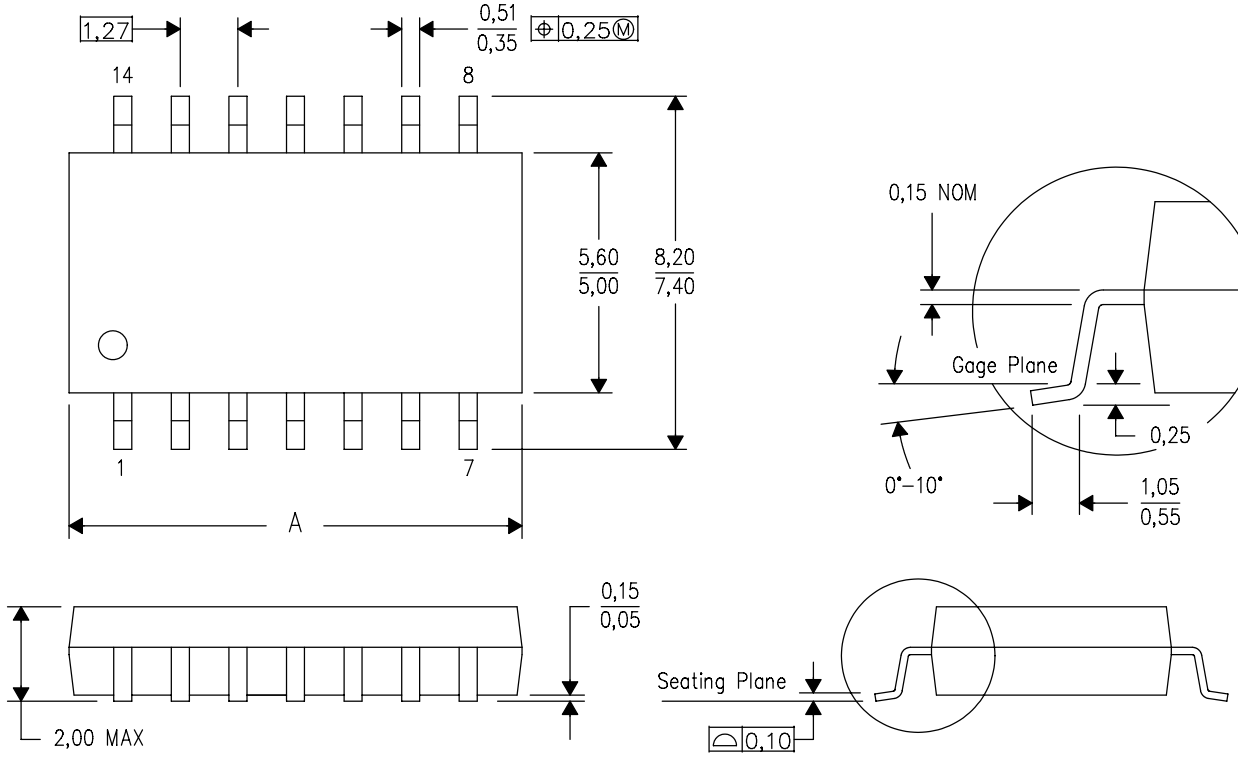


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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