TEXAS INSTRUMENTS

SN74LVC2G53

SCES324P – JULY 2001 – REVISED OCTOBER 2016

SN74LVC2G53 Single-Pole Double-Throw (SPDT) Analog Switch 2:1 Analog Multiplexer/Demultiplexer

1 Features

- Available in the Texas Instruments NanoFree™ Package
- 1.65-V to 5.5-V V_{CC} Operation
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- High Speed, Typically 0.5 ns (V_{CC} = 3 V, C_L = 50 pF)
- Low ON-State Resistance, Typically 6.5 Ω (V_{CC} = 4.5 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

2 Applications

- Wireless Devices
- Audio and Video Signal Routing
- Portable Computing
- Wearable Devices
- Signal Gating, Chopping, Modulation or Demodulation (Modem)
- Signal Multiplexing for Analog-to-Digital and Digital-to-Analog Conversion Systems

3 Description

This single 2:1 analog multiplexer/demultiplexer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G53 device can handle both analog and digital signals. This device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Device Information[(1)]

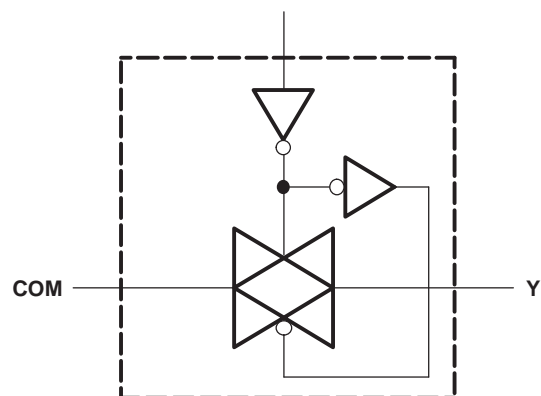| PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC2G53DCT	SM8 (8)	2.95 mm × 2.80 mm
SN74LVC2G53DCU	VSSOP (8)	2.30 mm × 2.00 mm
SN74LVC2G53YZP	DSBGA (8)	1.91 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram
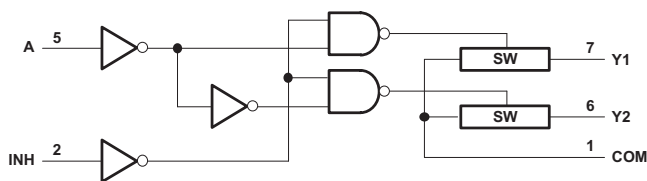
NOTE: For simplicity, the test conditions shown in Figure 1 through Figure 4 and Figure 6 through Figure 10 are for the demultiplexer configuration. Signals can be passed from COM to Y1 (Y2) or from Y1 (Y2) to COM.

Logic Diagram, Each Switch (SW)

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4 Revision History

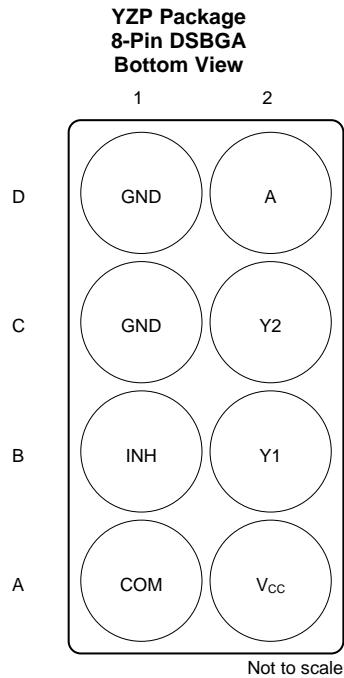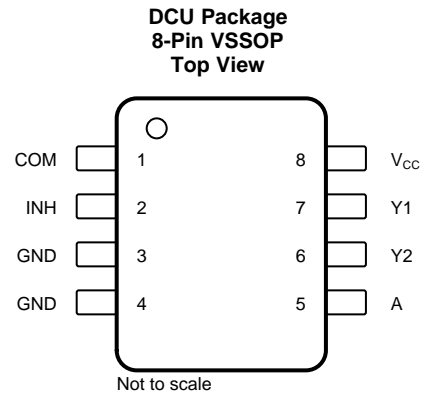NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (December 2015) to Revision P   **Page**

Changes from Revision N (January 2014) to Revision O   **Page**

5 Pin Configuration and Functions

DCT Package
8-Pin SM8
Top View

COM	1	8	V_{CC}

Not to scale

DCU Package
8-Pin VSSOP
Top View

Not to scale

YZP Package
8-Pin DSBGA
Bottom View

Not to scale
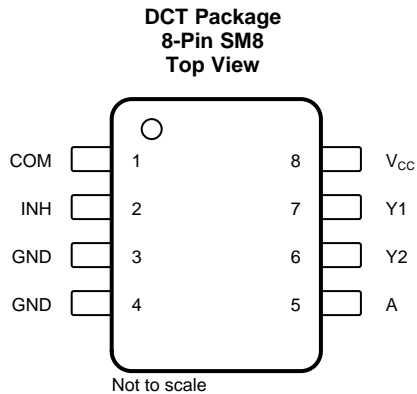
See *Mechanical, Packaging, and Orderable Information* for dimensions.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SM8, VSSOP	DSBGA		
A	5	D2	I	Controls the switch
COM	1	A1	I/O	Bidirectional signal to be switched
GND	3	C1	—	Ground pin
GND	4	D1	—	Ground pin
INH	2	B1	I	Enables or disables the switch
V$_{CC}$	8	A2	—	Power pin
Y2	6	C2	I/O	Bidirectional signal to be switched
Y1	7	B2	I/O	Bidirectional signal to be switched

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage[2]		−0.5	6.5	V
V_I	Input voltage[2][3]		−0.5	6.5	V
$V_{I/O}$	Switch I/O voltage[2][3][4]		−0.5	V_{CC} + 0.5	V
I_{IK}	Control input clamp current	$V_I < 0$		−50	mA
$I_{I/OK}$	I/O port diode current	$V_{I/O} < 0$ or $V_{I/O} > V_{CC}$		±50	mA
I_T	ON-state switch current	$V_{I/O} = 0$ to V_{CC}		±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See note[1].

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_{IH}	High-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V	$V_{CC} × 0.65$		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} × 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} × 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} × 0.7$		
V_{IL}	Low-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V		$V_{CC} × 0.35$	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} × 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} × 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} × 0.3$	
V_I	Control input voltage		0	5.5	V
$\Delta t/\Delta v$	Input transition rise and fall time	V_{CC} = 1.65 V to 1.95 V		20	ns/V
		V_{CC} = 2.3 V to 2.7 V		20	
		V_{CC} = 3 V to 3.6 V		10	
		V_{CC} = 4.5 V to 5.5 V		10	
T_A	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]		SN74LVC2G53			UNIT
		DCT (SM8)	DCU (VSSOP)	YZP (DSBGA)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	220	227	102	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP[1]	MAX	UNIT
r_{on}	ON-state switch resistance	$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$ (see Figure 2 and Figure 1)	$I_S = 4$ mA	1.65 V		13	30	Ω
			$I_S = 8$ mA	2.3 V		10	20	
			$I_S = 24$ mA	3 V		8.5	17	
			$I_S = 32$ mA	4.5 V		6.5	13	
$r_{on(p)}$	Peak ON-state resistance	$V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$ (see Figure 2 and Figure 1)	$I_S = 4$ mA	1.65 V		86.5	120	Ω
			$I_S = 8$ mA	2.3 V		23	30	
			$I_S = 24$ mA	3 V		13	20	
			$I_S = 32$ mA	4.5 V		8	15	
Δr_{on}	Difference of ON-state resistance between switches	$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see Figure 2 and Figure 1)	$I_S = 4$ mA	1.65 V			7	Ω
			$I_S = 8$ mA	2.3 V			5	
			$I_S = 24$ mA	3 V			3	
			$I_S = 32$ mA	4.5 V			2	
$I_{S(off)}$	OFF-state switch leakage current	$V_I = V_{CC}$ and $V_O = $ GND or $V_I = $ GND and $V_O = V_{CC}$, $V_{INH} = V_{IH}$ (see Figure 3)		5.5 V			±1	μA
							±0.1 [1]	
$I_{S(on)}$	ON-state switch leakage current	$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$, $V_O = $ Open (see Figure 4)		5.5 V			±1	μA
							±0.1 [1]	
I_I	Control input current	$V_C = V_{CC}$ or GND		5.5 V			±1	μA
							±0.1 [1]	
I_{CC}	Supply current	$V_C = V_{CC}$ or GND		5.5 V			1	μA
ΔI_{CC}	Supply-current change	$V_C = V_{CC} - 0.6$ V		5.5 V			500	μA
C_{ic}	Control input capacitance			5 V		3.5		pF
$C_{io(off)}$	Switch input/output capacitance	Y		5 V		6.5		pF
		COM				10		
$C_{io(on)}$	Switch input/output capacitance			5 V		19.5		pF

(1) $T_A = 25°C$

Product Folder Links: *SN74LVC2G53*

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V$_{CC}$	MIN	MAX	UNIT
t$_{pd}$[1]	COM or Y	Y or COM	V$_{CC}$ = 1.8 V ± 0.15 V		2	ns
			V$_{CC}$ = 2.5 V ± 0.2 V		1.2	
			V$_{CC}$ = 3.3 V ± 0.3 V		0.8	
			V$_{CC}$ = 5 V ± 0.5 V		0.6	
t$_{en}$[2]	INH	COM or Y	V$_{CC}$ = 1.8 V ± 0.15 V	3.3	9	ns
			V$_{CC}$ = 2.5 V ± 0.2 V	2.5	6.1	
			V$_{CC}$ = 3.3 V ± 0.3 V	2.2	5.4	
			V$_{CC}$ = 5 V ± 0.5 V	1.8	4.5	
t$_{dis}$[3]	INH	COM or Y	V$_{CC}$ = 1.8 V ± 0.15 V	3.2	10.9	ns
			V$_{CC}$ = 2.5 V ± 0.2 V	2.3	8.3	
			V$_{CC}$ = 3.3 V ± 0.3 V	2.3	8.1	
			V$_{CC}$ = 5 V ± 0.5 V	1.6	8	
t$_{en}$[2]	A	COM or Y	V$_{CC}$ = 1.8 V ± 0.15 V	2.9	10.3	ns
			V$_{CC}$ = 2.5 V ± 0.2 V	2.1	7.2	
			V$_{CC}$ = 3.3 V ± 0.3 V	1.9	5.8	
			V$_{CC}$ = 5 V ± 0.5 V	1.3	5.4	
t$_{dis}$[3]	A	COM or Y	V$_{CC}$ = 1.8 V ± 0.15 V	2.1	2.1	ns
			V$_{CC}$ = 2.5 V ± 0.2 V	1.4	7.9	
			V$_{CC}$ = 3.3 V ± 0.3 V	1.1	7.2	
			V$_{CC}$ = 5 V ± 0.5 V	1	5	

(1) t$_{PLH}$ and t$_{PHL}$ are the same as t$_{pd}$. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
(2) t$_{PZL}$ and t$_{PZH}$ are the same as t$_{en}$.
(3) t$_{PLZ}$ and t$_{PHZ}$ are the same as t$_{dis}$.

6.7 Analog Switch Characteristics

T$_A$ = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V$_{CC}$	TYP	UNIT
Frequency response (switch on)	COM or Y	Y or COM	C$_L$ = 50 pF, R$_L$ = 600 Ω, f$_{in}$ = sine wave (see Figure 6)	1.65 V	35	MHz
				2.3 V	120	
				3 V	190	
				4.5 V	215	
			C$_L$ = 5 pF, R$_L$ = 50 Ω, f$_{in}$ = sine wave (see Figure 6)	1.65 V	>300	
				2.3 V	>300	
				3 V	>300	
				4.5 V	>300	
Crosstalk[1] (between switches)	COM or Y	Y or COM	C$_L$ = 50 pF, R$_L$ = 600 Ω, f$_{in}$ = 1 MHz (sine wave) (see Figure 7)	1.65 V	−58	dB
				2.3 V	−58	
				3 V	−58	
				4.5 V	−58	
			C$_L$ = 5 pF, R$_L$ = 50 Ω, f$_{in}$ = 1 MHz (sine wave) (see Figure 7)	1.65 V	−42	
				2.3 V	−42	
				3 V	−42	
				4.5 V	−42	

(1) Adjust f$_{in}$ voltage to obtain 0 dBm at input.

Product Folder Links: *SN74LVC2G53*

Analog Switch Characteristics (continued)

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Crosstalk (control input to signal output)	INH	COM or Y	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)	1.65 V	35	mV
				2.3 V	50	
				3 V	70	
				4.5 V	100	
Feedthrough attenuation (switch off)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	1.65 V	−60	dB
				2.3 V	−60	
				3 V	−60	
				4.5 V	−60	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	1.65 V	−50	
				2.3 V	−50	
				3 V	−50	
				4.5 V	−50	
Sine-wave distortion	COM or Y	Y or COM	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	1.65 V	0.1%	
				2.3 V	0.025%	
				3 V	0.015%	
				4.5 V	0.01%	
			C_L = 50 pF, R_L = 10 kΩ, f_{in} = 10 kHz (sine wave) (see Figure 10)	1.65 V	0.15%	
				2.3 V	0.025%	
				3 V	0.015%	
				4.5 V	0.01%	

6.8 Operating Characteristics

T_A = 25°C

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	V_{CC} = 1.8 V	9	pF
		V_{CC} = 2.5 V	10	
		V_{CC} = 3.3 V	10	
		V_{CC} = 5 V	12	

6.9 Typical Characteristics
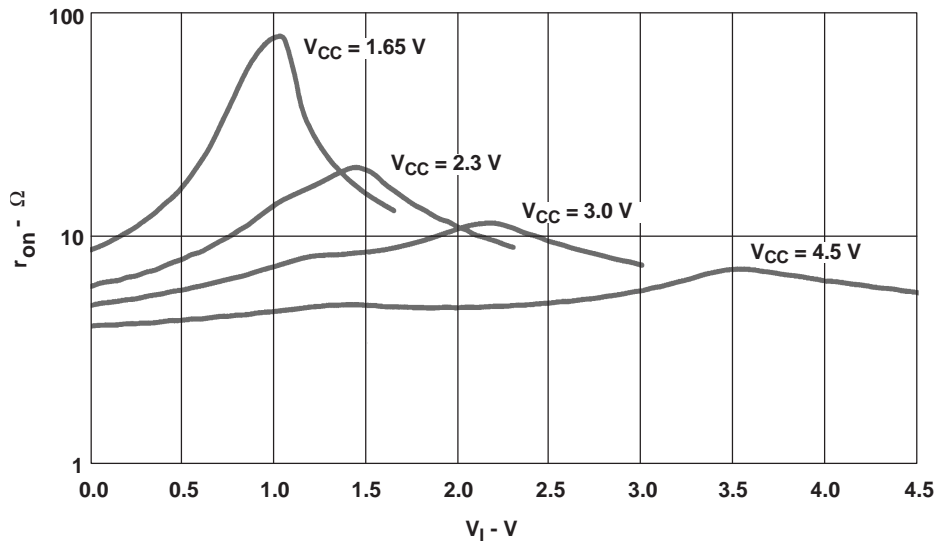
Figure 1. Typical r_{on} as a Function of Input Voltage (V_I) for V_I = 0 to V_{CC}

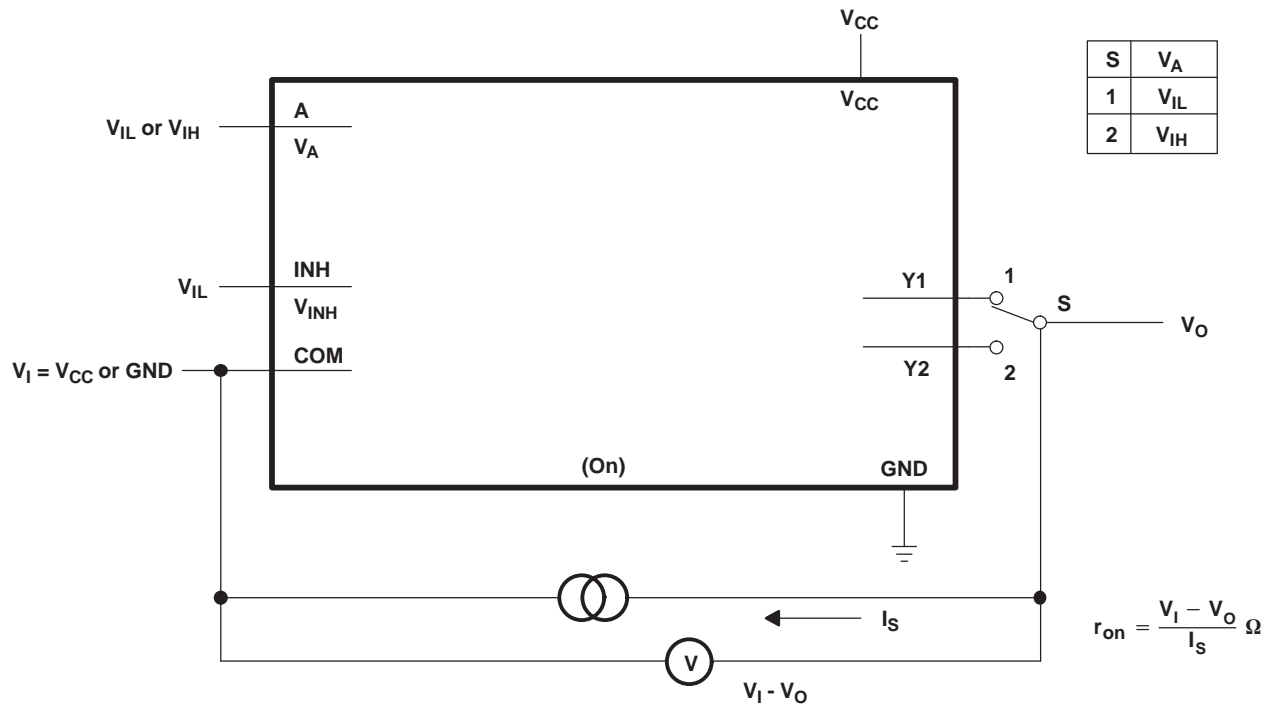Product Folder Links: *SN74LVC2G53*

# 7 Parameter Measurement Information

Figure 2. ON-State Resistance Test Circuit
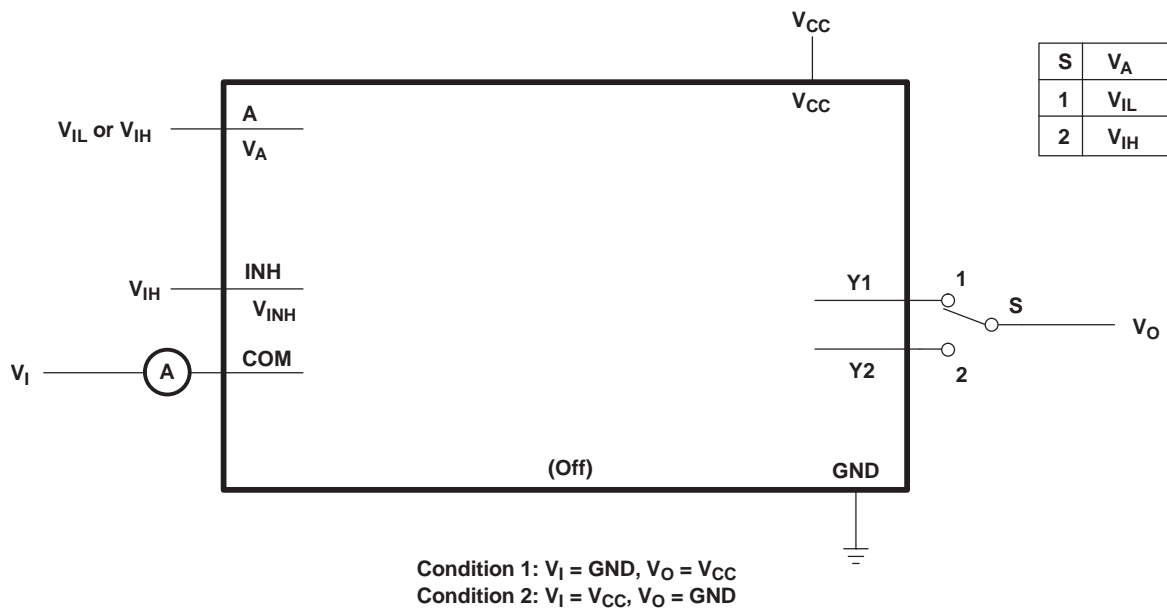
Figure 3. OFF-State Switch Leakage-Current Test Circuit

Product Folder Links: *SN74LVC2G53*

Parameter Measurement Information (continued)

S	V_A
1	V_{IL}
2	V_{IH}
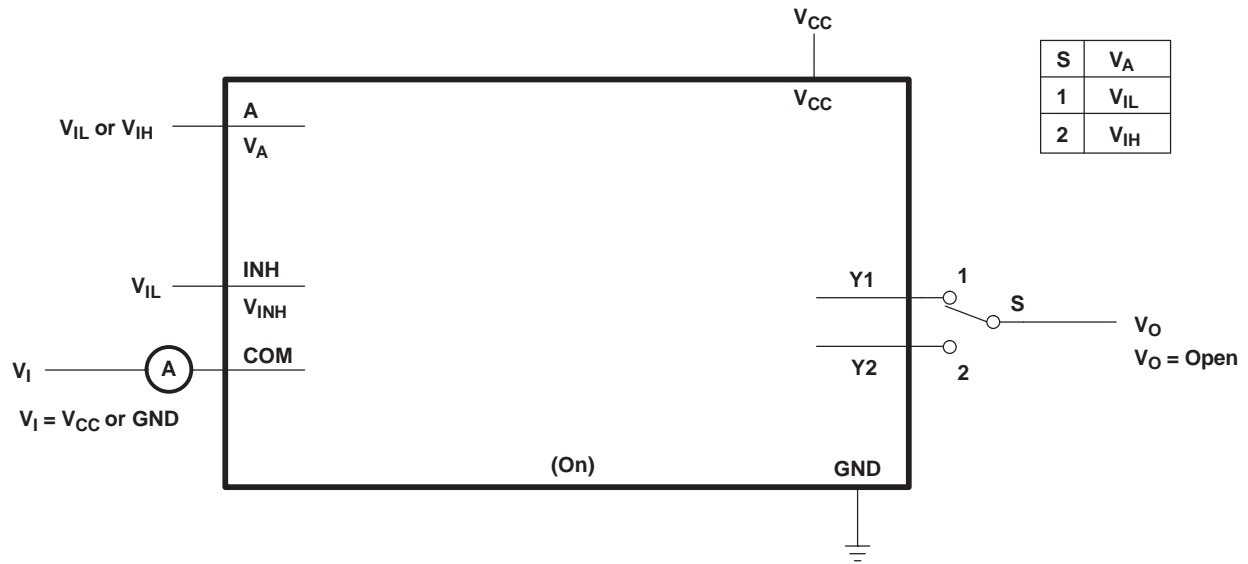
Figure 4. ON-State Switch Leakage-Current Test Circuit

Product Folder Links: *SN74LVC2G53*

Parameter Measurement Information (continued)
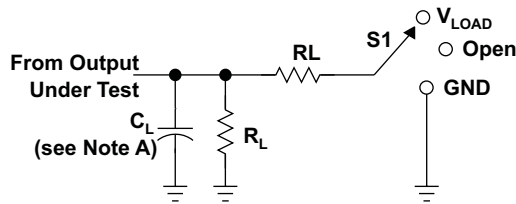
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

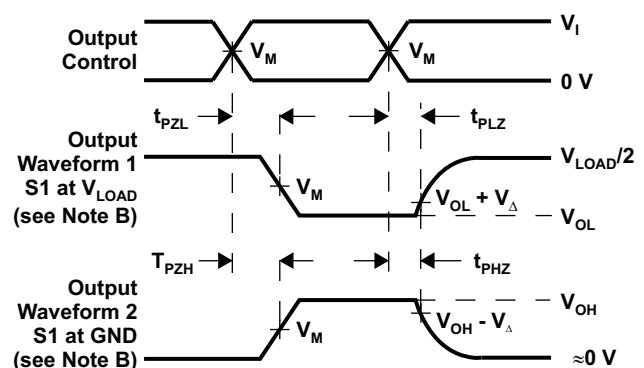| V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
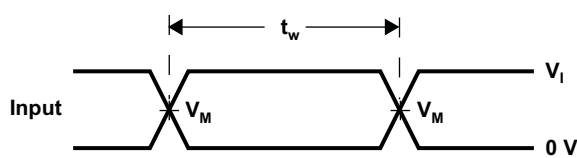
VOLTAGE WAVEFORMS
PULSE DURATION
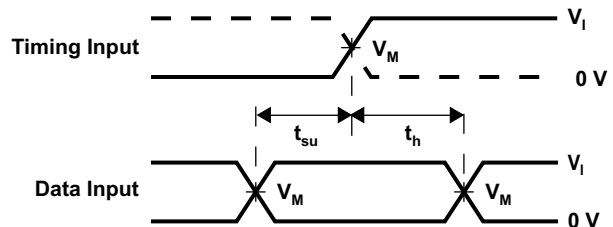
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
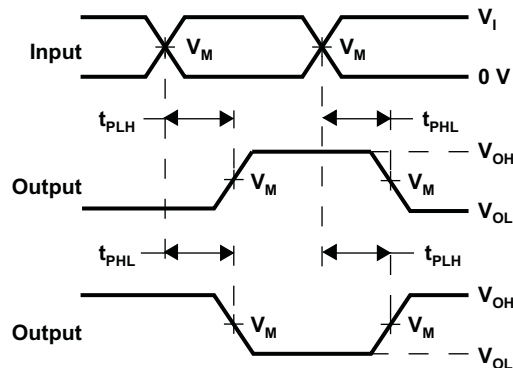
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 Mhz, Z_O = 50 Ω
   D. The outputs are measured one at a time, with one transition per measurement.
   E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
   F. t_{PZL} and t_{PZH} are the same as t_{en}.
   G. t_{PLH} and t_{PHL} are the same as t_{pd}.
   H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

Product Folder Links: SN74LVC2G53

Parameter Measurement Information (continued)

S	V_A
1	V_{IL}
2	V_{IH}

R_L/C_L: 600 Ω/50 pF
R_L/C_L: 50 Ω/5 pF
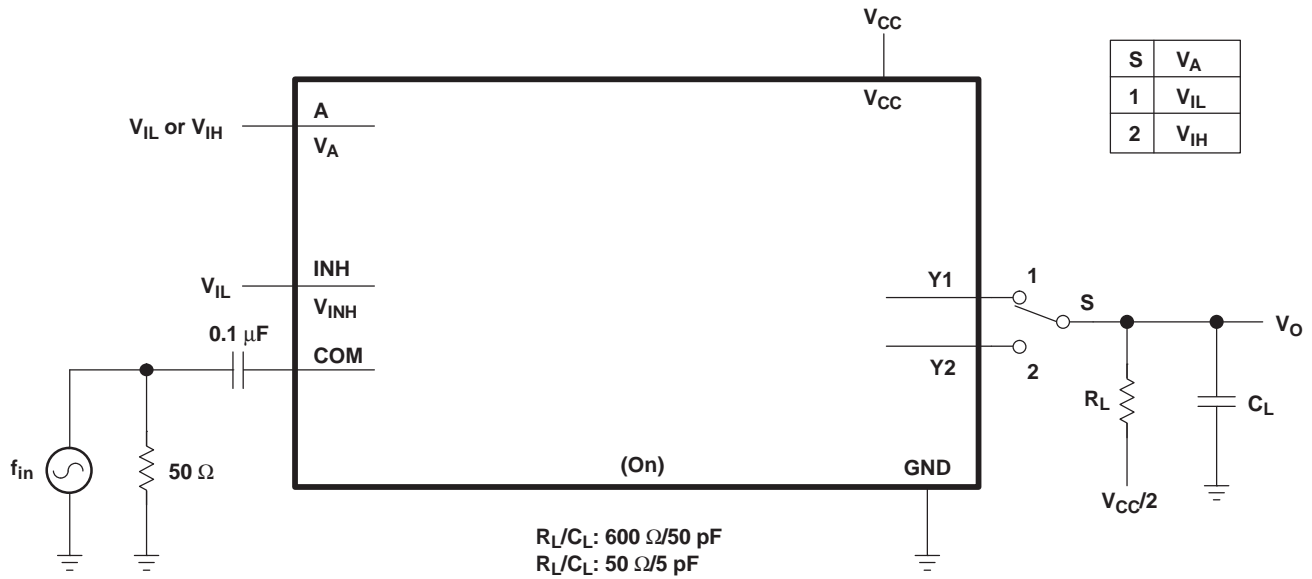
Figure 6. Frequency Response (Switch On)

V_A	TEST CONDITION
V_{IL}	$20\log_{10}(V_{O2}/V_I)$
V_{IH}	$20\log_{10}(V_{O1}/V_I)$
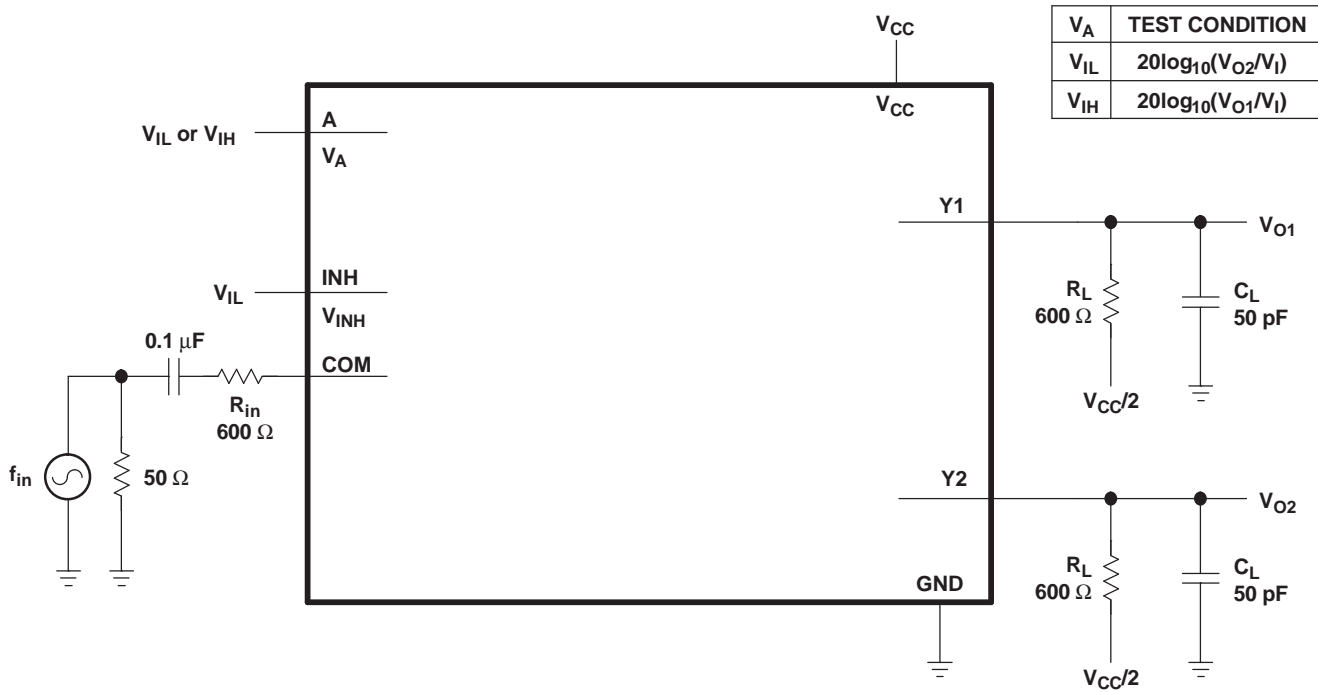
Figure 7. Crosstalk (Between Switches)

Parameter Measurement Information (continued)

S	V_A
1	V_{IL}
2	V_{IH}
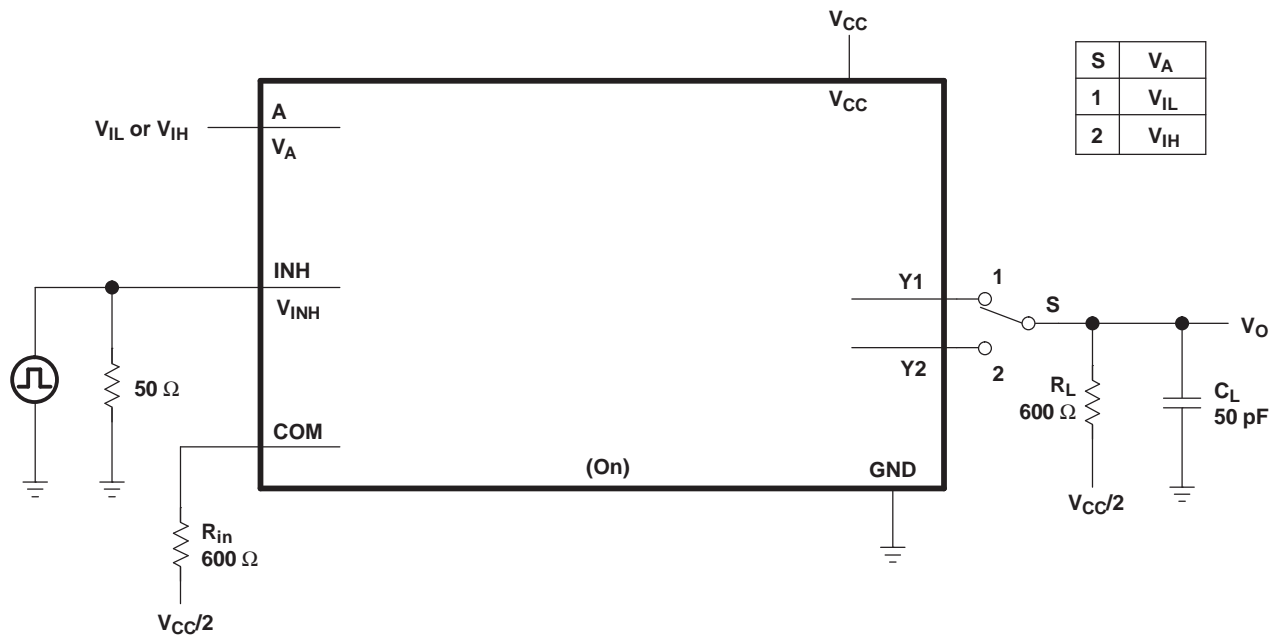
Figure 8. Crosstalk (Control Input, Switch Output)

S	V_A
1	V_{IL}
2	V_{IH}

R_L/C_L: 600 Ω/50 pF
R_L/C_L: 50 Ω/5 pF
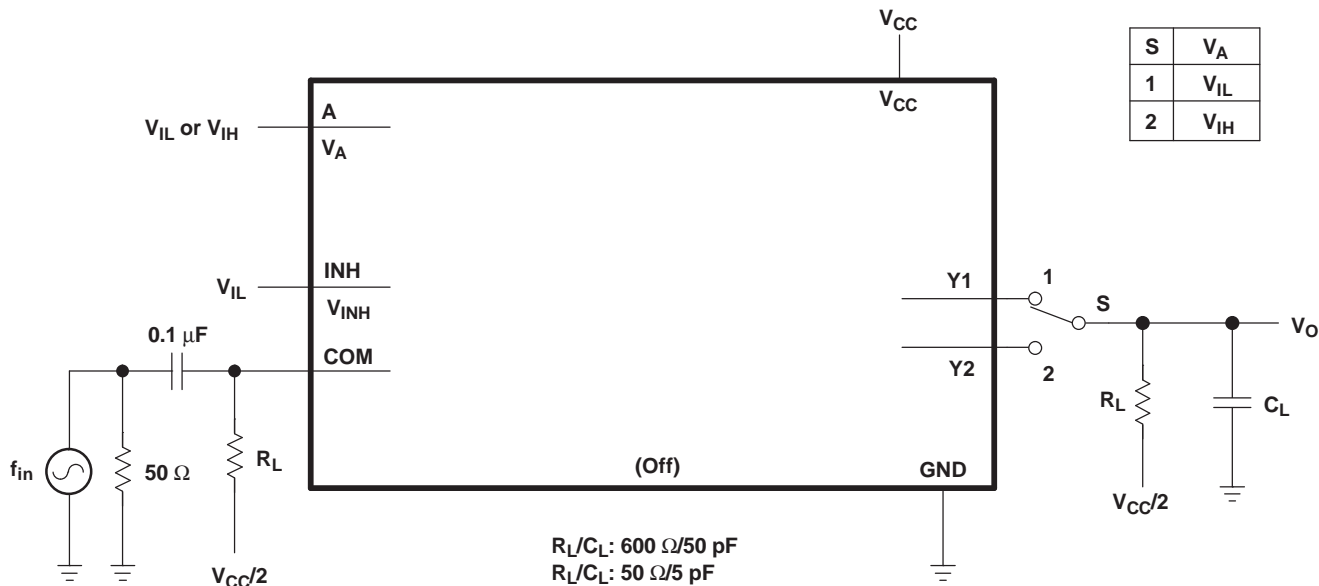
Figure 9. Feedthrough (Switch Off)

Product Folder Links: SN74LVC2G53

Parameter Measurement Information (continued)

S	V_A
1	V_{IL}
2	V_{IH}

V_{CC} = 1.65 V, V_I = 1.4 V_{P-P}
V_{CC} = 2.30 V, V_I = 2.0 V_{P-P}
V_{CC} = 3.00 V, V_I = 2.5 V_{P-P}
V_{CC} = 4.50 V, V_I = 4.0 V_{P-P}
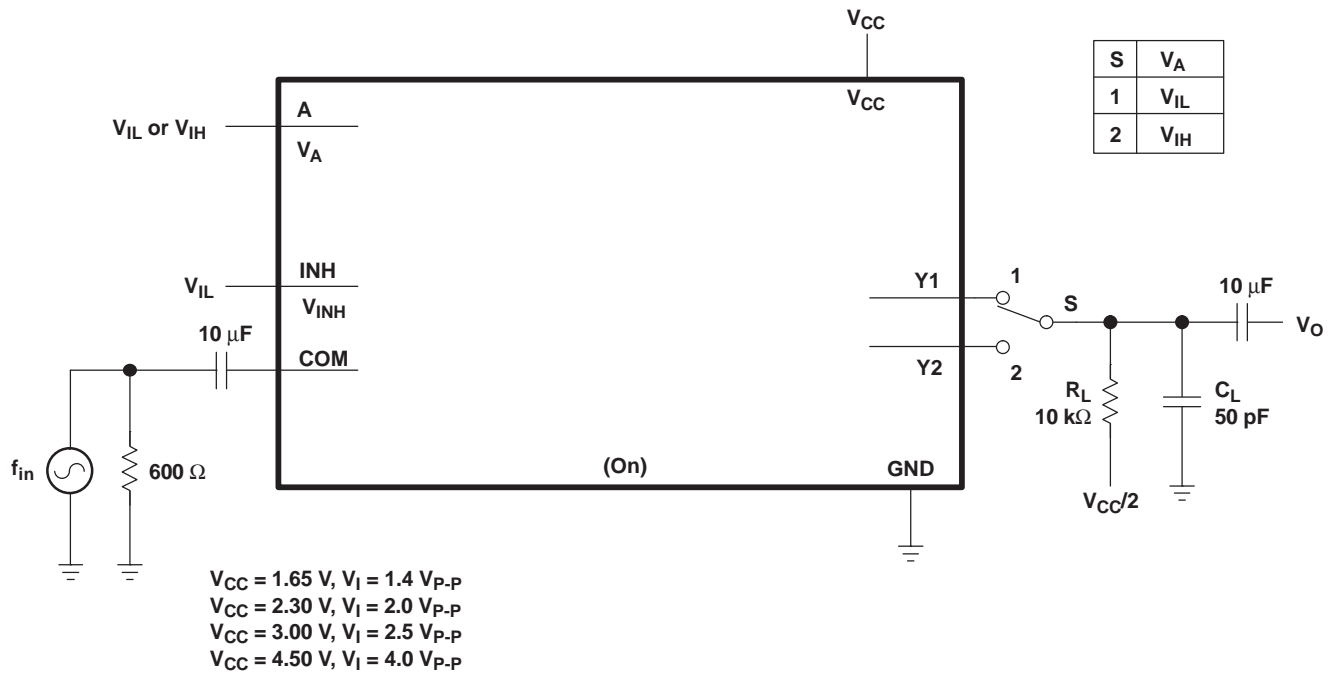
Figure 10. Sine-Wave Distortion

Product Folder Links: *SN74LVC2G53*

8 Detailed Description

8.1 Overview

This dual analog multiplexer/demultiplexer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G53 device can handle both analog and digital signals. This device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

8.2 Functional Block Diagram
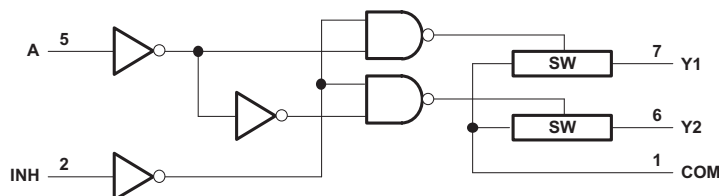
NOTE: For simplicity, the test conditions shown in Figure 1 through Figure 4 and Figure 6 through Figure 10 are for the demultiplexer configuration. Signals can be passed from COM to Y1 (Y2) or from Y1 (Y2) to COM.

Figure 11. Logic Diagram
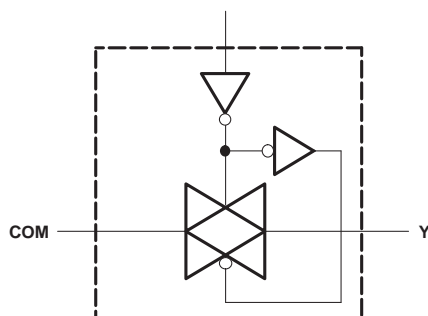
Figure 12. Logic Diagram, Each Switch (SW)

8.3 Feature Description

A high-level voltage applied to INH disables the switches. When INH is low, signals can pass from A to Y or Y to A. Low ON-resistance of 6.5 Ω at 4.5-V V_{CC} is ideal for analog signal conditioning systems. The control signals can accept voltages up to 5.5 V without V_{CC} connected in the system. Combination of lower t_{pd} of 0.8 ns at 3.3 V and low enable and disable time make this part suitable for high-speed signal switching applications.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC2G53.

Table 1. Function Table

CONTROL INPUTS		ON CHANNEL
INH	A	
L	L	Y1
L	H	Y2
H	X	None

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC2G53 can be used in any situation where an SPDT switch is required in an application. This switch helps to select one of two signals of which signals can be either digital or analog.

9.2 Typical Application
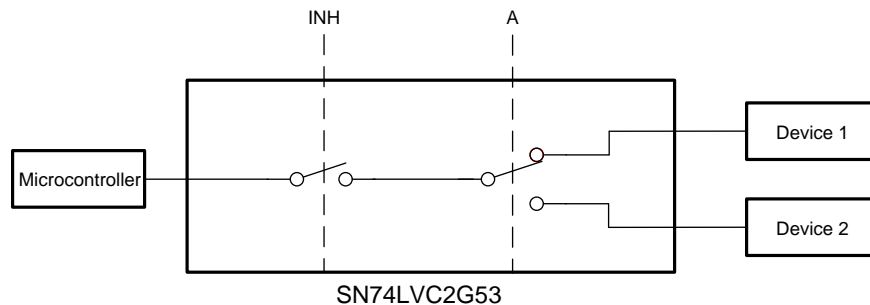
Figure 13. Typical Application Schematic

9.2.1 Design Requirements

The SN74LVC2G53 allows on/off control of analog and digital signals with a digital control signal. All input signals should remain between 0 V and V_{CC} for optimal operation.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   – For rise time and fall time specifications, see Δt/Δv in the *Recommended Operating Conditions* table.
   – For specified high and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
   – Inputs and outputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommended Output Conditions:
   – Load currents should not exceed ±50 mA.
3. Frequency Selection Criterion:
   – Maximum frequency tested is 150 MHz.
   – Added trace resistance or capacitance can reduce maximum frequency capability; use layout practices as directed in *Layout*.

Product Folder Links: *SN74LVC2G53*

Typical Application (continued)

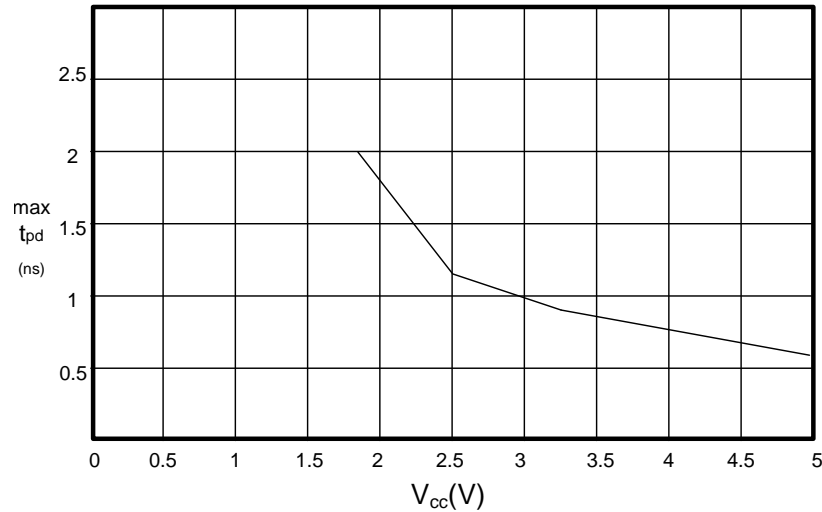### 9.2.3 Application Curve

Figure 14. t_{pd} vs V_{CC}

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* .

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection.

NOTE

Not all PCB traces can be straight, and so they will have to turn corners. Figure 15 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

11.2 Layout Example

WORST   BETTER   BEST

2W

1W min.

W

Figure 15. Trace Example

Product Folder Links: *SN74LVC2G53*
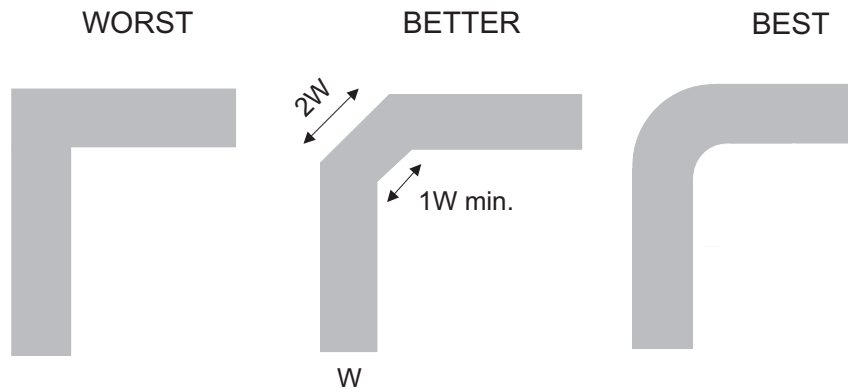
12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC2G53DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C53 Z	Samples
SN74LVC2G53DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C53 Z	Samples
SN74LVC2G53DCTRG4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C53 Z	Samples
SN74LVC2G53DCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	(53 ~ C53Q ~ C53R) CZ	Samples
SN74LVC2G53DCURG4	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C53R	Samples
SN74LVC2G53DCUT	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	(53 ~ C53Q ~ C53R) CZ	Samples
SN74LVC2G53DCUTG4	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C53R	Samples
SN74LVC2G53YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C4N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G53DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G53DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G53DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.05	3.3	1.0	4.0	8.0	Q3
SN74LVC2G53DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G53DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G53YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

TEXAS INSTRUMENTS

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G53DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G53DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G53DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
SN74LVC2G53DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G53DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G53YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

DCU (R−PDSO−G8)   PLASTIC SMALL−OUTLINE PACKAGE (DIE DOWN)

4200503/F 07/05

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO−187 variation CA.

DCU (S−PDSO−G8)   PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)

Example Board Layout
(Note C,E)

6x 0,5

3,1

Example Stencil Design
(Note D)

8x 0,25

6x 0,5

8x 0,75

3,1

0,3

0,8

Example
Solder Mask Opening

Pad Geometry

0,05

All Around

4210064/C 04/12

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS
INSTRUMENTS
www.ti.com

DCT (R-PDSO-G8)   **PLASTIC SMALL-OUTLINE PACKAGE**

4188781/C 09/02

NOTES: A. All linear dimensions are in millimeters.
            B. This drawing is subject to change without notice.
            C. Body dimensions do not include mold flash or protrusion
            D. Falls within JEDEC MO-187 variation DA.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

DCT (R−PDSO−G8)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C,E)

6x0,65

3,40

Example Stencil Design
(Note D)

8x0,25   6x0,65

8x1,55

3,40

Non Solder Mask Defined Pad

0,30

1,60

0,07
All Around

Example
Pad Geometry
(Note C)

Example
Non−solder Mask Opening
(Note E)

4212201/A   10/11

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers
            should contact their board assembly site for stencil design recommendations. Refer to IPC−7525.
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

B ▶| E |◀ A

BALL A1
CORNER

D

0.5 MAX

0.19
0.15

BALL TYP

C

SEATING PLANE

⌒ 0.05 C

0.5 TYP

D

C

SYMM
₵

1.5
TYP

B

0.5
TYP

A

D: Max = 1.918 mm, Min =1.858 mm

E: Max = 0.918 mm, Min =0.858 mm

8X ⌀ 0.25
0.21

1   2

⊕ 0.015Ⓜ C A B

SYMM
₵

4223082/A   07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.

8X ($\emptyset$ 0.23)

(0.5) TYP

(0.5) TYP

1 2

A

B

SYMM
℄

C

D

SYMM
℄

LAND PATTERN EXAMPLE
SCALE:40X

SOLDER MASK
OPENING

0.05 MAX

($\emptyset$ 0.23)
METAL

NON-SOLDER MASK
DEFINED
(PREFERRED)

0.05 MIN

($\emptyset$ 0.23)
SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A   07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE