# SN74LVC827A 10-Bit Buffer/Driver With 3-State Outputs

## 1 Features

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max $t_{pd}$ of 6.7 ns at 3.3 V
- Typical $V_{OLP}$ (Output Ground Bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) > 2 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V $V_{CC}$)
- $I_{off}$ Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 1000-V Charged-Device Model

## 2 Applications

- LED Displays
- Network Switches
- Telecom Infrastructure
- Servers
- Motor Drivers
- I/O Expanders

## 3 Description/Ordering Information

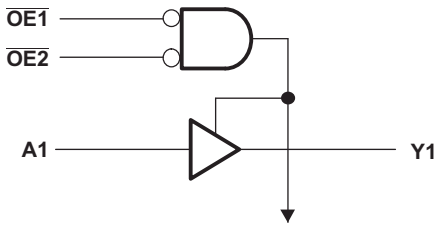
The SN74LVC827A device is a 10-bit buffer/bus driver is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74LVC827A | TVSOP (24) | 5.00 mm × 4.40 mm |
| | SOIC (24) | 15.40 mm × 7.50 mm |
| | SSOP (24) | 8.20 mm × 5.30 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## 4 Simplified Schematic



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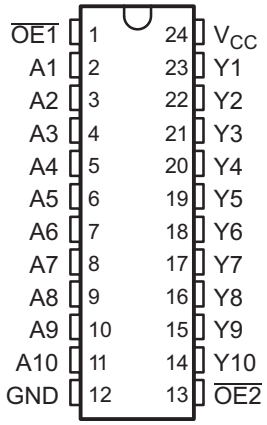
## 5 Revision History

**Changes from Revision J (February 2005) to Revision K** **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table. ... 1
- Changed $I_{off}$ bullet in *Features*. ... 1
- Changed MAX operating temperature to 125°C in the *Recommended Operating Conditions* table. ... 5
- Added –40°C to 125°C temperature range to *Electrical Characteristics* table. ... 6
- Changed $t_{sk(o)}$ in *Switching Characteristics, –40°C to 85°C* table. ... 6
- Added *Switching Characteristics, –40°C to 125°C* table. ... 6

# 6 Pin Configuration and Functions

**DB, DGV, DW, OR PW PACKAGE**
**(TOP VIEW)**




**Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | $\overline{OE1}$ | I | Output Enable 1 |
| 2 | A1 | I | A1 Input |
| 3 | A2 | I | A2 Input |
| 4 | A3 | I | A3 Input |
| 5 | A4 | I | A4 Input |
| 6 | A5 | I | A5 Input |
| 7 | A6 | I | A6 Input |
| 8 | A7 | I | A7 Input |
| 9 | A8 | I | A8 Input |
| 10 | A9 | I | A9 Input |
| 11 | A10 | I | A10 Input |
| 12 | GND | — | Ground Pin |
| 13 | $\overline{OE2}$ | I | Output Enable 2 |
| 14 | Y10 | O | Y10 Output |
| 15 | Y9 | O | Y9 Output |
| 16 | Y8 | O | Y8 Output |
| 17 | Y7 | O | Y7 Output |
| 18 | Y6 | O | Y6 Output |
| 19 | Y5 | O | Y5 Output |
| 20 | Y4 | O | Y4 Output |
| 21 | Y3 | O | Y3 Output |
| 22 | Y2 | O | Y2 Output |
| 23 | Y1 | O | Y1 Output |
| 24 | $V_{CC}$ | — | Power Pin |

# 7 Specifications

## 7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range, applied to any output in the high-impedance or power-off state(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range, applied to any output in the high or low state(2)(3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CC}$ is provided in the *Recommended Operating Conditions* table.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | 1000 | |
| | | Machine Model (MM) | 200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | High or low state | 0 | $V_{CC}$ | V |
| | | 3-state | 0 | 5.5 | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | –8 | |
| | | $V_{CC}$ = 2.7 V | | –12 | |
| | | $V_{CC}$ = 3 V | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 2.7 V | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | |
| Δt/Δv | Input transition rise or fall rate | | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 7.4 Thermal Information

| THERMAL METRIC(1) | | SN74LVC827A | | | | UNIT |
|---|---|---|---|---|---|---|
| | | DB | DGV | DW | PW | |
| | | 24 PINS | | | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 75.5 | 89.4 | 65.1 | 88.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 36.9 | 22.1 | 33.3 | 20.7 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 33.1 | 42.8 | 34.7 | 43.4 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 7.6 | 0.5 | 9.4 | 0.5 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 32.7 | 42.4 | 34.3 | 42.9 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | — | — | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | –40°C to 85°C | | | –40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP(1) | MAX | MIN | TYP(1) | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –100 µA | | 1.65 V to 3.6 V | $V_{CC}$ – 0.2 | | | $V_{CC}$ – 0.2 | | | V |
| | | $I_{OH}$ = –4 mA | | 1.65 V | 1.2 | | | 1.2 | | | |
| | | $I_{OH}$ = –8 mA | | 2.3 V | 1.7 | | | 1.7 | | | |
| | | $I_{OH}$ = –12 mA | | 2.7 V | 2.2 | | | 2.2 | | | |
| | | | | 3 V | 2.4 | | | 2.4 | | | |
| | | $I_{OH}$ = –24 mA | | 3 V | 2.2 | | | 2.2 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 µA | | 1.65 V to 3.6 V | | | 0.2 | | | 0.2 | V |
| | | $I_{OL}$ = 4 mA | | 1.65 V | | | 0.45 | | | 0.45 | |
| | | $I_{OL}$ = 8 mA | | 2.3 V | | | 0.7 | | | 0.7 | |
| | | $I_{OL}$ = 12 mA | | 2.7 V | | | 0.4 | | | 0.4 | |
| | | $I_{OL}$ = 24 mA | | 3 V | | | 0.55 | | | 0.60 | |
| $I_I$ | | $V_I$ = 0 to 5.5 V | | 3.6 V | | | ±5 | | | ±5 | µA |
| $I_{off}$ | | $V_I$ or $V_O$ = 5.5 V | | 0 | | | ±10 | | | ±10 | µA |
| $I_{OZ}$ | | $V_O$ = 0 to 5.5 V | | 3.6 V | | | ±10 | | | ±10 | µA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND | $I_O$ = 0 | 3.6 V | | | 10 | | | 10 | µA |
| | | 3.6 V ≤ $V_I$ ≤ 5.5 V(2) | | | | | | | | 10 | |
| $\Delta I_{CC}$ | | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | 2.7 V to 3.6 V | | | 500 | | | 500 | µA |
| $C_i$ | Control inputs | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 5 | | | | | pF |
| | Data inputs | | | | | 4 | | | | | |
| $C_o$ | | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | 7 | | | | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
(2) This applies in the disabled state only.

## 7.6 Switching Characteristics, –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | | 5.5 | | 5.7 | | 7.1 | 1 | 6.7 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | 9.6 | | 8.9 | | 8.5 | 1 | 7.3 | ns |
| $t_{dis}$ | $\overline{OE}$ | Y | | 8.4 | | 7.9 | | 7.3 | 1.8 | 6.7 | ns |
| $t_{sk(o)}$ | | | | 1 | | 1 | | 1 | | 1 | ns |

## 7.7 Switching Characteristics, –40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | | 5.8 | | 6.2 | | 8.3 | 1 | 7.9 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | 9.9 | | 9.8 | | 9.7 | 1 | 8.5 | ns |
| $t_{dis}$ | $\overline{OE}$ | Y | | 8.6 | | 8.55 | | 8.5 | 1.8 | 7.9 | ns |
| $t_{sk(o)}$ | | | | 1 | | 1 | | 1 | | 1.5 | ns |

## 7.8 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance per buffer/driver | Outputs enabled | f = 10 MHz | 20 | 22 | 24 | pF |
| | | Outputs disabled | | 3 | 4 | 5 | |

## 7.9 Typical Characteristics

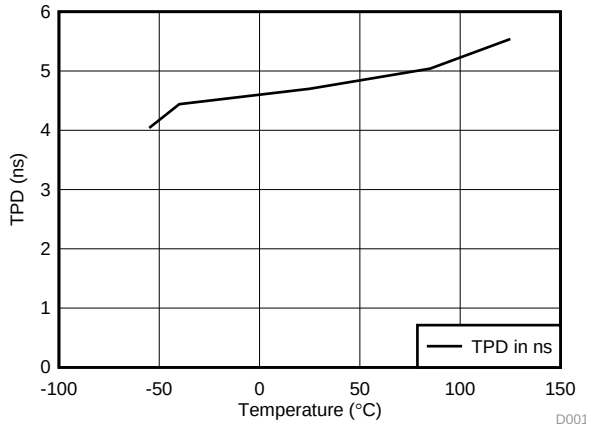



**Figure 1. TPD vs Temperature**

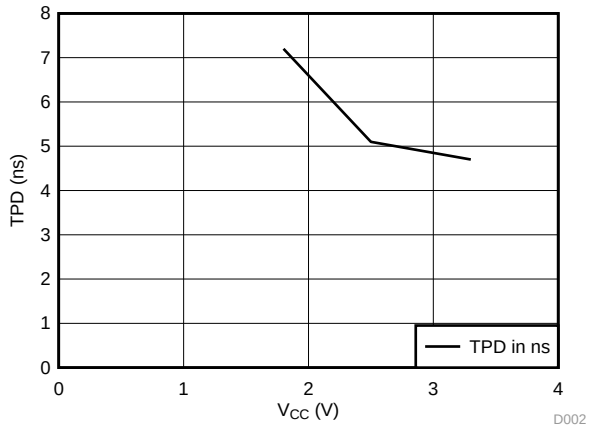
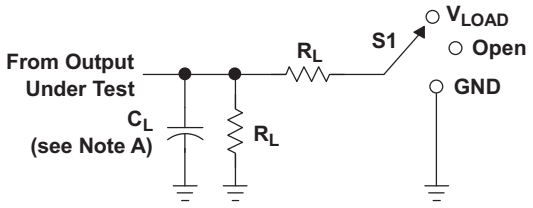



**Figure 2. TPD vs $V_{CC}$**

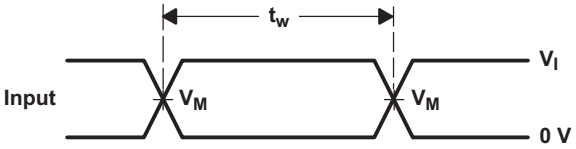
# 8 Parameter Measurement Information



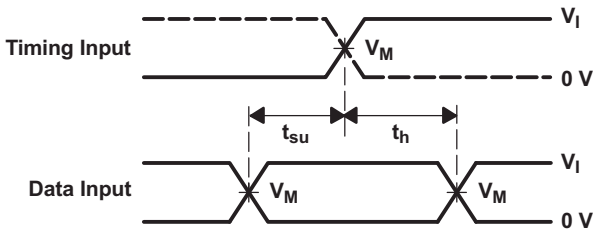

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

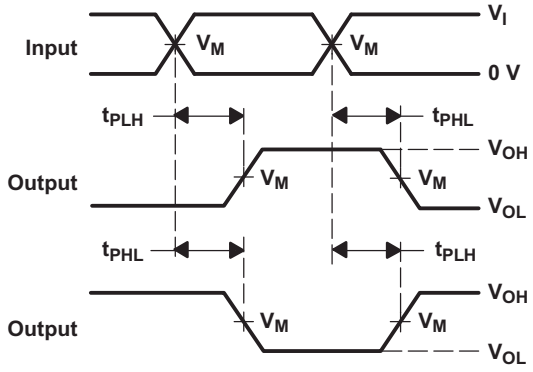
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V ± 0.3 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



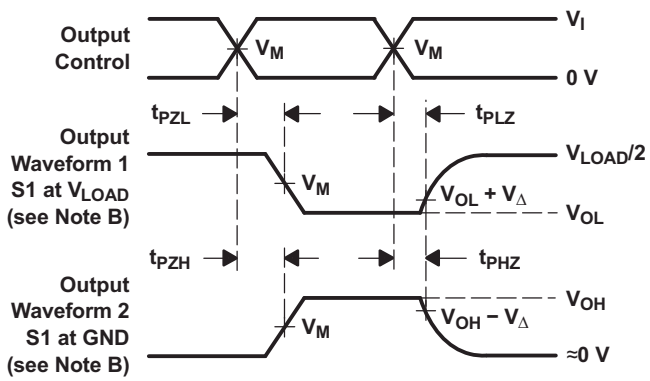

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit And Voltage Waveforms**

# 9 Detailed Description

## 9.1 Overview

This 10-bit buffer/bus driver is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

The SN74LVC827A provides a high-performance bus interface for wide data paths or buses carrying parity.

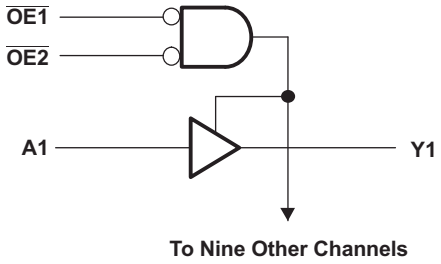
The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all ten outputs are in the high-impedance state. The SN74LVC827A provides true data at its outputs.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## 9.2 Functional Block Diagram




## 9.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65 V to 3.6 V
- Allows down voltage translation
  - Inputs accept voltages to 5.5 V
- $I_{off}$ feature
  - Allows voltages on the inputs and outputs when $V_{CC}$ is 0 V

## 9.4 Device Functional Modes

**Table 1. Function Table**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The SN74LVC827A is a high-drive CMOS device that can be used for a multitude of bus interface type applications where the data needs to be retained. It can produce 24 mA of drive current at 3.3 V, thus making this device ideal for driving multiple outputs and for high-speed applications up to 150 MHz. The inputs are 5.5-V tolerant, allowing the device to translate down to $V_{CC}$.

## 10.2 Typical Application

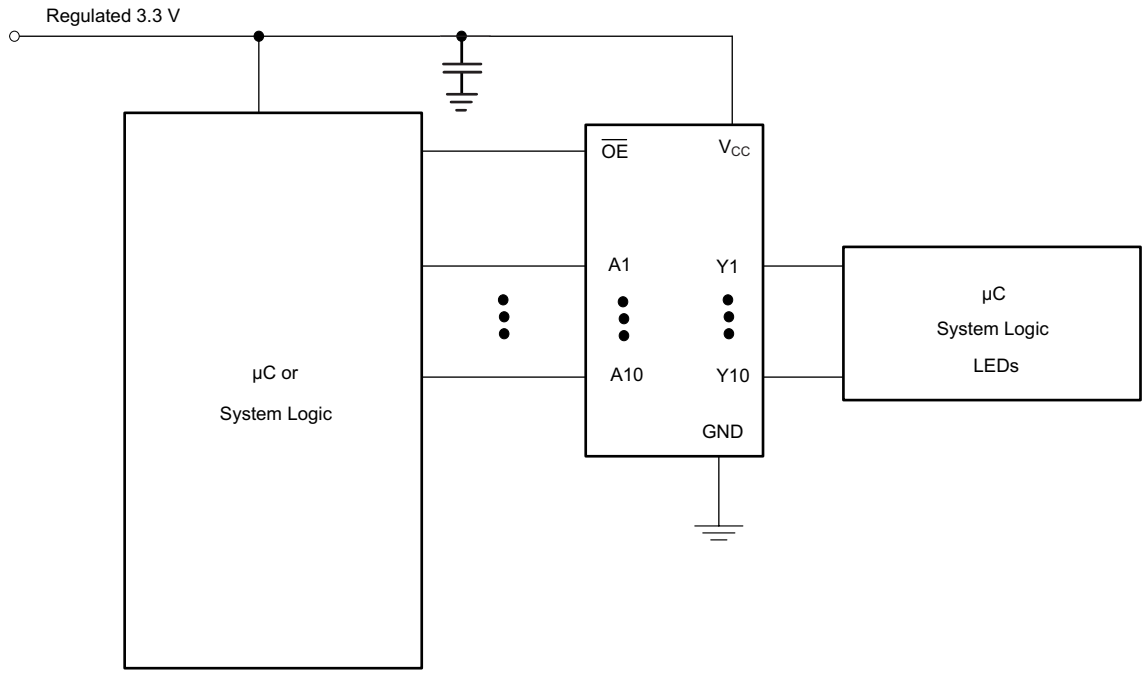



**Figure 4. Typical Application Schematic**

### 10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifcations, see Δt/ΔV in the *Recommended Operating Conditions* table.
   - For specified high and low levels, see $V_{IH}$ and $V_{IL}$ in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC}$.
2. Recommend Output Conditions:
   - Load currents should not exceed 50 mA per output and 100 mA total for the part.
   - Outputs should not be pulled above $V_{CC}$.

## Typical Application (continued)

### 10.2.3 Application Curves

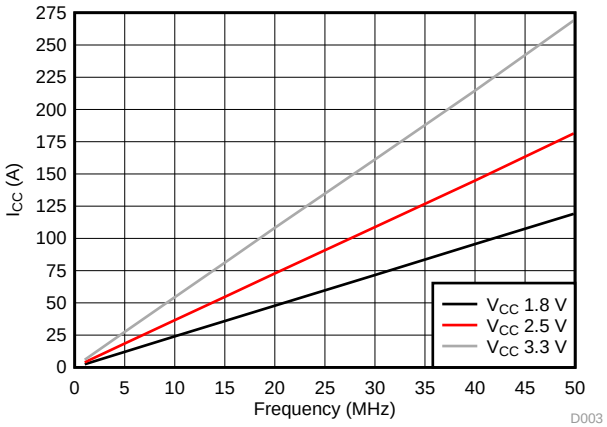



**Figure 5. $I_{CC}$ vs Frequency**

## 11 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the *Recommended Operating Conditions* table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended and if there are multiple $V_{CC}$ pins then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

# 12 Layout

## 12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Recommended Operating Conditions are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver.

## 12.2 Layout Example

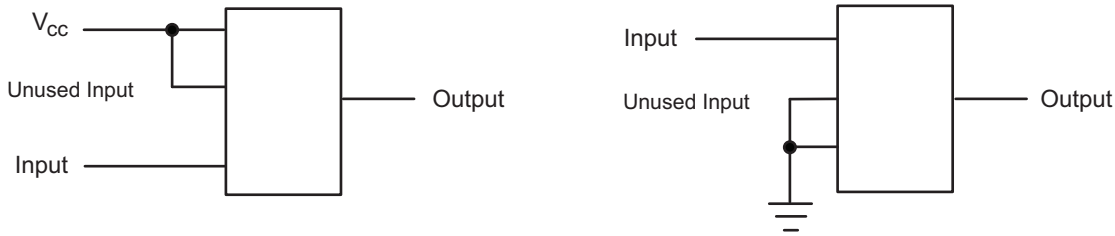



**Figure 6. Layout Diagram**

# 13 Device and Documentation Support

## 13.1 Trademarks

All trademarks are the property of their respective owners.

## 13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC827ADBR | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC827A | Samples |
| SN74LVC827ADBRE4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC827A | Samples |
| SN74LVC827ADBRG4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC827A | Samples |
| SN74LVC827ADGVR | ACTIVE | TVSOP | DGV | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC827A | Samples |
| SN74LVC827ADGVRG4 | ACTIVE | TVSOP | DGV | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC827A | Samples |
| SN74LVC827ADW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC827A | Samples |
| SN74LVC827ADWG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC827A | Samples |
| SN74LVC827ADWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC827A | Samples |
| SN74LVC827APW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC827A | Samples |
| SN74LVC827APWG4 | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC827A | Samples |
| SN74LVC827APWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC827A | Samples |
| SN74LVC827APWT | ACTIVE | TSSOP | PW | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC827A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

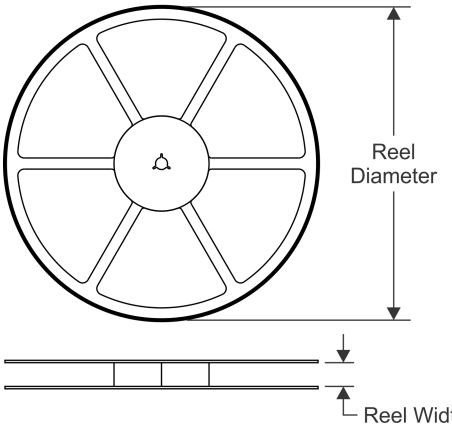
**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

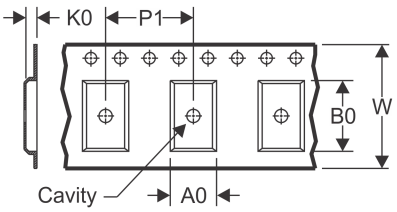
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

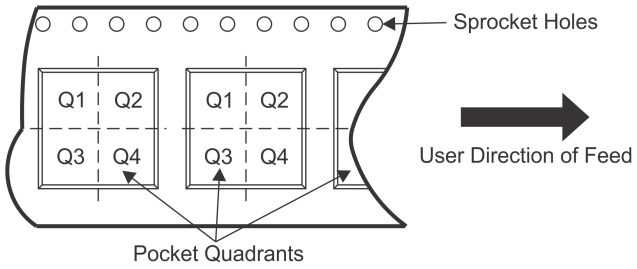



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

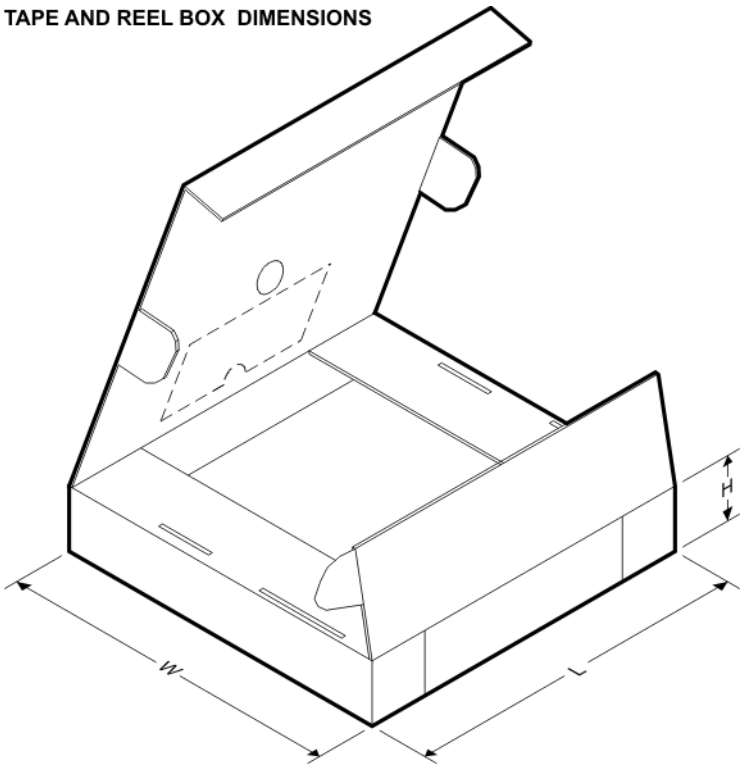
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC827ADBR | SSOP | DB | 24 | 2000 | 330.0 | 16.4 | 8.2 | 8.8 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC827ADGVR | TVSOP | DGV | 24 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC827ADWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVC827APWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LVC827APWT | TSSOP | PW | 24 | 250 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

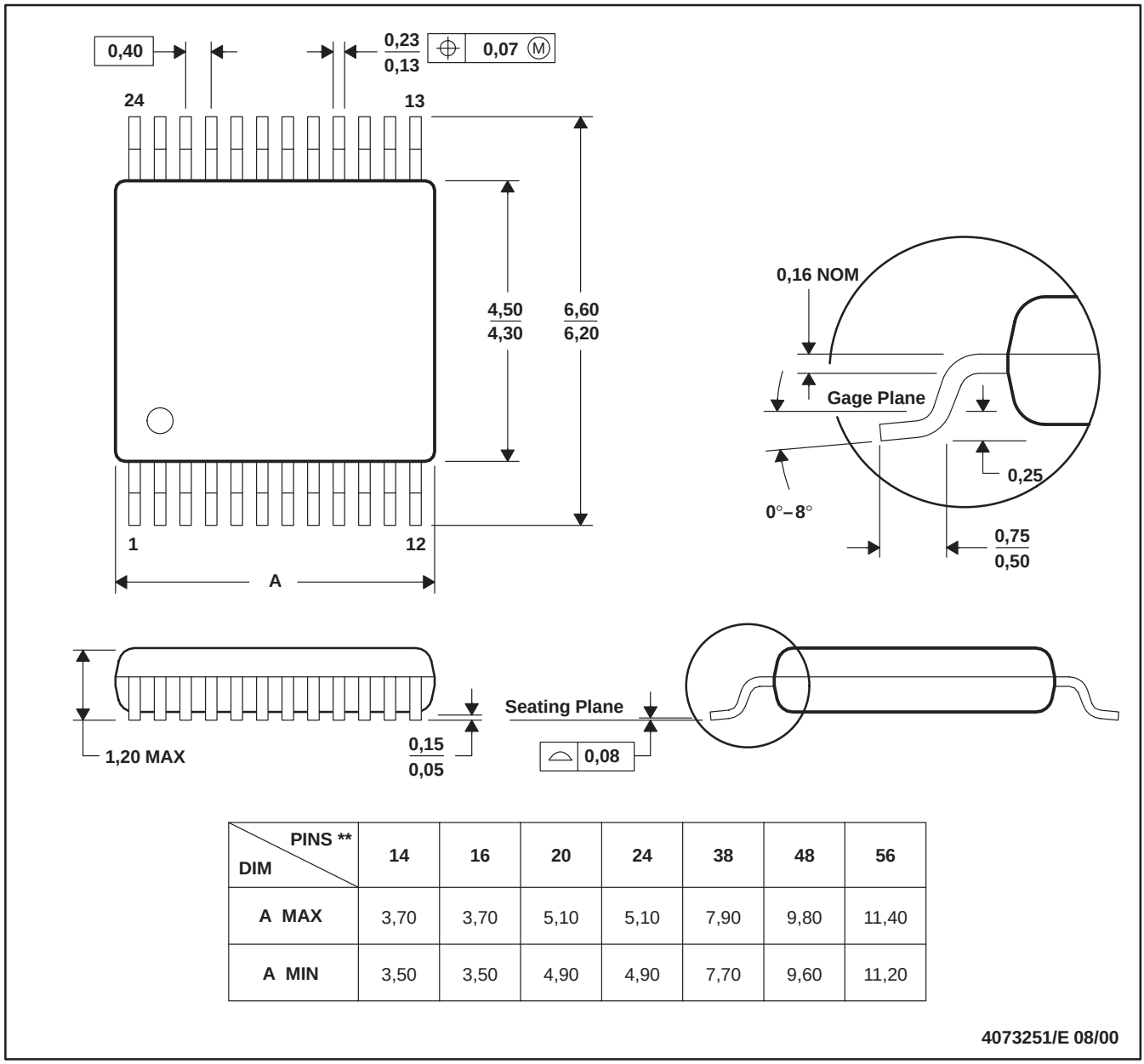



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC827ADBR | SSOP | DB | 24 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVC827ADGVR | TVSOP | DGV | 24 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LVC827ADWR | SOIC | DW | 24 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVC827APWR | TSSOP | PW | 24 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVC827APWT | TSSOP | PW | 24 | 250 | 367.0 | 367.0 | 38.0 |

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

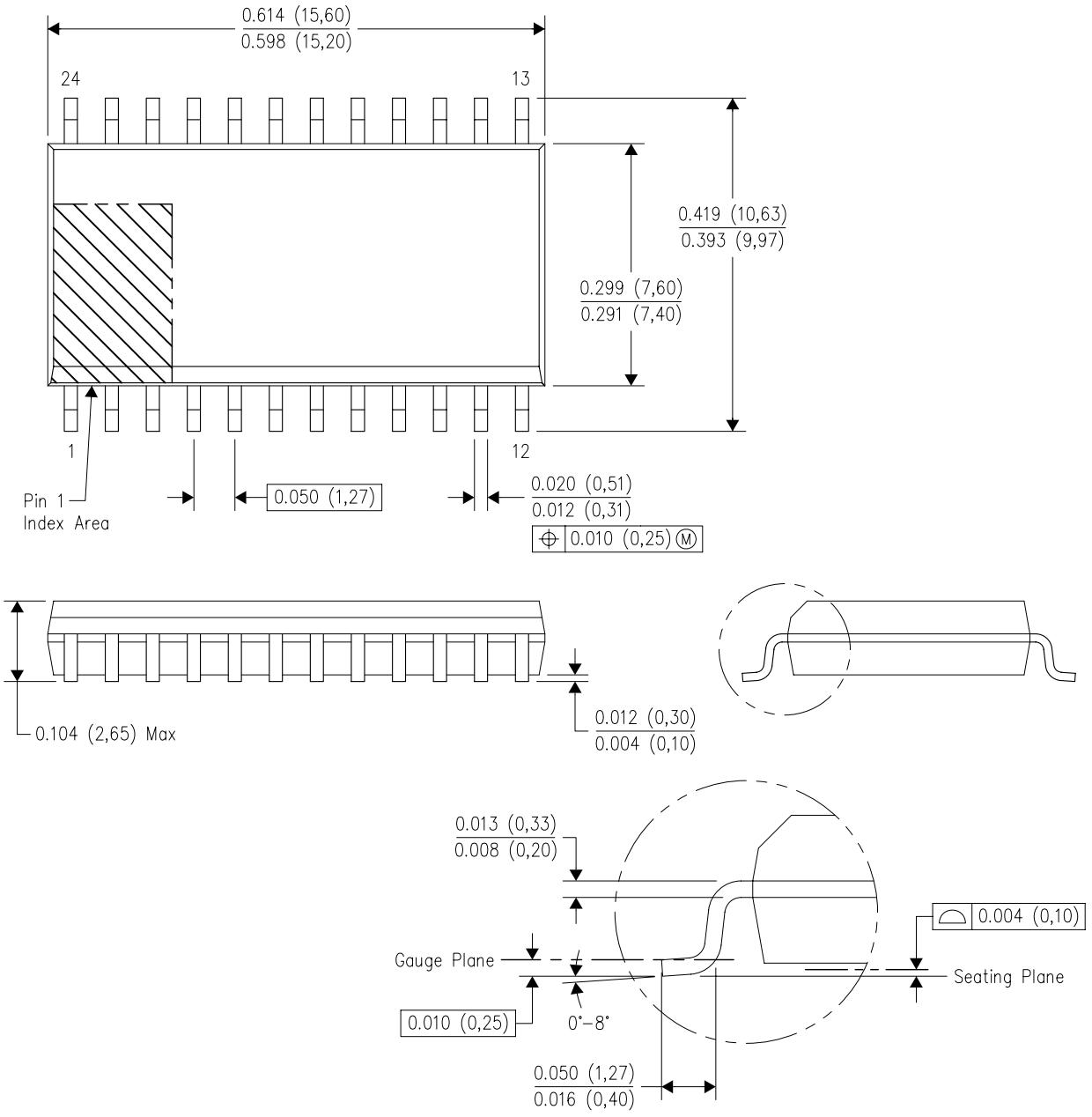



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

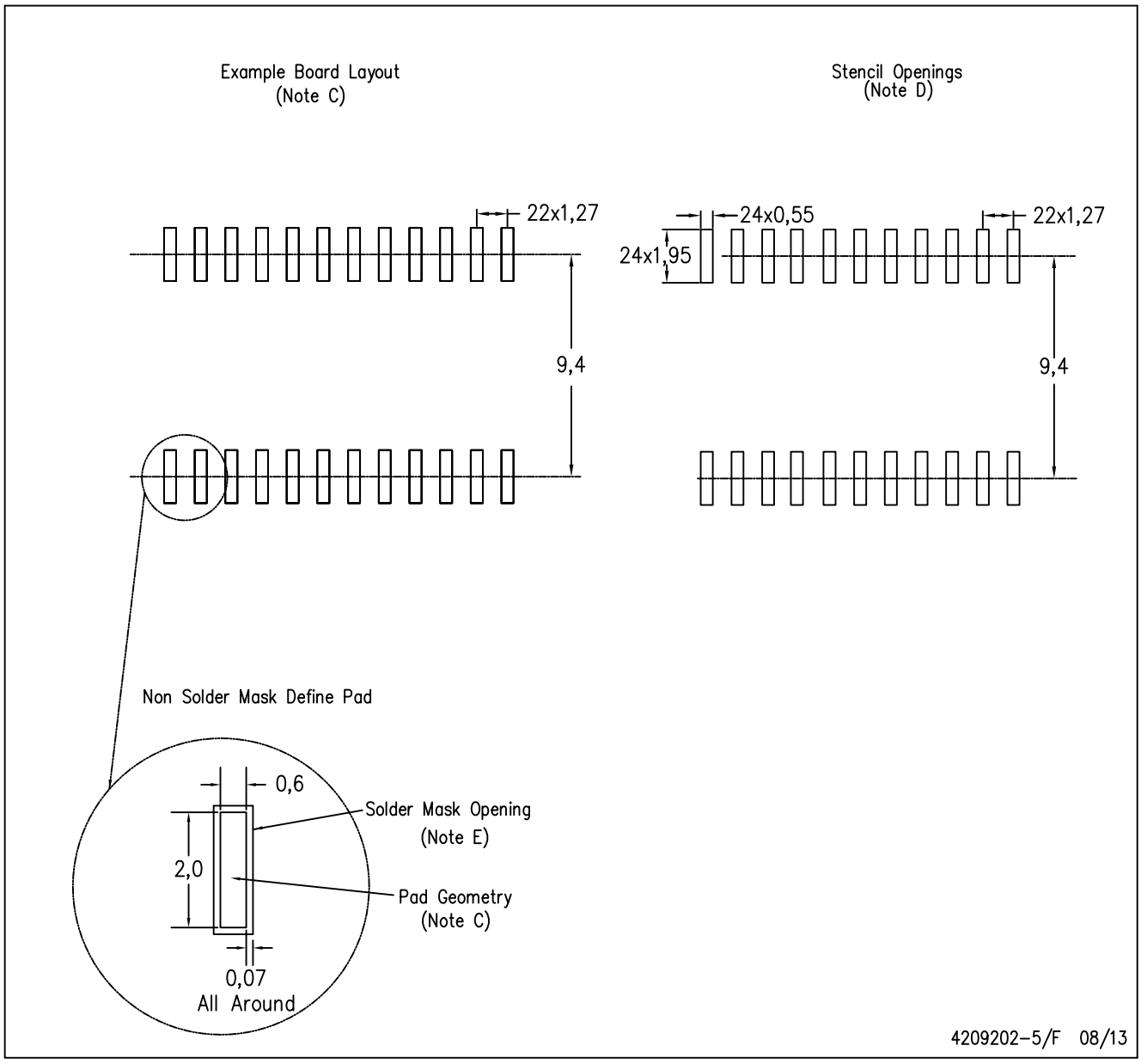
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



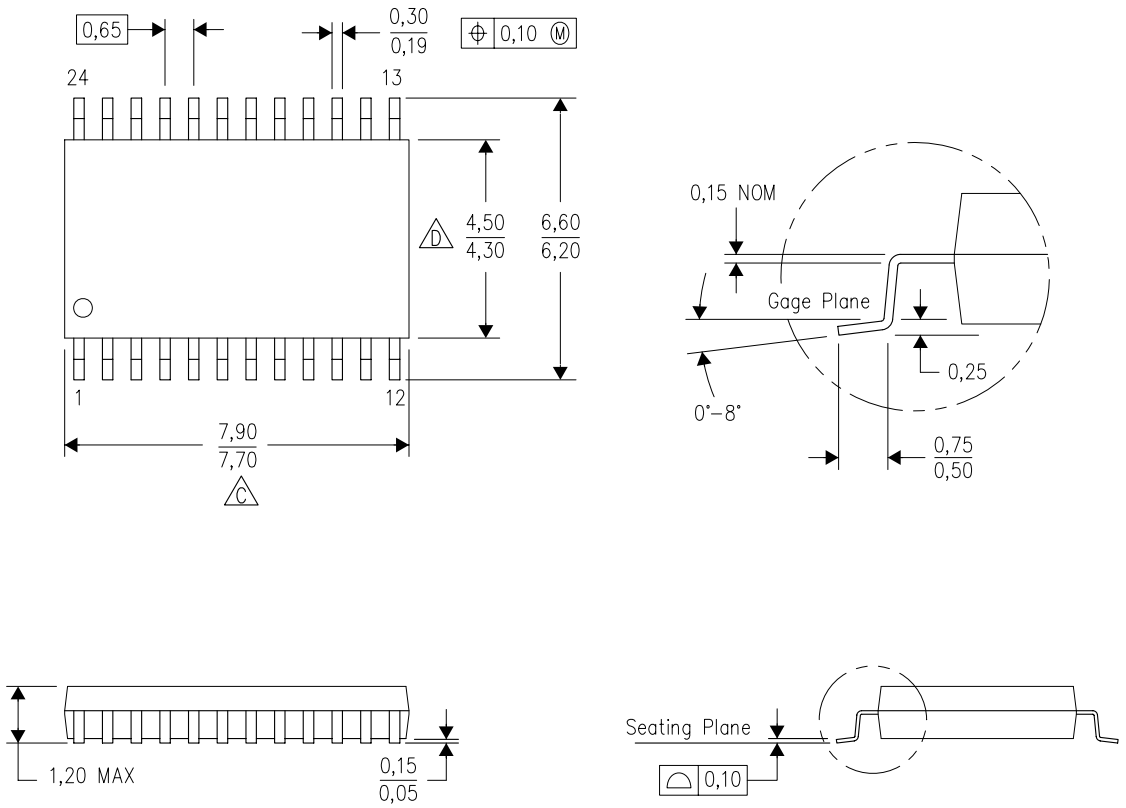

NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

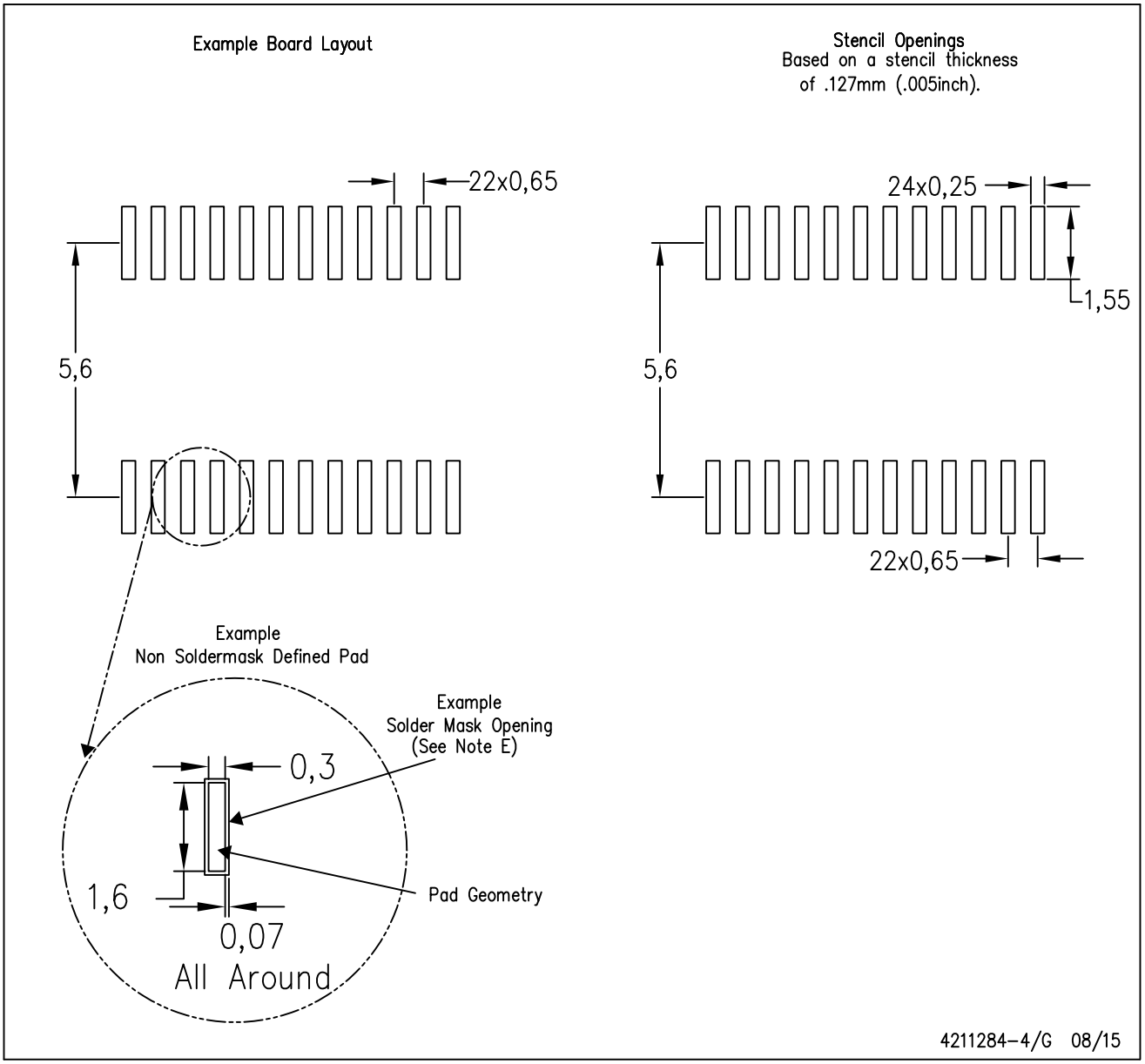
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE




4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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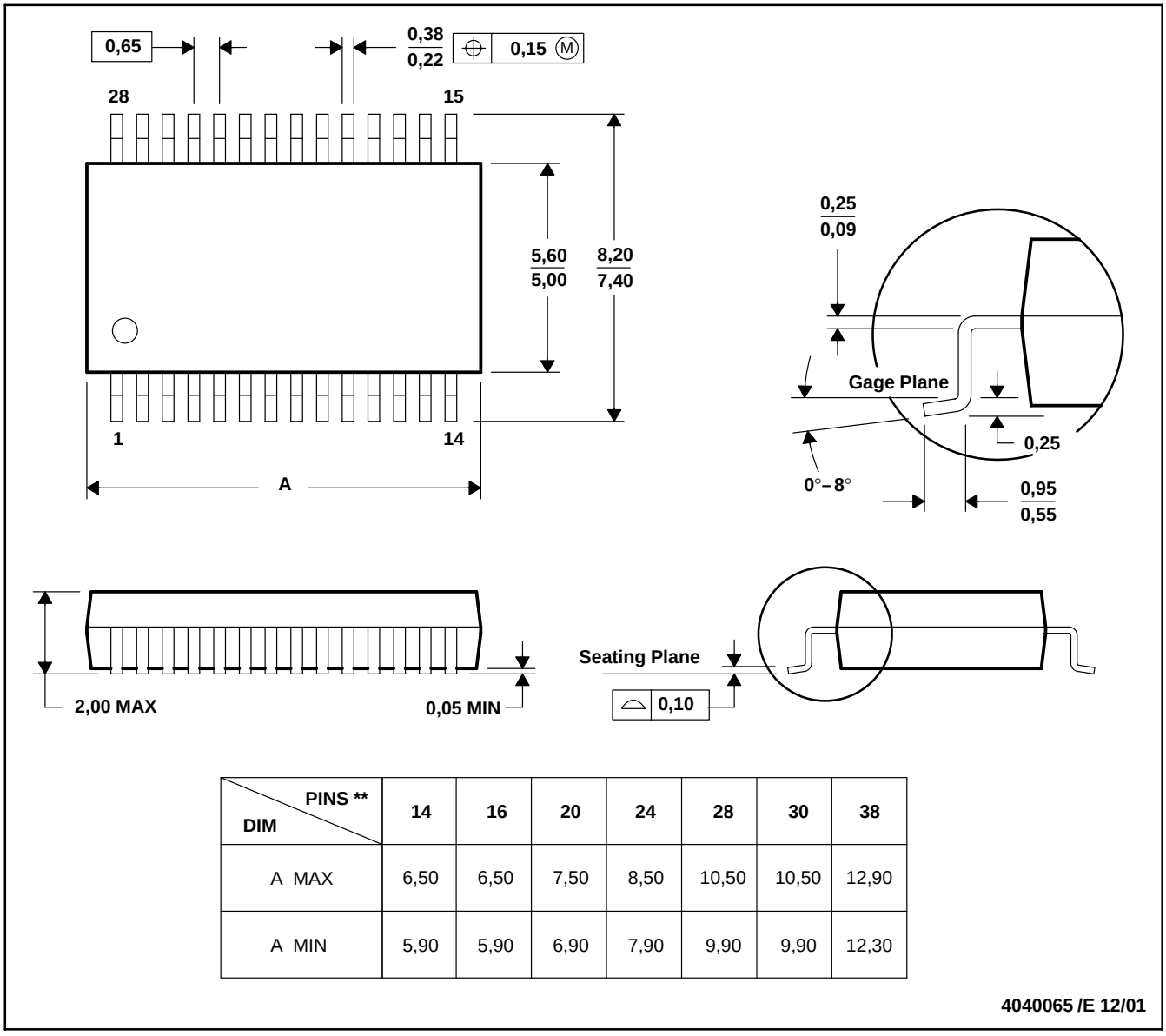
**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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