SN74LVC8T245 8-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and 3-State Outputs

1 Features

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All Are in the High-Impedance State
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  – 4000-V Human-Body Model (A114-A)
  – 100-V Machine Model (A115-A)
  – 1000-V Charged-Device Model (C101)

2 Applications

- Personal Electronic
- Industrial
- Enterprise
- Telecom

3 Description

This 8-bit noninverting bus transceiver uses two separate configurable power-supply rails. The SN74LVC8T245 is optimized to operate with V_{CCA} and V_{CCB} set at 1.65 V to 5.5 V. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5.5-V voltage nodes.

The SN74LVC8T245 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

The SN74LVC8T245 is designed so that the control pins (DIR and $\overline{OE}$) are supplied by V_{CCA}.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC8T245	SSOP (24)	8.20 mm x 5.30 mm
	SSOP (24)	8.65 mm x 3.90 mm
	TSSOP (24)	7.80 mm x 4.40 mm
	TVSOP (24)	5.00 mm x 4.40 mm
	VQFN (24)	5.50 mm x 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Logic Diagram (Positive Logic)

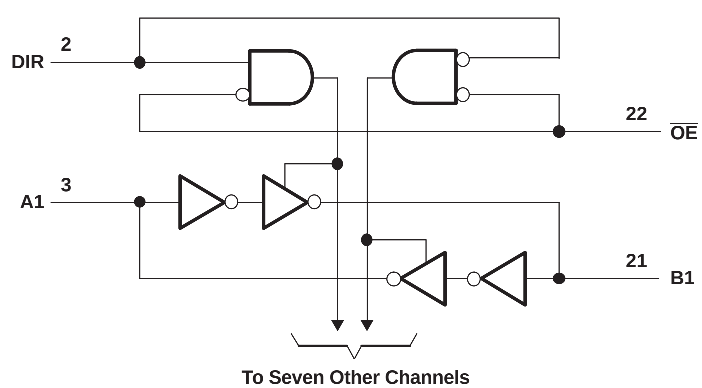


Table of Contents

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2005) to Revision B	Page
• Added the list of Application, Pin Functions table, Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.	1
• Changed Feature From: 200-V Machine Model (A115-A) To: 100-V Machine Model (A115-A)	1

Changes from Original (June 2005) to Revision A	Page
• Changed the device From: Product Preview To: Production	1

6 Description (continued)

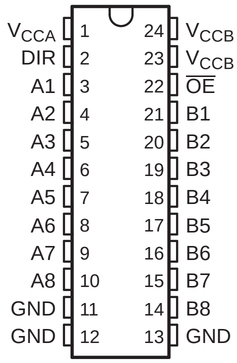
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, all outputs are in the high-impedance state.

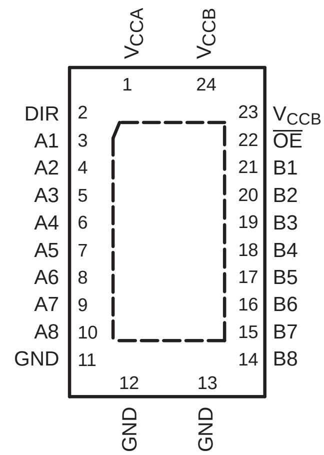
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7 Pin Configuration and Functions

DB, DBQ, DGV, OR PW PACKAGE (TOP VIEW)



RHL PACKAGE (TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A1	3	I/O	Input/output A1. Referenced to V_{CCA}.
A2	4	I/O	Input/output A2. Referenced to V_{CCA}.
A3	5	I/O	Input/output A3. Referenced to V_{CCA}.
A4	6	I/O	Input/output A4. Referenced to V_{CCA}.
A5	7	I/O	Input/output A5. Referenced to V_{CCA}.
A6	8	I/O	Input/output A6. Referenced to V_{CCA}.
A7	9	I/O	Input/output A7. Referenced to V_{CCA}.
A8	10	I/O	Input/output A8. Referenced to V_{CCA}.
B1	21	I/O	Input/output B1. Referenced to V_{CCB}.
B2	20	I/O	Input/output B2. Referenced to V_{CCB}.
B3	19	I/O	Input/output B3. Referenced to V_{CCB}.
B4	18	I/O	Input/output B4. Referenced to V_{CCB}.
B5	17	I/O	Input/output B5. Referenced to V_{CCB}.
B6	16	I/O	Input/output B6. Referenced to V_{CCB}.
B7	15	I/O	Input/output B7. Referenced to V_{CCB}.
B8	14	I/O	Input/output B8. Referenced to V_{CCB}.
DIR	2	I	Direction-control signal.
GND	11, 12, 13	G	Ground
$\overline{OE}$	22	I	3-state output-mode enables. Pull $\overline{OE}$ high to place all outputs in 3-state mode. Referenced to V_{CCA}.
V_{CCA}	1	P	A-port supply voltage. 1.65 V ≤ V_{CCA} ≤ 5.5 V
V_{CCB}	23, 24	P	B-port supply voltage. 1.65 V ≤ V_{CCA} ≤ 5.5 V

8 Specifications

8.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Supply voltage range, V_{CCA}, V_{CCB}		–0.5	6.5	V
V_I	Input voltage range[2]	I/O ports (A port)	–0.5	6.5	V
		I/O ports (B port)	–0.5	6.5	
		Control inputs	–0.5	6.5	
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]	A port	–0.5	6.5	V
		B port	–0.5	6.5	
V_O	Voltage range applied to any output in the high or low state[2] [3]	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CCA}, V_{CCB}, and GND			±100	mA

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.

8.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	–4000	4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	–1000	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions[(1)] [(2)] [(3)] [(4)]

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.65	5.5	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs[(5)]	1.65 V to 1.95 V		V_{CCI} × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V_{CCI} × 0.7		
V_{IL}	Low-level input voltage	Data inputs[(5)]	1.65 V to 1.95 V			V_{CCI} × 0.35	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			V_{CCI} × 0.3	
V_{IH}	High-level input voltage	Control inputs (referenced to V_{CCA})[(6)]	1.65 V to 1.95 V		V_{CCA} × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V_{CCA} × 0.7		
V_{IL}	Low-level input voltage	Control inputs (referenced to V_{CCA})[(6)]	1.65 V to 1.95 V			V_{CCA} × 0.35	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			V_{CCA} × 0.3	
V_I	Input voltage	Control inputs			0	5.5	V
$V_{I/O}$	Input/output voltage	Active state			0	V_{CCO}	V
		3-State			0	5.5	V
I_{OH}	High-level output current			1.65 V to 1.95 V		–4	mA
				2.3 V to 2.7 V		–8	
				3 V to 3.6 V		–24	
				4.5 V to 5.5 V		–32	
I_{OL}	Low-level output current			1.65 V to 1.95 V		4	mA
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		24	
				4.5 V to 5.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	Data inputs	1.65 V to 1.95 V			20	ns/V
			2.3 V to 2.7 V			20	
			3 V to 3.6 V			10	
			4.5 V to 5.5 V			5	
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the data input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V_{CCI} or GND) to ensure proper device operation and minimize power. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs,* literature number SCBA004.
(4) All unused control inputs must be held at V_{CCA} or GND to ensure proper device operation and minimize power comsumption.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
(6) For V_{CCA} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

8.4 Thermal Information DB, DBQ and DGV

THERMAL METRIC(1)		DB	DBQ	DGV	UNIT
		24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88.5	81.2	91.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.7	44.8	23.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	44.1	34.5	44.5	
ψ_{JT}	Junction-to-top characterization parameter	12.8	9.5	0.6	
ψ_{JB}	Junction-to-board characterization parameter	43.6	37.2	44.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Thermal Information PW and RHL

THERMAL METRIC(1)		PW	RHL	UNIT
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.6	37.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.6	38.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	45.3	15.2	
ψ_{JT}	Junction-to-top characterization parameter	1.3	0.7	
ψ_{JB}	Junction-to-board characterization parameter	44.8	15.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	4.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.6 Electrical Characteristics(1) (2)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	MIN	TYP	MAX	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 μA,	$V_I = V_{IH}$	1.65 V to 4.5 V	1.65 V to 4.5 V				V_{CCO} – 0.1		V
		I_{OH} = –4 mA,	$V_I = V_{IH}$	1.65 V	1.65 V				1.2		
		I_{OH} = –8 mA,	$V_I = V_{IH}$	2.3 V	2.3 V				1.9		
		I_{OH} = –24 mA,	$V_I = V_{IH}$	3 V	3 V				2.4		
		I_{OH} = –32 mA,	$V_I = V_{IH}$	4.5 V	4.5 V				3.8		
V_{OL}		I_{OL} = 100 μA,	$V_I = V_{IL}$	1.65 V to 4.5 V	1.65 V to 4.5 V					0.1	V
		I_{OL} = 4 mA,	$V_I = V_{IL}$	1.65 V	1.65 V					0.45	
		I_{OL} = 8 mA,	$V_I = V_{IL}$	2.3 V	2.3 V					0.3	
		I_{OL} = 24 mA,	$V_I = V_{IL}$	3 V	3 V					0.55	
		I_{OL} = 32 mA,	$V_I = V_{IL}$	4.5 V	4.5 V					0.55	
I_I	DIR	$V_I = V_{CCA}$ or GND		1.65 V to 5.5 V	1.65 V to 5.5 V			±1		±2	μA
I_{off}	A or B port	V_I or V_O = 0 to 5.5 V		0 V	0 to 5.5 V			±1		±2	μA
				0 to 5.5 V	0 V			±1		±2	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND, $\overline{OE} = V_{IH}$		1.65 V to 5.5 V	1.65 V to 5.5 V			±1		±2	μA
I_{CCA}		$V_I = V_{CCI}$ or GND,	$I_O = 0$	1.65 V to 5.5 V	1.65 V to 5.5 V					15	μA
				5 V	0 V					15	
				0 V	5 V					–2	
I_{CCB}		$V_I = V_{CCI}$ or GND,	$I_O = 0$	1.65 V to 5.5 V	1.65 V to 5.5 V					15	μA
				5 V	0 V					–2	
				0 V	5 V					15	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND,	$I_O = 0$	1.65 V to 5.5 V	1.65 V to 5.5 V					25	μA
ΔI_{CCA}	A port	One A port at V_{CCA} – 0.6 V, DIR at V_{CCA}, B port = open		3 V to 5.5 V	3 V to 5.5 V					50	μA
	DIR	DIR at V_{CCA} – 0.6 V, B port = open, A port at V_{CCA} or GND								50	
ΔI_{CCB}	B port	One B port at V_{CCB} – 0.6 V, DIR at GND, A port = open		3 V to 5.5 V	3 V to 5.5 V					50	μA
C_i	Control inputs	$V_I = V_{CCA}$ or GND		3.3 V	3.3 V		4			5	pF
C_{io}	A or B port	$V_O = V_{CCA/B}$ or GND		3.3 V	3.3 V		8.5			10	pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.

8.7 Switching Characteristics, V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	A	B	1.7	21.9	1.3	9.2	1	7.4	0.8	7.1	ns
t_{PLH}, t_{PHL}	B	A	0.9	23.8	0.8	23.6	0.7	23.4	0.7	23.4	ns
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	1.5	29.6	1.5	29.4	1.5	29.3	1.4	29.2	ns
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	2.4	32.2	1.9	13.1	1.7	12	1.3	10.3	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	A	0.4	24	0.4	23.8	0.4	23.7	0.4	23.7	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	B	1.8	32	1.5	16	1.2	12.6	0.9	10.8	ns

8.8 Switching Characteristics, V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	A	B	1.5	21.4	1.2	9	0.8	6.2	0.6	4.8	ns
t_{PLH}, t_{PHL}	B	A	1.2	9.3	1	9.1	1	8.9	0.9	8.8	ns
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	1.4	9	1.4	9	1.4	9	1.4	9	ns
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	2.3	29.6	1.8	11	1.7	9.3	0.9	6.9	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	A	1	10.9	1	10.9	1	10.9	1	10.9	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	B	1.7	28.2	1.5	12.9	1.2	9.4	1	6.9	ns

8.9 Switching Characteristics, V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	A	B	1.5	21.2	1.1	8.8	0.8	6.3	0.5	4.4	ns
t_{PLH}, t_{PHL}	B	A	0.8	7.2	0.8	6.2	0.7	6.1	0.6	6	ns
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	1.6	8.2	1.6	8.2	1.6	8.2	1.6	8.2	ns
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	2.1	29	1.7	10.3	1.5	8.6	0.8	6.3	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	A	0.8	8.1	0.8	8.1	0.8	8.1	0.8	8.1	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	B	1.8	27.7	1.4	12.4	1.1	8.5	0.9	6.4	ns

8.10 Switching Characteristics, V_{CCA} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CCA} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	A	B	1.5	21.4	1	8.8	0.7	6	0.4	4.2	ns
t_{PLH}, t_{PHL}	B	A	0.7	7	0.4	4.8	0.3	4.5	0.3	4.3	ns
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	0.3	5.4	0.3	5.4	0.3	5.4	0.3	5.4	ns
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	2	28.7	1.6	9.7	1.4	8	0.7	5.7	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	A	0.7	6.4	0.7	6.4	0.7	6.4	0.7	6.4	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	B	1.5	27.6	1.3	11.4	1	8.1	0.9	6	ns

8.11 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	V_{CCA} = V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	2	2	2	3	pF
	B-port input, A-port output		12	13	13	16	
C_{pdB} (1)	A-port input, B-port output		13	13	14	16	
	B-port input, A-port output		2	2	2	3	

(1) Power dissipation capacitance per transceiver

8.12 Typical Characteristics

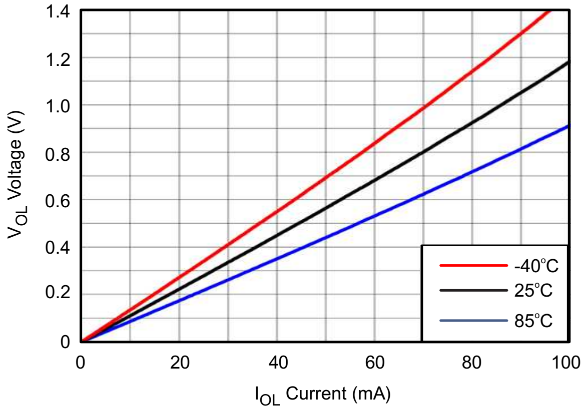


Figure 1. Voltage vs Current

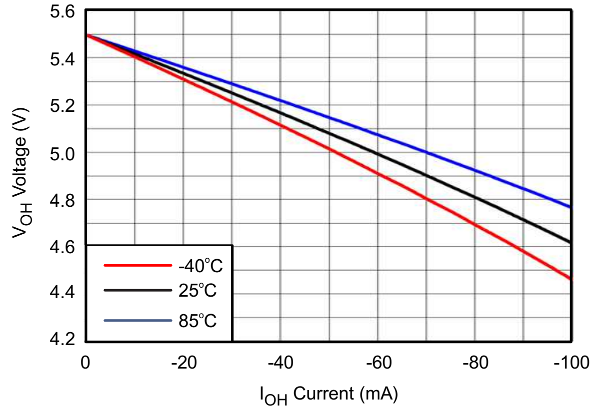
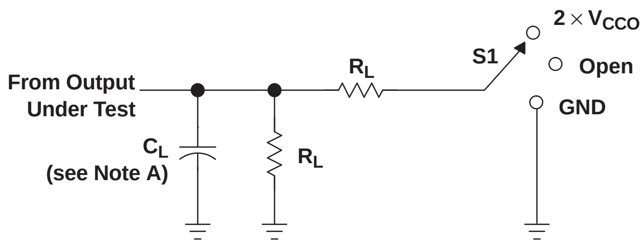


Figure 2. Voltage vs Current

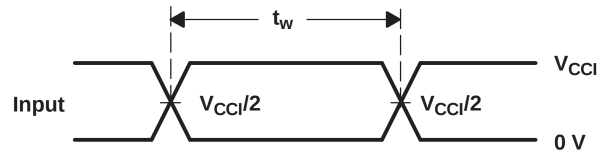
9 Parameter Measurement Information



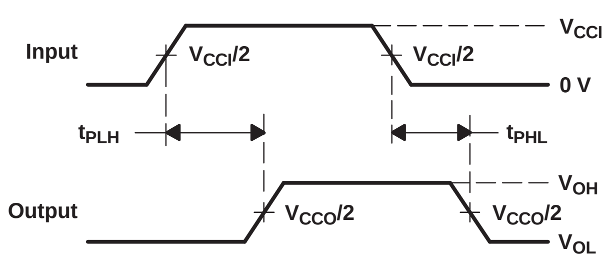
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

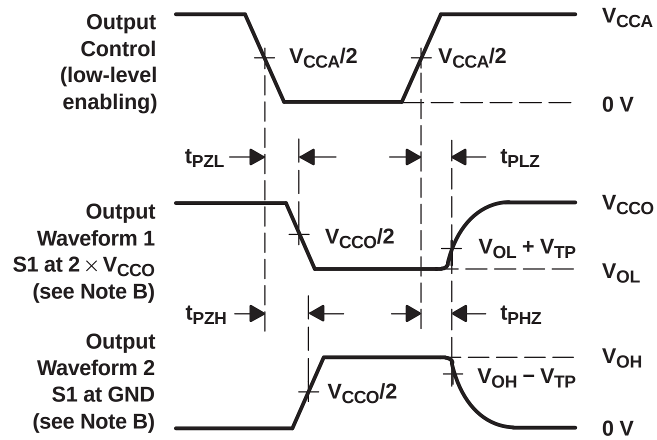
V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V
5 V ± 0.5 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.
J. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

10 Detailed Description

10.1 Overview

The SN74LVC8T245 is an 8-bit, dual supply non-inverting voltage level translation. Pin Ax and direction control pin are support by V_{CCA} and pin Bx is support by V_{CCB}. The A port is able to accept I/O voltages ranging from 1.65 V to 5.5 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A.

10.2 Functional Block Diagram

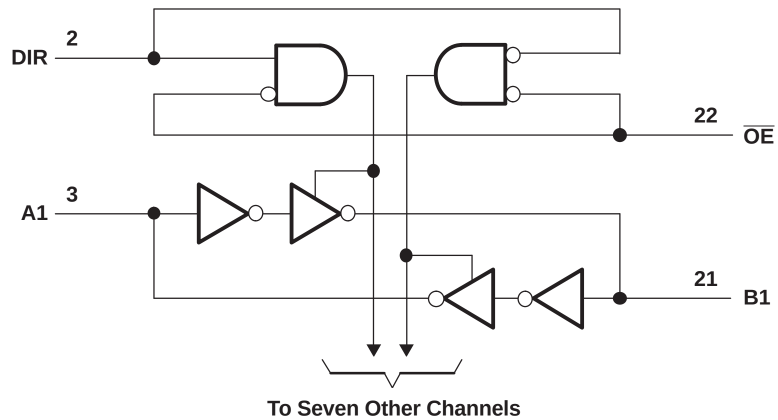


Figure 4. Logic Diagram (Positive Logic)

10.3 Feature Description

10.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.65 V and 5.5 V making the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, 3.3 V and 5 V).

10.3.2 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} prevents backflow current by disabling I/O output circuits when device is in partial-power-down mode.

10.4 Device Functional Modes

The SN74LVC8T245 is voltage level translator that can operate from 1.65 V to 5.5 V (V_{CCA}) and 1.65 V to 5.5 V (V_{CCB}). The signal translation between 1.65 V and 5.5 V requires direction control and output enable control. When $\overline{OE}$ is low and DIR is high, data transmission is from A to B. When $\overline{OE}$ is low and DIR is low, data transmission is from B to A. When $\overline{OE}$ is high, both output ports will be high-impedance.

Table 1. Function Table(1)
(Each 8-Bit Section)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The SN74LVC8T245 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The maximum output current can be up to 32 mA when device is powered by 5 V.

11.2 Typical Application

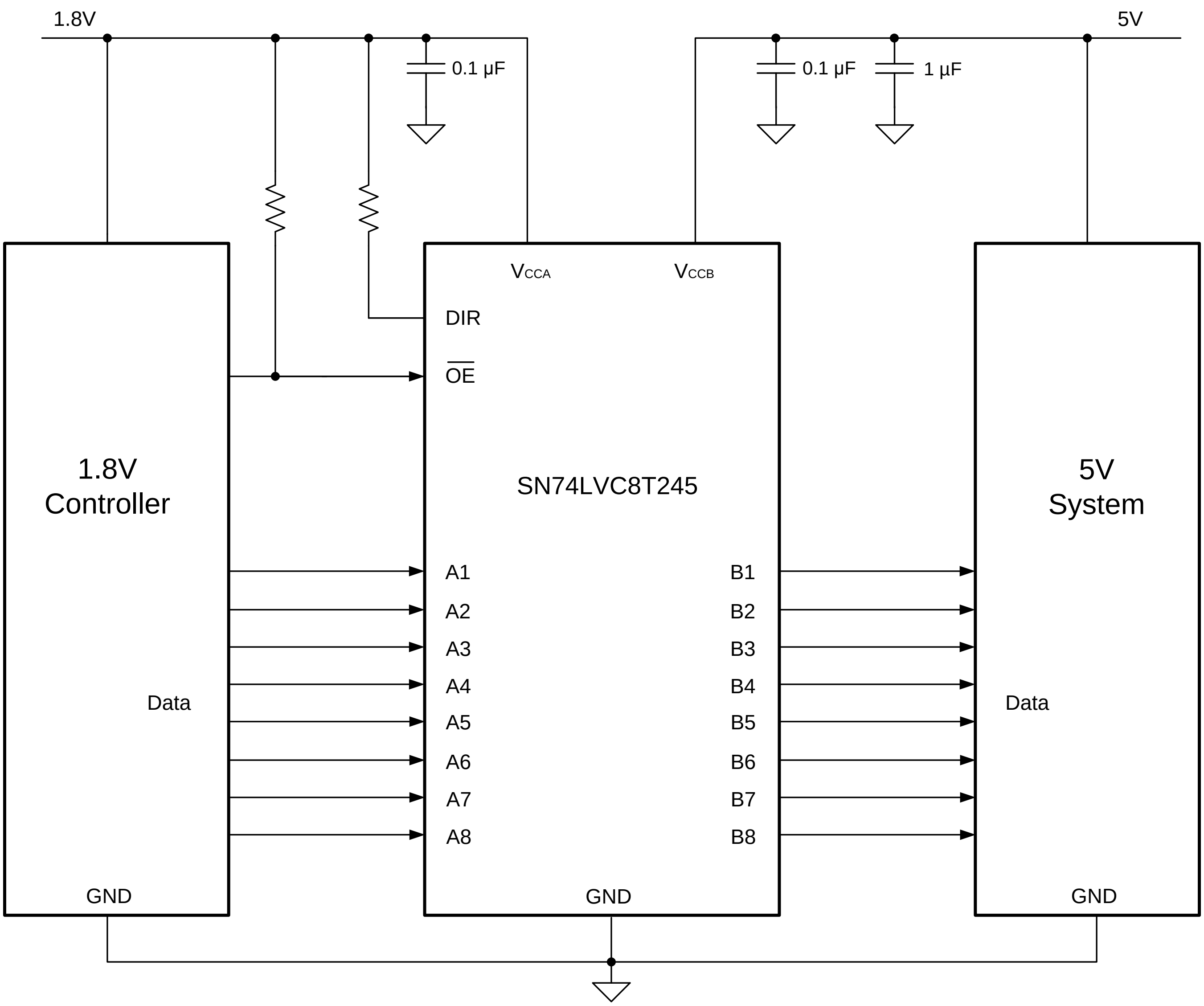


Figure 5. Typical Application Circuit

Typical Application (continued)

11.2.1 Design Requirements

For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

PARAMETERS	VALUES
Input voltage range	1.65 V to 5.5 V
Output voltage	1.65 V to 5.5 V

11.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74LVC8T245 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74LVC8T245 device is driving to determine the output voltage range.

11.2.3 Application Curve

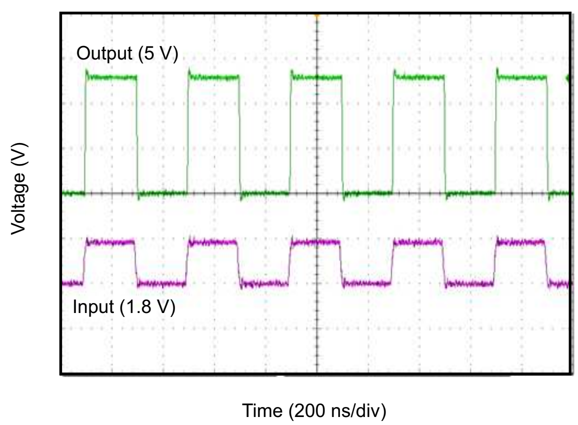


Figure 6. Translation Up (1.8 V to 5 V) at 2.5 MHz

12 Power Supply Recommendations

The SN74LVC8T245 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V and V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage bidirectional translation between any of the 1.8-V, 2.5 -V, 3.3-V and 5-V voltage nodes.

13 Layout

13.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors helps adjust rise and fall times of signals depending on the system requirements.

13.2 Layout Example

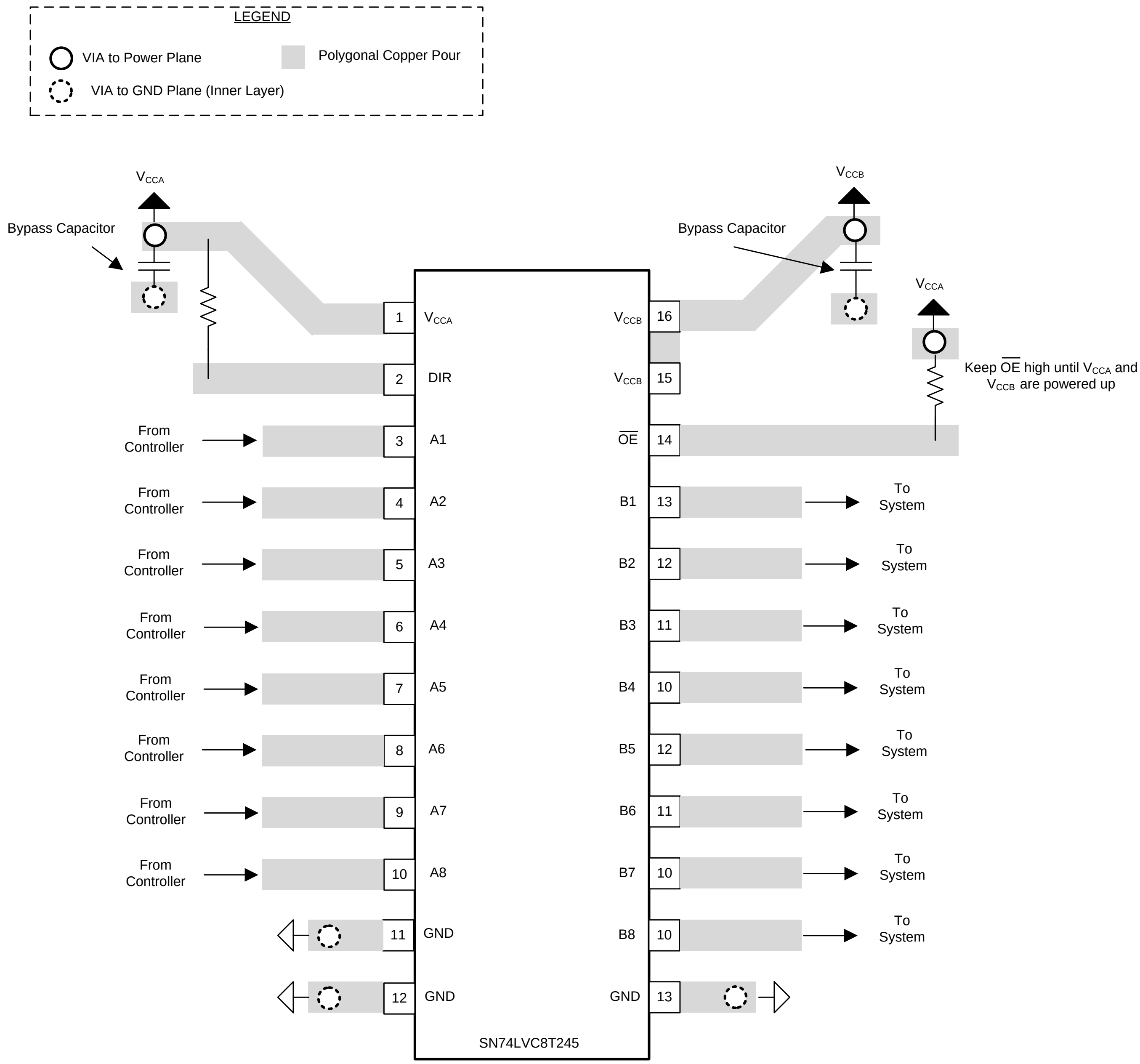


Figure 7. SN74LVC8T245 Layout

14 Device and Documentation Support

14.1 Trademarks

All trademarks are the property of their respective owners.

14.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVC8T245DBQRG4	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVC8T245	Samples
74LVC8T245RHLRG4	ACTIVE	VQFN	RHL	24	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NH245	Samples
SN74LVC8T245DBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVC8T245	Samples
SN74LVC8T245DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245	Samples
SN74LVC8T245DBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245	Samples
SN74LVC8T245DGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245	Samples
SN74LVC8T245DGVRG4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245	Samples
SN74LVC8T245DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC8T245	Samples
SN74LVC8T245DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC8T245	Samples
SN74LVC8T245NSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC8T245	Samples
SN74LVC8T245PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245	Samples
SN74LVC8T245PWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245	Samples
SN74LVC8T245PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245	Samples
SN74LVC8T245PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245	Samples
SN74LVC8T245PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245	Samples
SN74LVC8T245PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245	Samples
SN74LVC8T245RHLR	ACTIVE	VQFN	RHL	24	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NH245	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC8T245 :

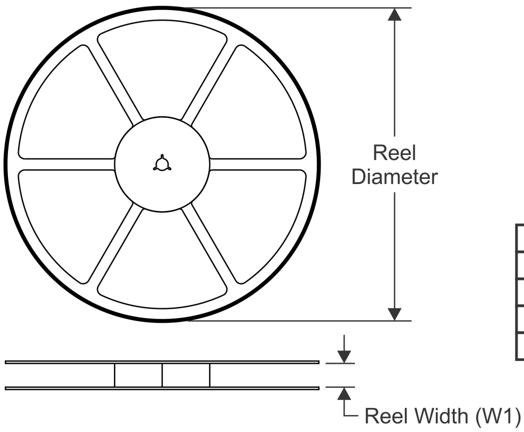
- Automotive: SN74LVC8T245-Q1
- Enhanced Product: SN74LVC8T245-EP

NOTE: Qualified Version Definitions:

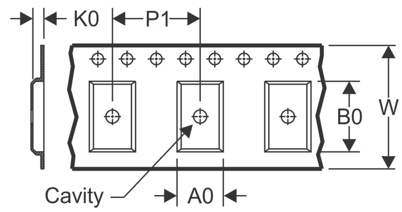
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

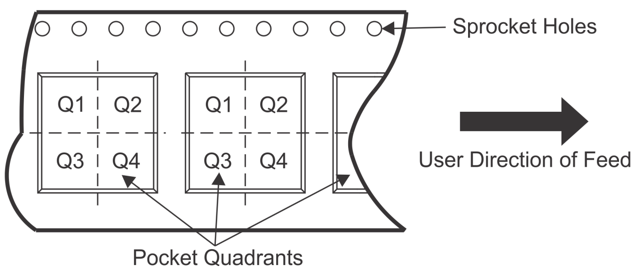


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

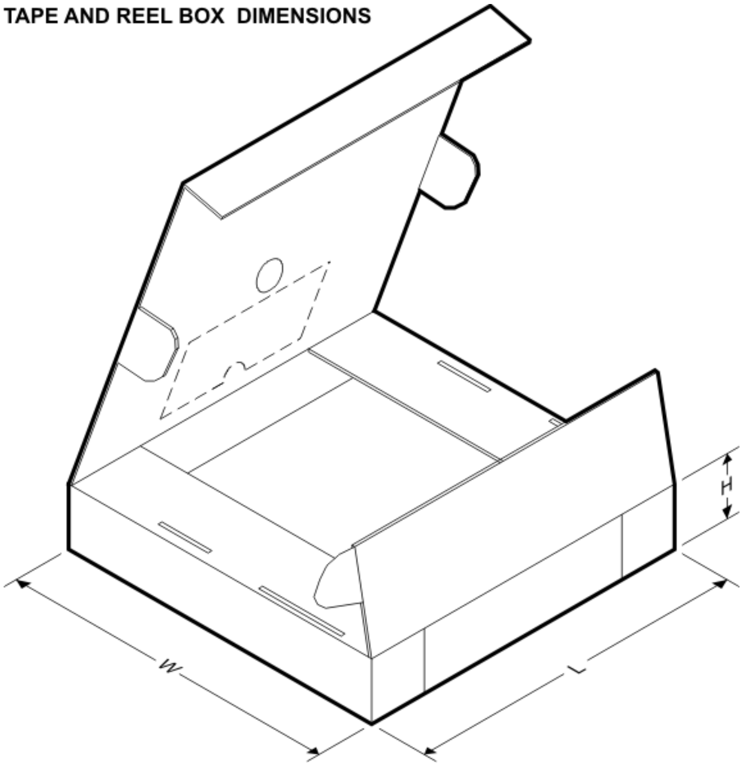
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC8T245DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC8T245DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVC8T245DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC8T245DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVC8T245NSR	SO	NS	24	2000	330.0	24.4	8.3	15.4	2.6	12.0	24.0	Q1
SN74LVC8T245RHLR	VQFN	RHL	24	1000	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

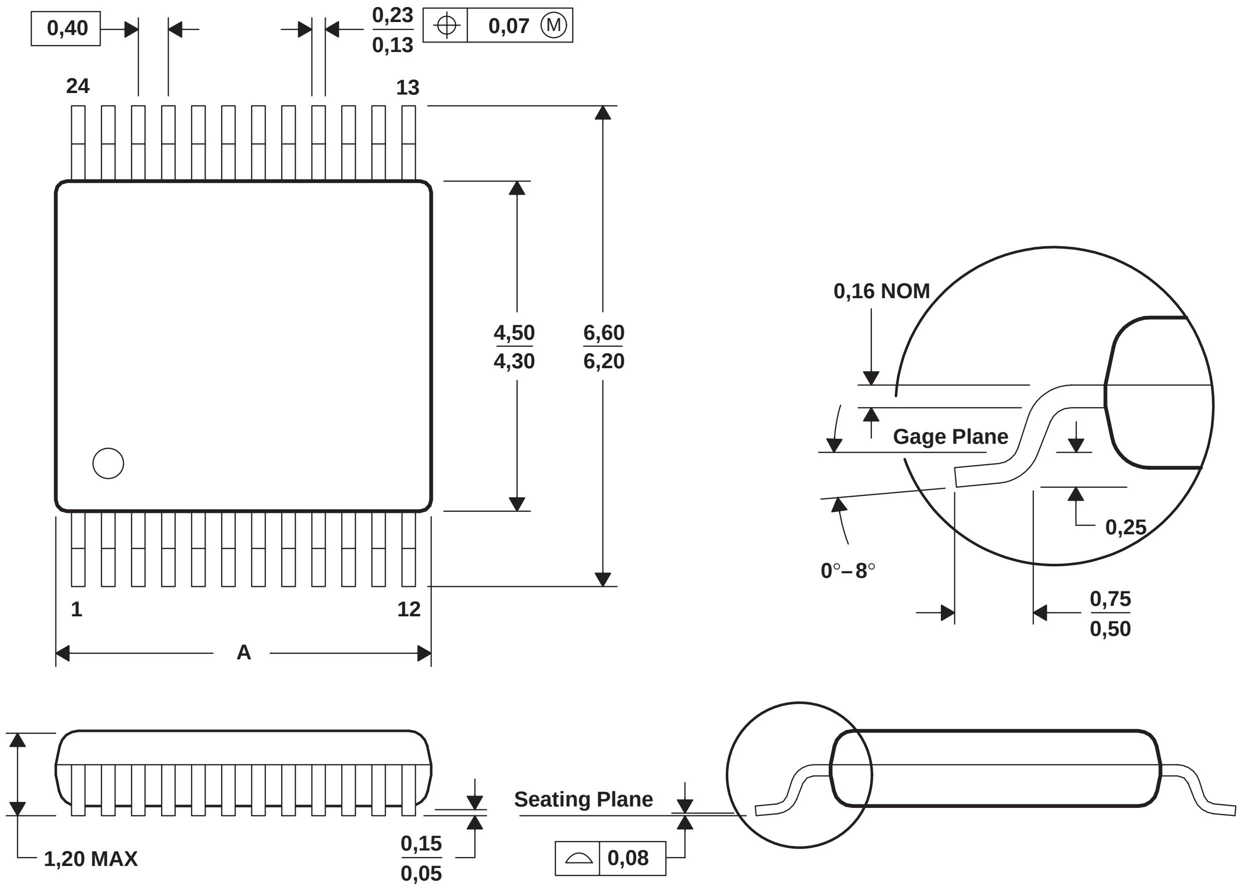


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC8T245DBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
SN74LVC8T245DBR	SSOP	DB	24	2000	367.0	367.0	38.0
SN74LVC8T245DGVR	TVSOP	DGV	24	2000	367.0	367.0	35.0
SN74LVC8T245DWR	SOIC	DW	24	2000	367.0	367.0	45.0
SN74LVC8T245NSR	SO	NS	24	2000	367.0	367.0	45.0
SN74LVC8T245RHLR	VQFN	RHL	24	1000	210.0	185.0	35.0

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

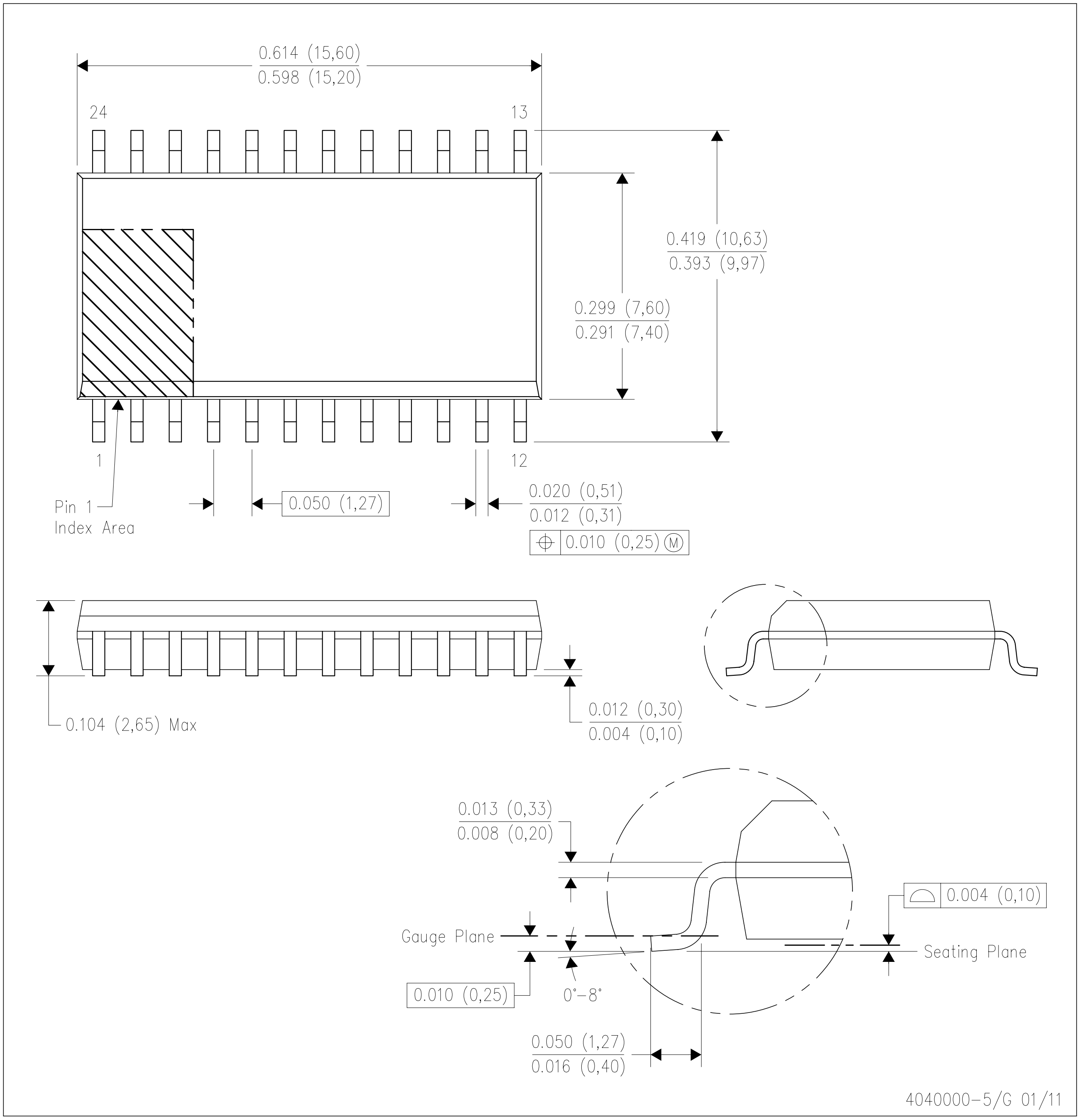


PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

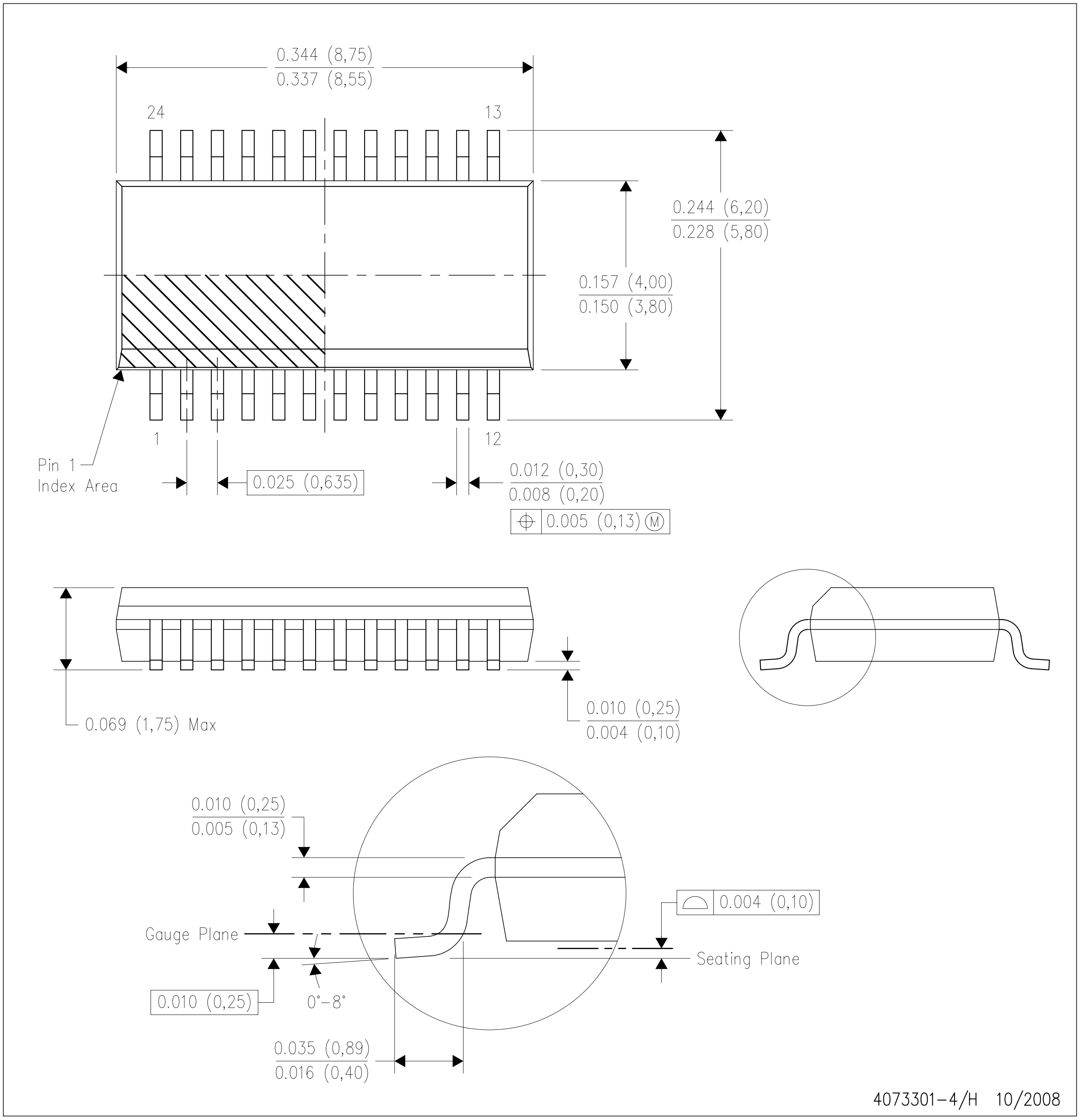
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DW (R-PDSO-G24) PLASTIC SMALL OUTLINE



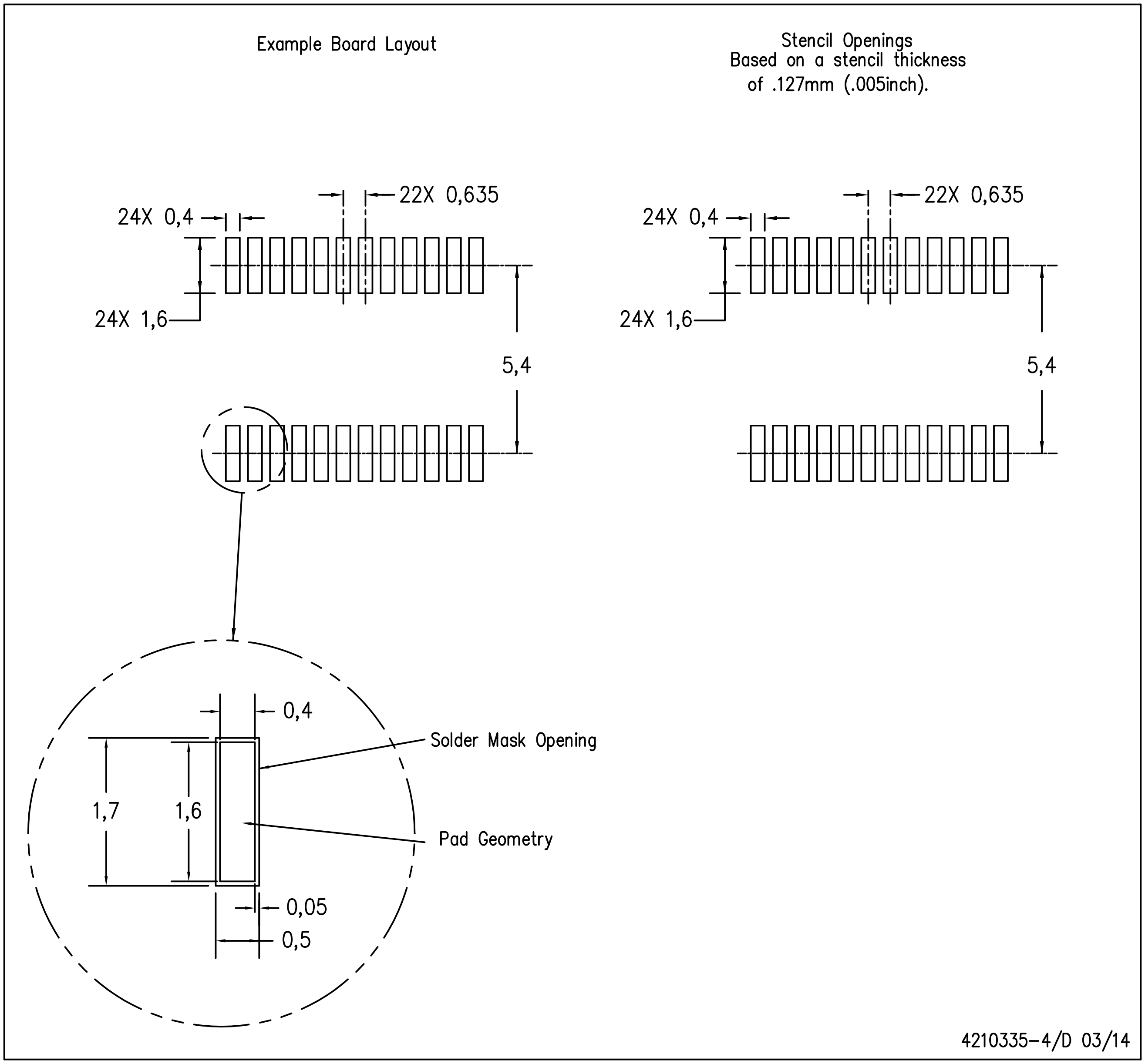
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AD.

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



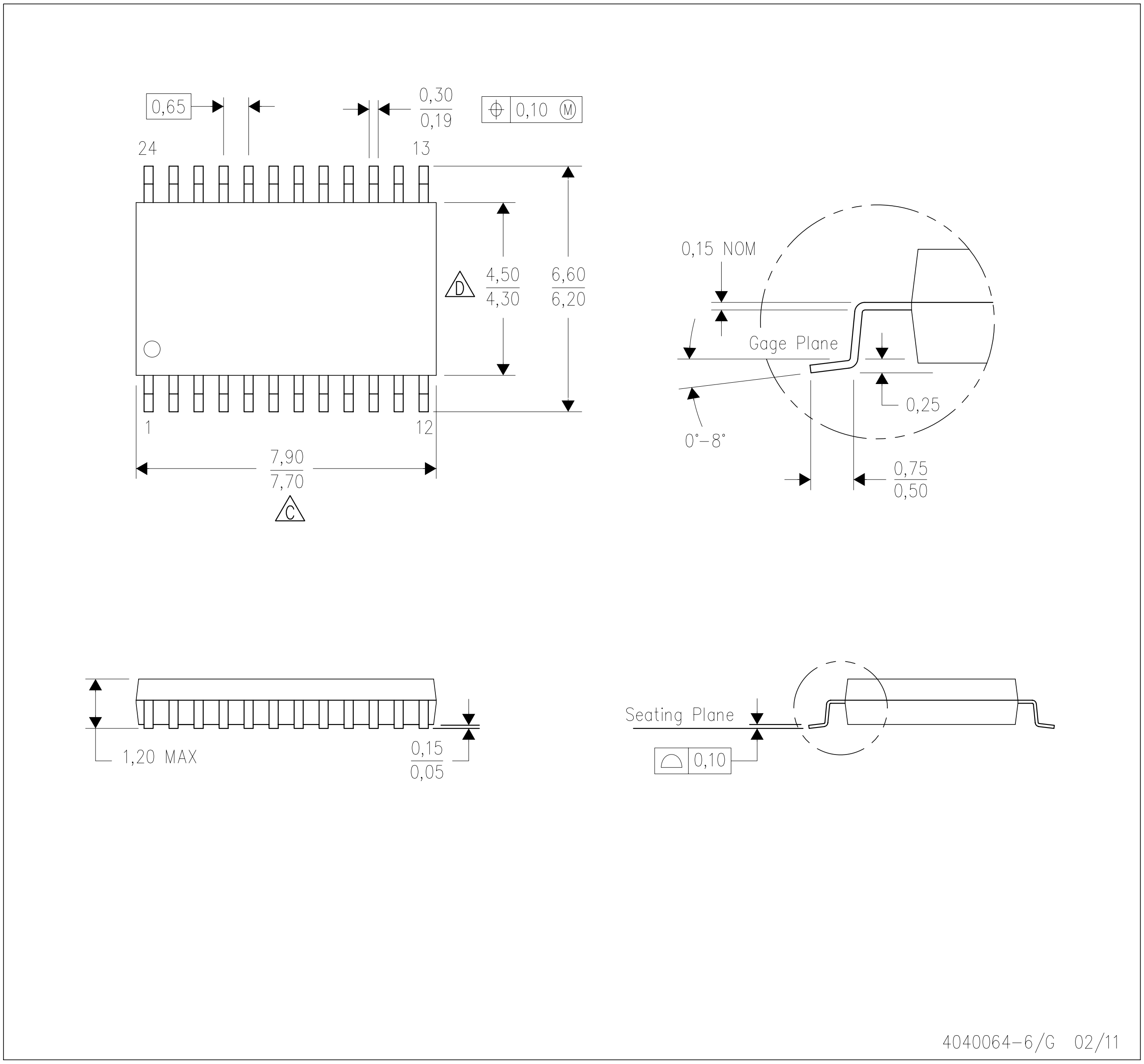
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

DBQ (R–PDSO–G24) PLASTIC SMALL OUTLINE PACKAGE



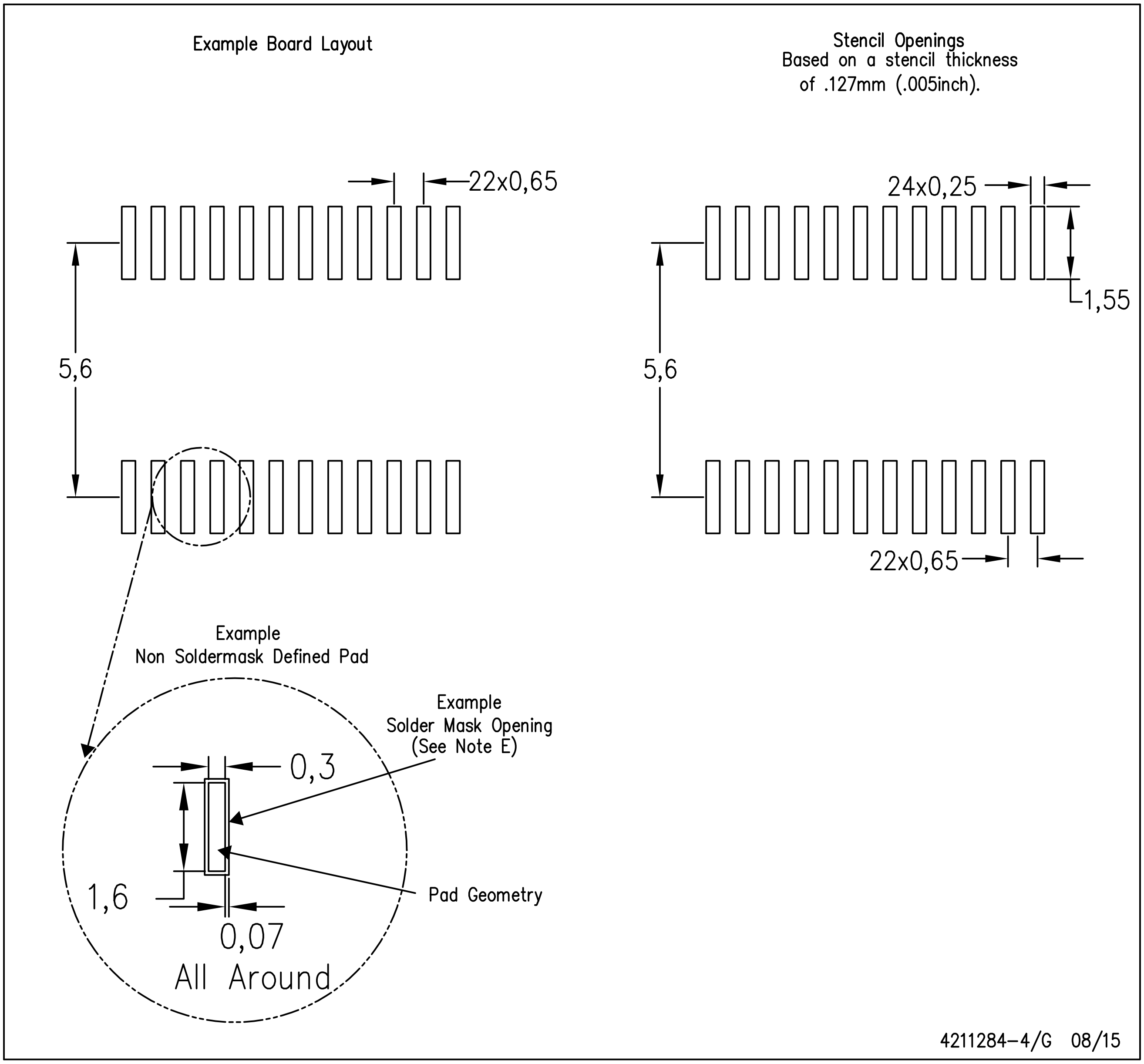
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PW (R-PDSO-G24) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

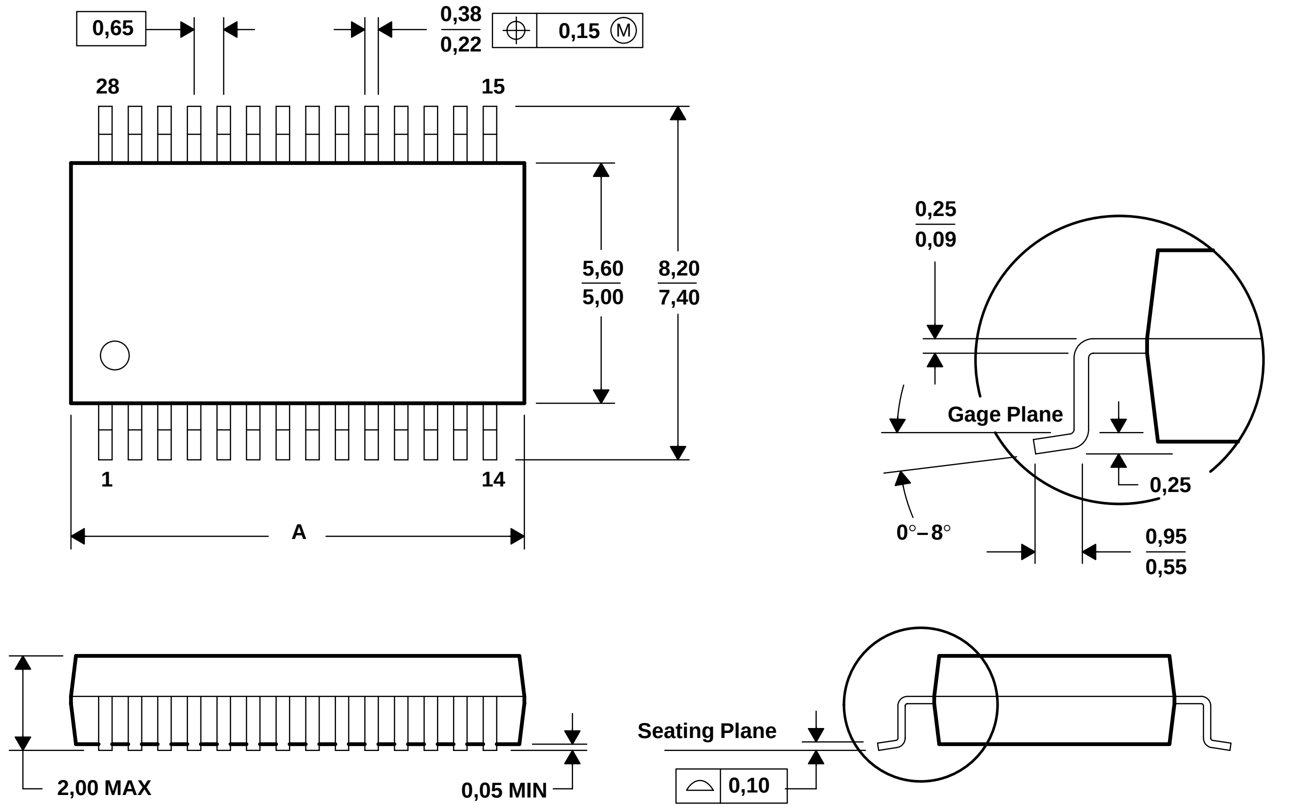
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

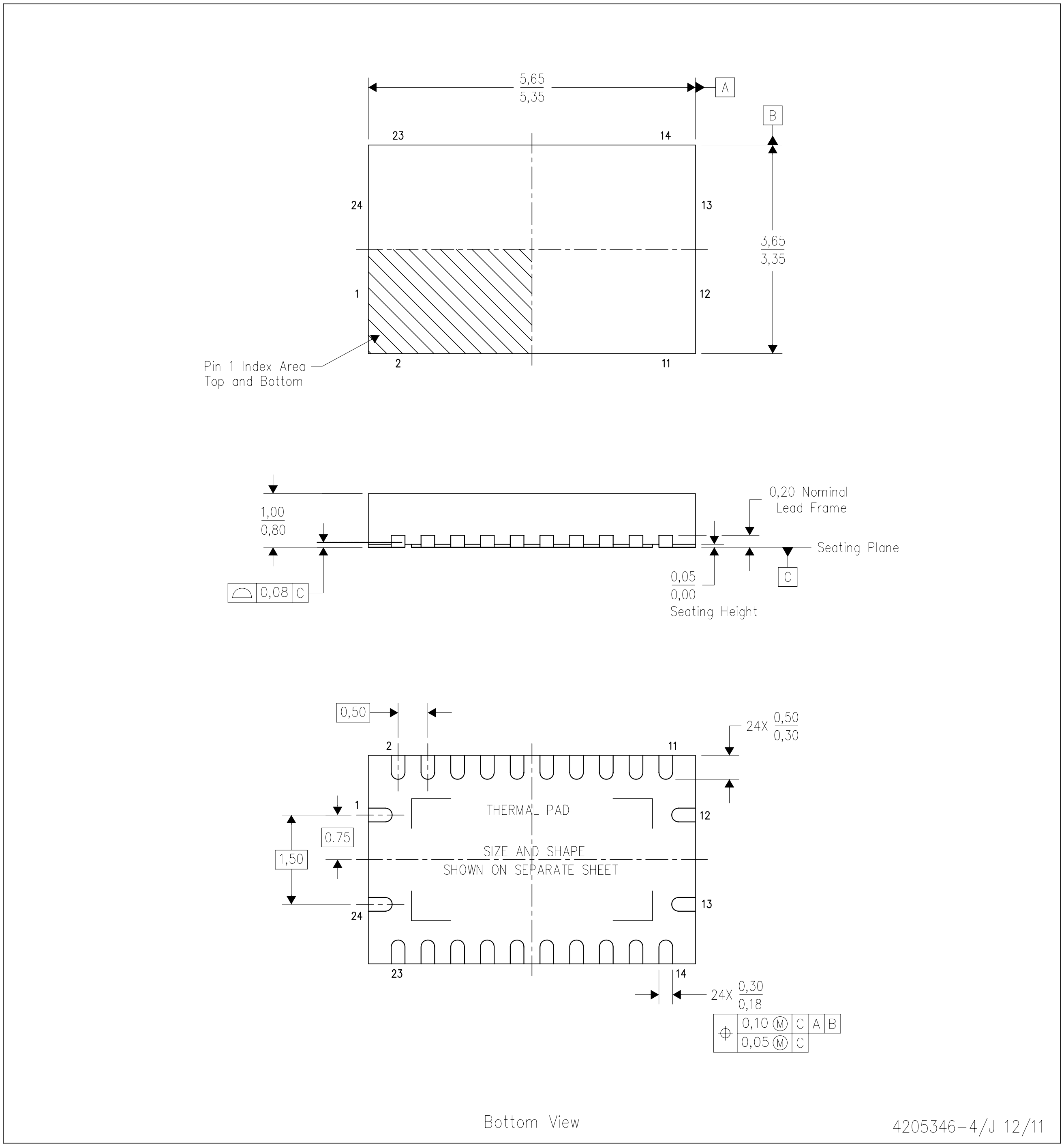


PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

RHL (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. JEDEC MO–241 package registration pending.

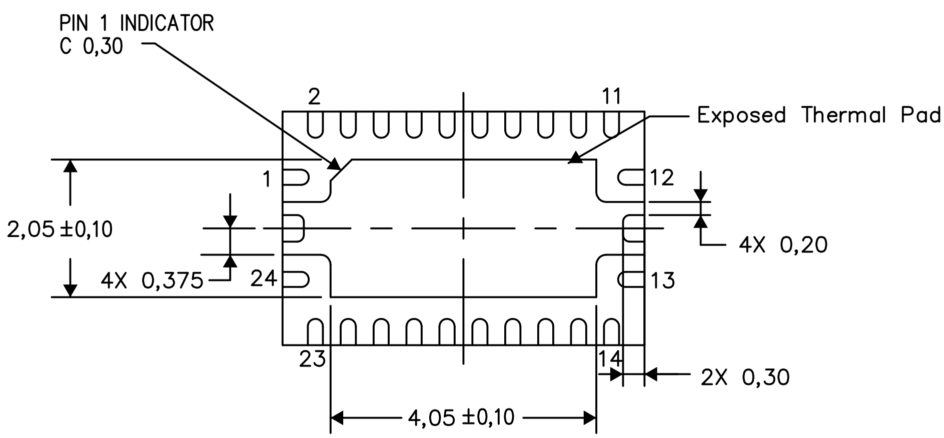
RHL (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



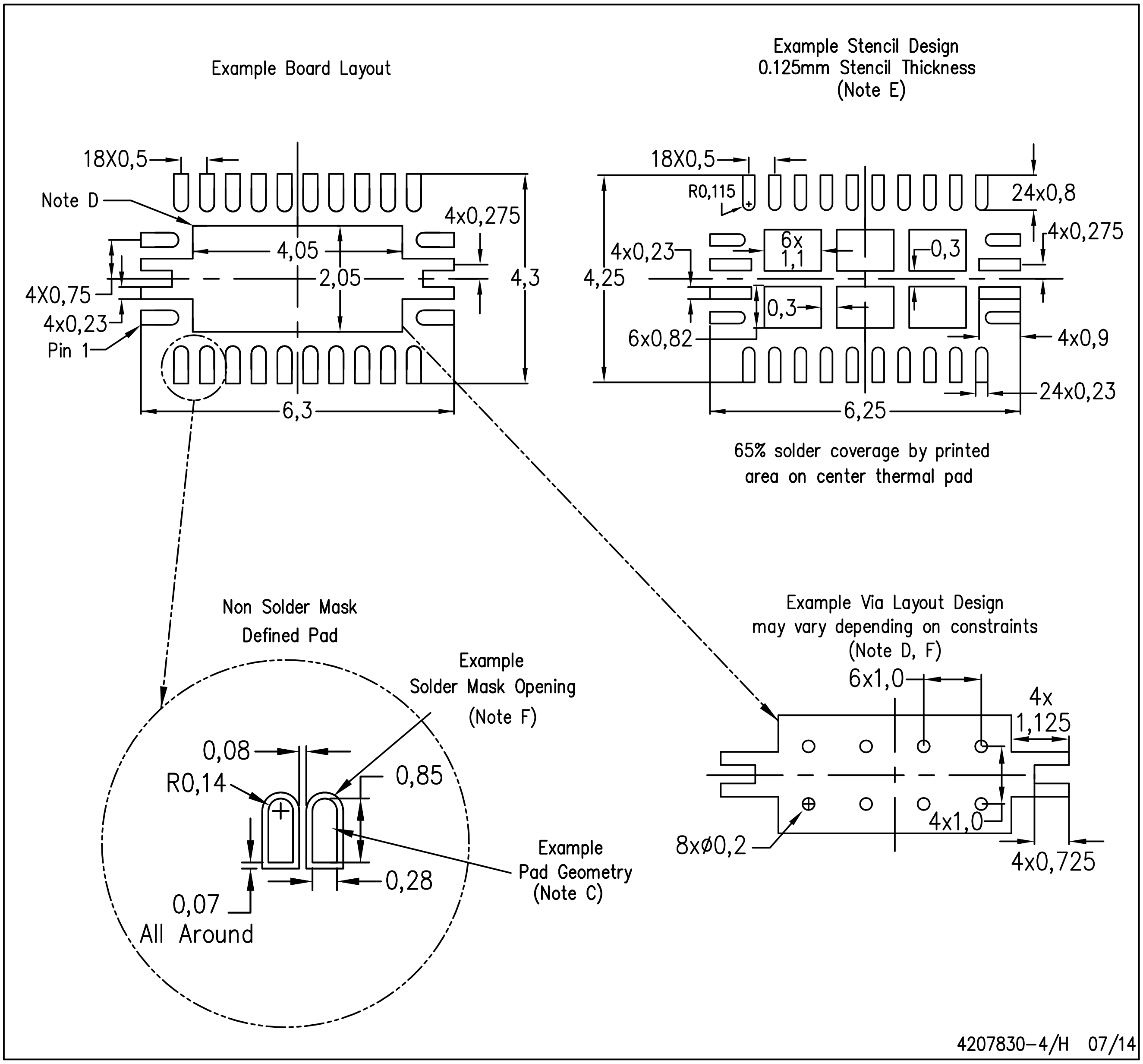
Bottom View

Exposed Thermal Pad Dimensions

4206363–4/N 07/14

NOTE: All linear dimensions are in millimeters

RHL (R-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD

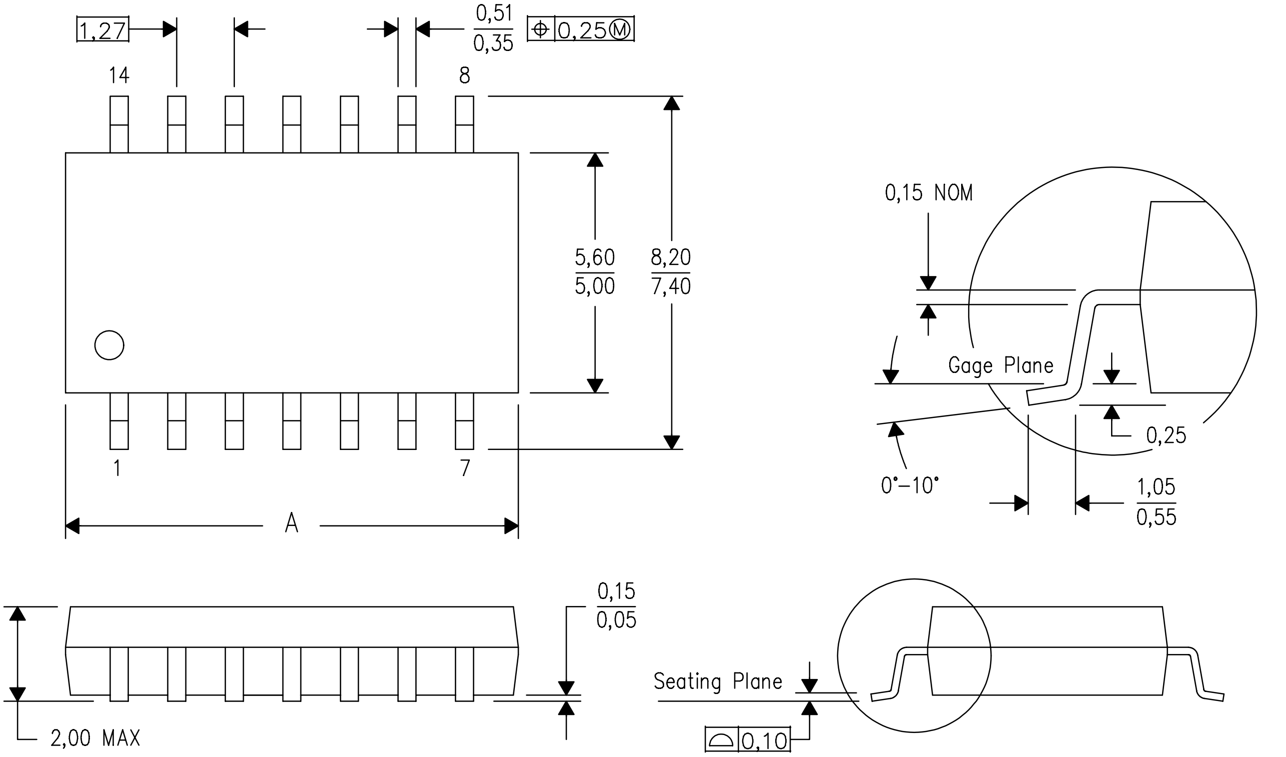


NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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