SN74LVCC3245A Octal Bus Transceiver With Adjustable Output Voltage and 3-State Outputs

1 Features

- Bidirectional Voltage Translator
- 2.3 V to 3.6 V on A Port and 3 V to 5.5 V on B Port
- Control Inputs V_{IH} and V_{IL} Levels Are Referenced to V_{CCA} Voltage
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Level translation
- USB
- Interfacing
- Analog and Digital Applications

3 Description

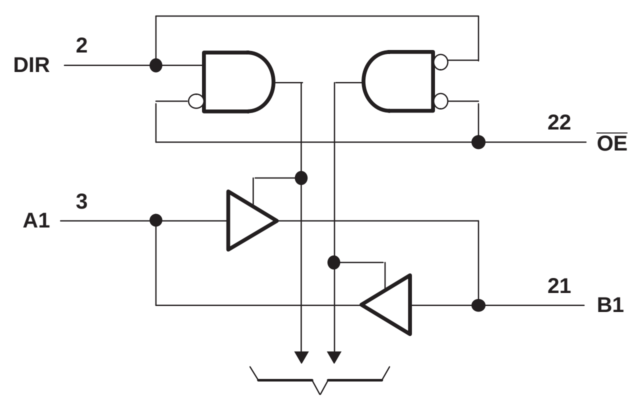
The SN74LVCC3245A device is 8-bit (octal) noninverting bus transceiver contains two separate supply rails. The B port is designed to track V_{CCB}, which accepts voltages from 3 V to 5.5 V, and the A port is designed to track V_{CCA}, which operates at 2.3 V to 3.6 V. This allows for translation from a 3.3-V to a 5-V system environment and vice versa, from a 2.5-V to a 3.3-V system environment and vice versa.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVCC3245ADBQ	SSOP (24)	8.65 mm × 3.90 mm
SN74LVCC3245ADW	SOIC (24)	15.40 mm × 7.50 mm
SN74LVCC3245ADB	SSOP (24)	8.20 mm × 5.30 mm
SN74LVCC3245ANS	SO (24)	15.00 mm × 5.30 mm
SN74LVCC3245APW	TSSOP (24)	7.80 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

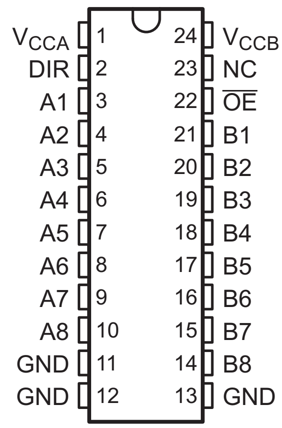
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (March 2005) to Revision P — **Page**

- Added *Applications* section, *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Removed *Ordering Information* table. ... 1

5 Pin Configuration and Functions

DB, DBQ, DW, NS, or PW Package
24-Pin SSOP, SOIC, SO, or TSSOP
Top View



NC – No internal connection

See *Mechanical, Packaging, and Orderable Information* for dimensions.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A1	3	I/O	A1 port
A2	4	I/O	A2 port
A3	5	I/O	A3 port
A4	6	I/O	A4 port
A5	7	I/O	A5 port
A6	8	I/O	A6 port
A7	9	I/O	A7 port
A8	10	I/O	A8 port
B1	21	I/O	B1 port
B2	20	I/O	B2 port
B3	19	I/O	B3 port
B4	18	I/O	B4 port
B5	17	I/O	B5 port
B6	16	I/O	B6 port
B7	15	I/O	B7 port
B8	14	I/O	B8 port
DIR	2	I	Dir input
GND	11	--	Ground
	12		
	13		
NC	23	--	Unconnected
$\overline{OE}$	22	I	Output Enable active low
V_{CCA}	1	--	A port power
V_{CCB}	24	--	B port power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage		–0.5	6	V
V_I	Input voltage	All A ports(2)	–0.5	V_{CCA} + 0.5	V
		All B ports(3)	–0.5	V_{CCB} + 0.5	
		Except I/O ports(2)	–0.5	V_{CCA} + 0.5	
V_O	Output voltage(3)	All A ports	–0.5	V_{CCA} + 0.5	V
		All B ports	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This value is limited to 4.6 V maximum.
(3) This value is limited to 6 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1)

		V_{CCA}	V_{CCB}	MIN	NOM	MAX	UNIT
V_{CCA}	Supply voltage			2.3	3.3	3.6	V
V_{CCB}	Supply voltage			3	5	5.5	V
V_{IHA}	High-level input voltage	2.3 V	3 V	1.7			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	2			
V_{IHB}	High-level input voltage	2.3 V	3 V	2			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	3.85			
V_{ILA}	Low-level input voltage	2.3 V	3 V			0.7	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Recommended Operating Conditions(1) (continued)

		V_{CCA}	V_{CCB}	MIN	NOM	MAX	UNIT
V_{ILB}	Low-level input voltage	2.3 V	3 V			0.8	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			1.65	
V_{IH}	High-level input voltage (control terminals) (referenced to V_{CCA})	2.3 V	3 V	1.7			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	2			
V_{IL}	Low-level input voltage (control terminals) (referenced to V_{CCA})	2.3 V	3 V			0.7	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	
V_{IA}	Input voltage			0		V_{CCA}	V
V_{IB}	Input voltage			0		V_{CCB}	V
V_{OA}	Output voltage			0		V_{CCA}	V
V_{OB}	Output voltage			0		V_{CCB}	V
I_{OHA}	High-level output current	2.3 V	3 V			–8	mA
		2.7 V	3 V			–12	
		3 V	3 V			–24	
		2.7 V	4.5 V			–24	
I_{OHB}	High-level output current	2.3 V	3 V			–12	mA
		2.7 V	3 V			–12	
		3 V	3 V			–24	
		2.7 V	4.5 V			–24	
I_{OLA}	Low-level output current	2.3 V	3 V			8	mA
		2.7 V	3 V			12	
		3 V	3 V			24	
		2.7 V	4.5 V			24	
I_{OLB}	Low-level output current	2.3 V	3 V			12	mA
		2.7 V	3 V			12	
		3 V	3 V			24	
		2.7 V	4.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate					10	ns/V
T_A	Operating free-air temperature			–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)(2)		SN74LVCC3245A					UNIT
		DB (SSOP)	DBQ (SSOP)	DW (SOIC)	NS (SO)	PW (TSSOP)	
		24 PINS	24 PINS	24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63	61	46	65	88	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OHA}		I_{OH} = –100 µA	3 V	3 V	2.9	3		V
		I_{OH} = –8 mA	2.3 V	3 V	2			
		I_{OH} = –12 mA	2.7 V	3 V	2.2	2.5		
			3 V	3 V	2.4	2.8		
		I_{OH} = –24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	2	2.3		
V_{OHB}		I_{OH} = –100 µA	3 V	3 V	2.9	3		V
		I_{OH} = –12 mA	2.3 V	3 V	2.4			
			2.7 V	3 V	2.4	2.8		
		I_{OH} = –24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	3.2	4.2		
V_{OLA}		I_{OL} = 100 µA	3 V	3 V			0.1	V
		I_{OL} = 8 mA	2.3 V	3 V			0.6	
		I_{OL} = 12 mA	2.7 V	3 V		0.1	0.5	
		I_{OL} = 24 mA	3 V	3 V		0.2	0.5	
			2.7 V	4.5 V		0.2	0.5	
V_{OLB}		I_{OL} = 100 µA	3 V	3 V			0.1	V
		I_{OL} = 12 mA	2.3 V	3 V			0.4	
		I_{OL} = 24 mA	3 V	3 V		0.2	0.5	
			2.7 V	4.5 V		0.2	0.5	
I_I	Control inputs	$V_I = V_{CCA}$ or GND	3.6 V	3.6 V		±0.1	±1	µA
				5.5 V		±0.1	±1	
I_{OZ} (1)	A or B ports	$V_O = V_{CCA/B}$ or GND, $V_I = V_{IL}$ or V_{IH}	3.6 V	3.6 V		±0.5	±5	µA
I_{CCA}	B to A	A port = V_{CCA} or GND, $I_O = 0$	3.6 V	Open		5	50	µA
		B port = V_{CCB} or GND, $I_O = 0$	3.6 V	3.6 V		5	50	
				5.5 V		5	50	
I_{CCB}	A to B	A port = V_{CCA} or GND, $I_O = 0$	3.6 V	3.6 V		5	50	µA
				5.5 V		8	80	
ΔI_{CCA} (2)	A port	$V_I = V_{CCA}$ – 0.6 V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at GND and DIR at V_{CCA}	3.6 V	3.6 V		0.35	0.5	mA
	$\overline{OE}$	$V_I = V_{CCA}$ – 0.6 V, Other inputs at V_{CCA} or GND, DIR at V_{CCA}	3.6 V	3.6 V		0.35	0.5	
	DIR	$V_I = V_{CCA}$ – 0.6 V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at GND	3.6 V	3.6 V		0.35	0.5	
ΔI_{CCB} (2)	B port	$V_I = V_{CCB}$ – 2.1 V, Other inputs at V_{CCB} or GND, $\overline{OE}$ at GND and DIR at GND	3.6 V	5.5 V		1	1.5	mA
C_i	Control inputs	$V_I = V_{CCA}$ or GND	Open	Open		4		pF
C_{io}	A or B ports	$V_O = V_{CCA/B}$ or GND	3.3 V	5 V		18.5		pF

(1) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(2) This is the increase in supply current for each input that is at one of the specified voltage levels, rather than 0 V or the associated V_{CC}.

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2 through Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA}, V_{CCB}	MIN	MAX	UNIT
t_{PHL}	A	B	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	9.4	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	6	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	7.1	
t_{PLH}	A	B	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	9.1	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	5.3	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	7.2	
t_{PHL}	B	A	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	11.2	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	5.8	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	6.4	
t_{PLH}	B	A	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	9.9	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	7	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	7.6	
t_{PZL}	$\overline{OE}$	A	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	14.5	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	9.2	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	9.7	
t_{PZH}	$\overline{OE}$	A	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	12.9	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	9.5	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	9.5	
t_{PZL}	$\overline{OE}$	B	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	13	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	8.1	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	9.2	
t_{PZH}	$\overline{OE}$	B	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	12.8	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	8.4	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	9.9	
t_{PLZ}	$\overline{OE}$	A	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	7.1	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	7	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	6.6	

Switching Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2 through Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA}, V_{CCB}	MIN	MAX	UNIT
t_{PHZ}	$\overline{OE}$	A	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	6.9	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	7.8	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	6.9	
t_{PLZ}	$\overline{OE}$	B	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	8.8	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	7.3	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	7.5	
t_{PHZ}	$\overline{OE}$	B	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V	1	8.9	ns
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V	1	7	
			V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V	1	7.9	

6.7 Operating Characteristics

V_{CCA} = 3.3 V, V_{CCB} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50, f = 10 MHz	38	pF
		Outputs disabled		4.5	

6.8 Typical Characteristics

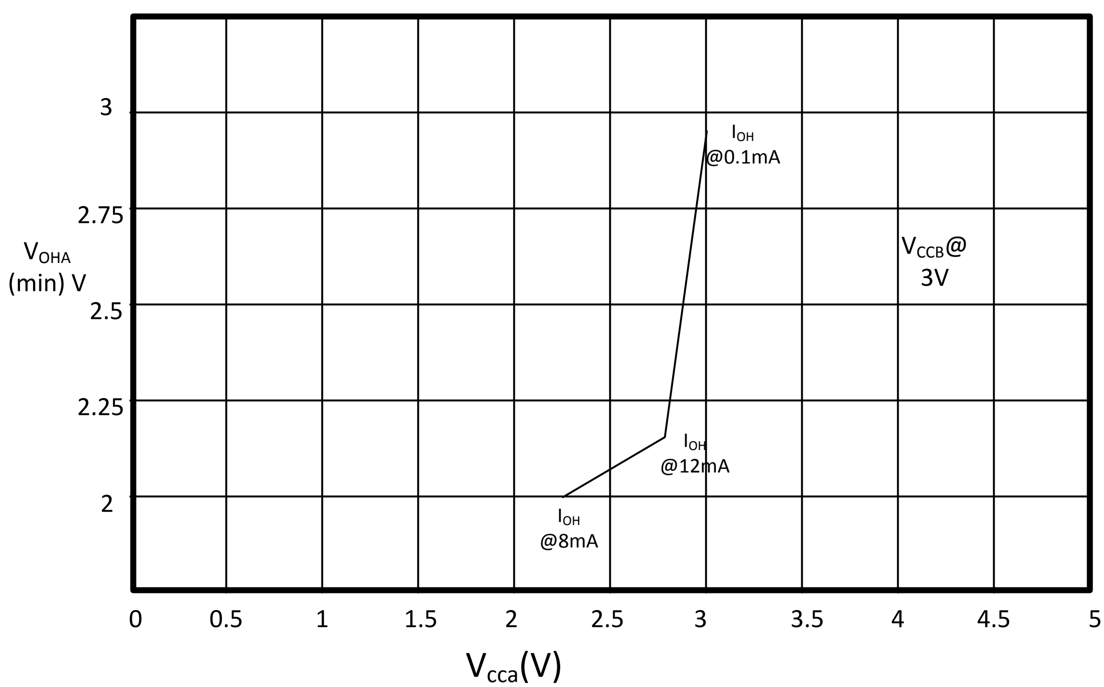
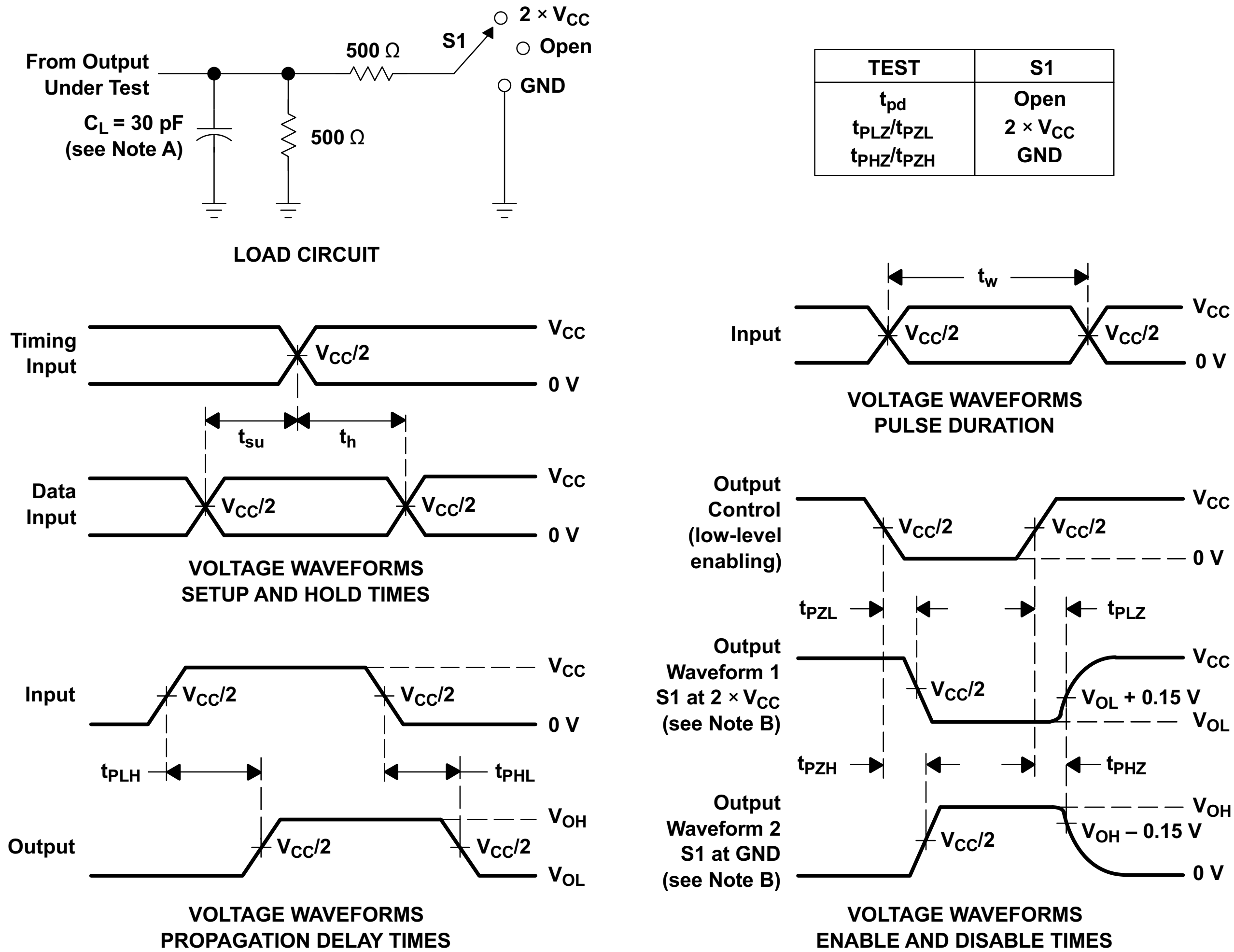


Figure 1. $V_{OHA(min)}$ VS V_{CCA}

7 Parameter Measurement Information

7.1 A Port (V_{CCA} = 2.5 V ± 0.2 V and V_{CCB} = 3.3 V ± 0.3 V)



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

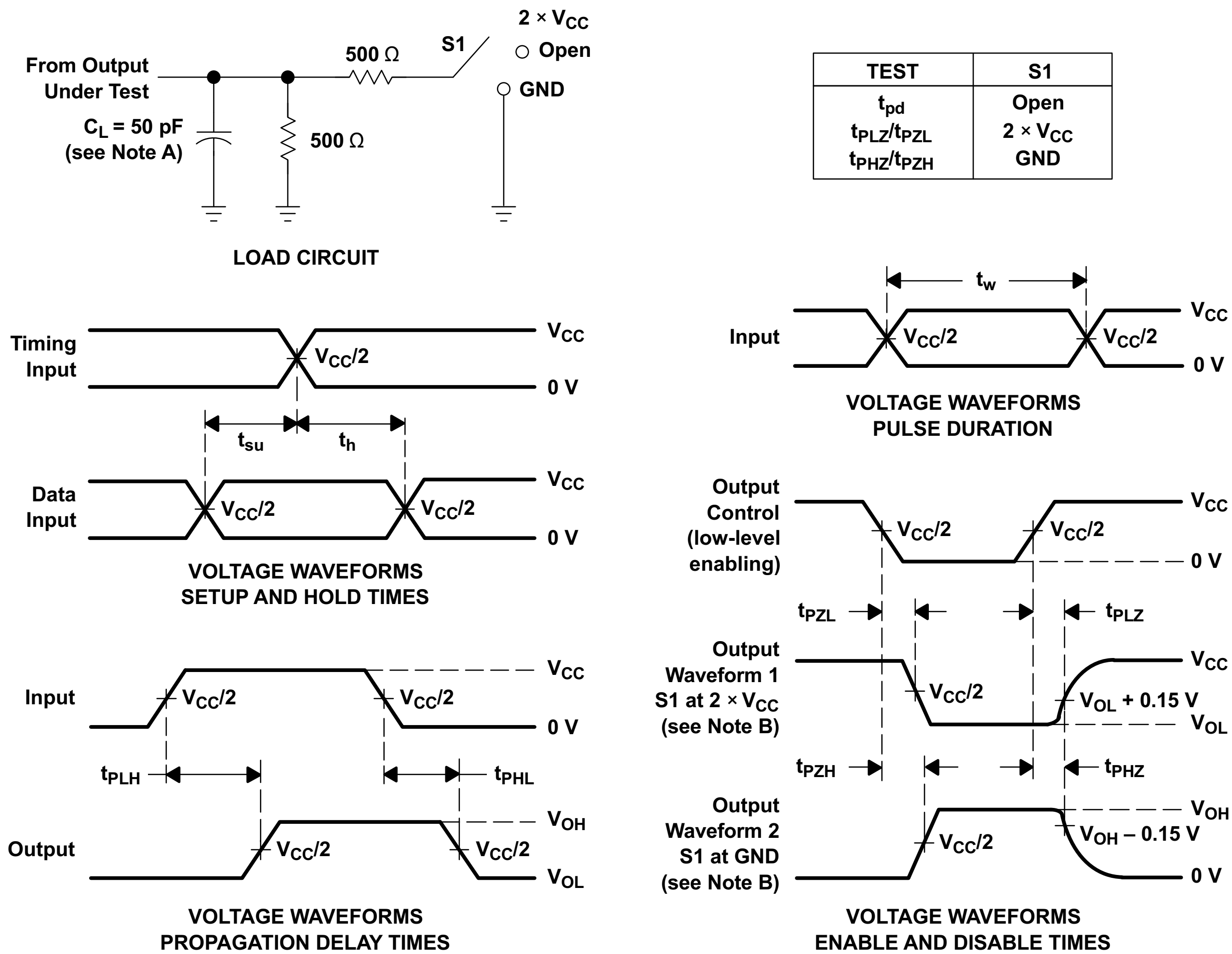
F. t_{PZL} and $t_{PZH}$are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

7.2 B Port (V_{CCA} = 2.5 V ± 0.2 V and V_{CCB} = 3.3 V ± 0.3 V)



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

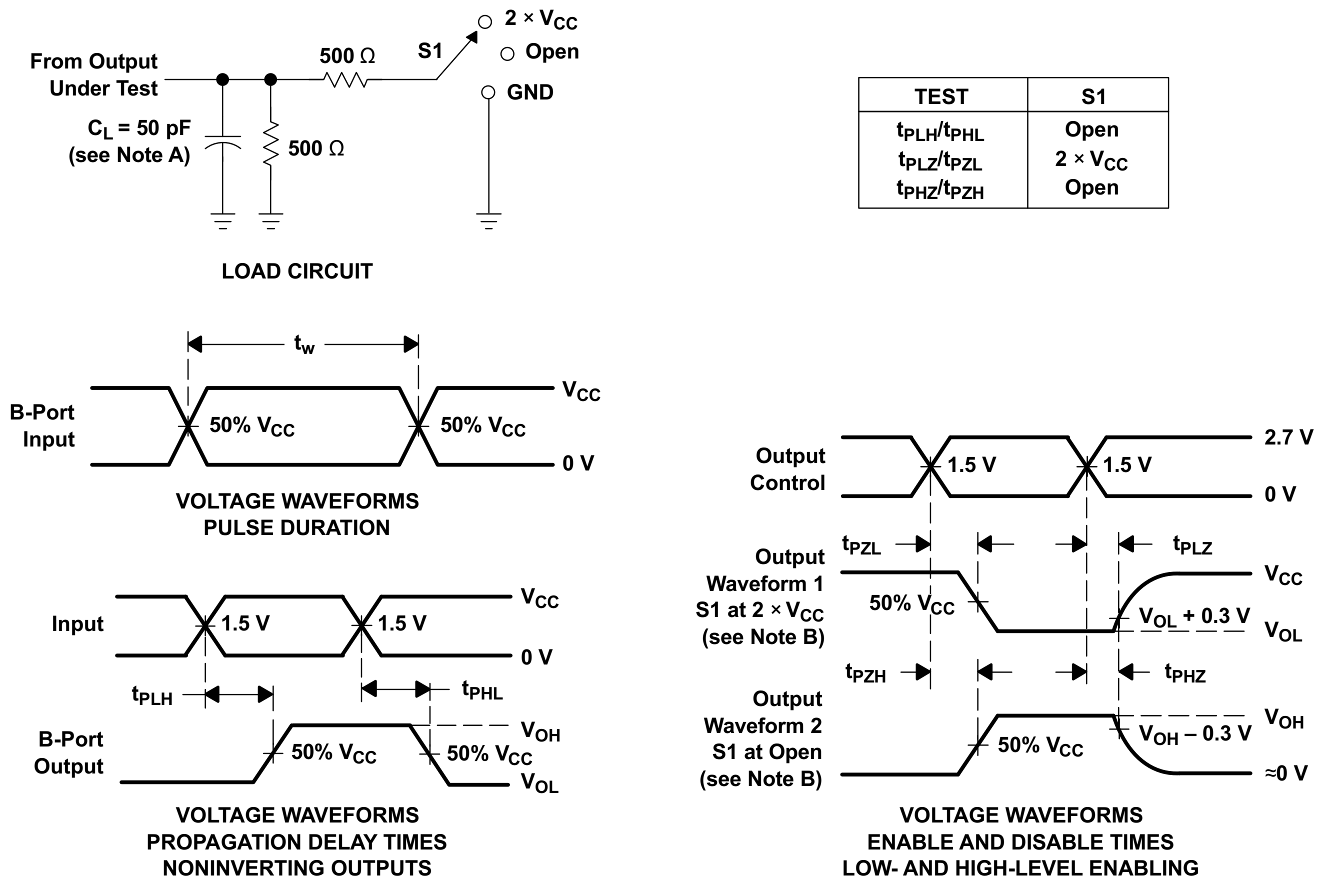
F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

7.3 B Port (V_{CCA} = 3.6 V and V_{CCB} = 5.5 V)



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	Open

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

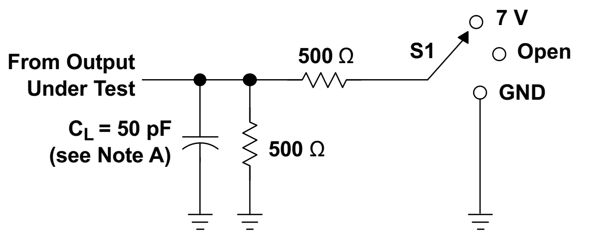
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

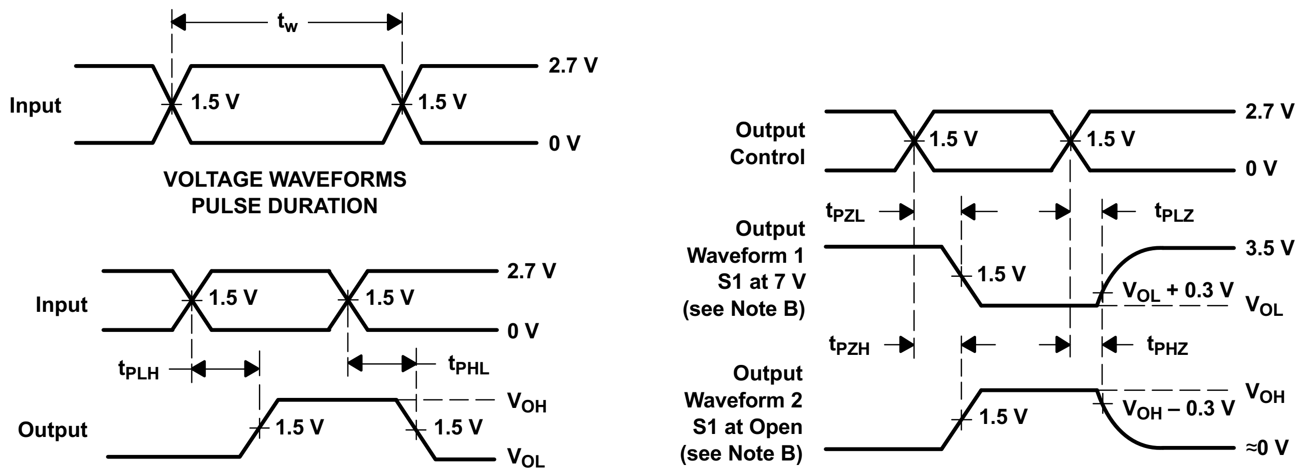
Figure 4. Load Circuit and Voltage Waveforms

7.4 A and B Port (V_{CCA} and V_{CCB} = 3.6 V)



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

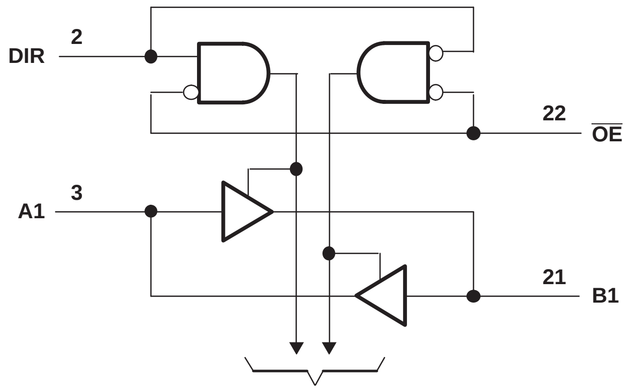
Figure 5. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVCC3245A device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, $\overline{OE}$) is powered by V_{CCA} .

8.2 Functional Block Diagram



8.3 Feature Description

This device is a bidirectional level translator designed to operate from 2.3 V to 3.6 V on Port A and 3 V to 5.5 V on B port. The control inputs recommended operating specifications are referenced with respect to V_{CCA} Voltage.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVCC3245A.

Table 1. Function Table (Each Transceiver)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVCC3245A device is a bidirectional level translator designed to operate from 2.3 V to 3.6 V on Port A and 3 V to 5.5 V on B port and designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input.

9.2 Typical Application

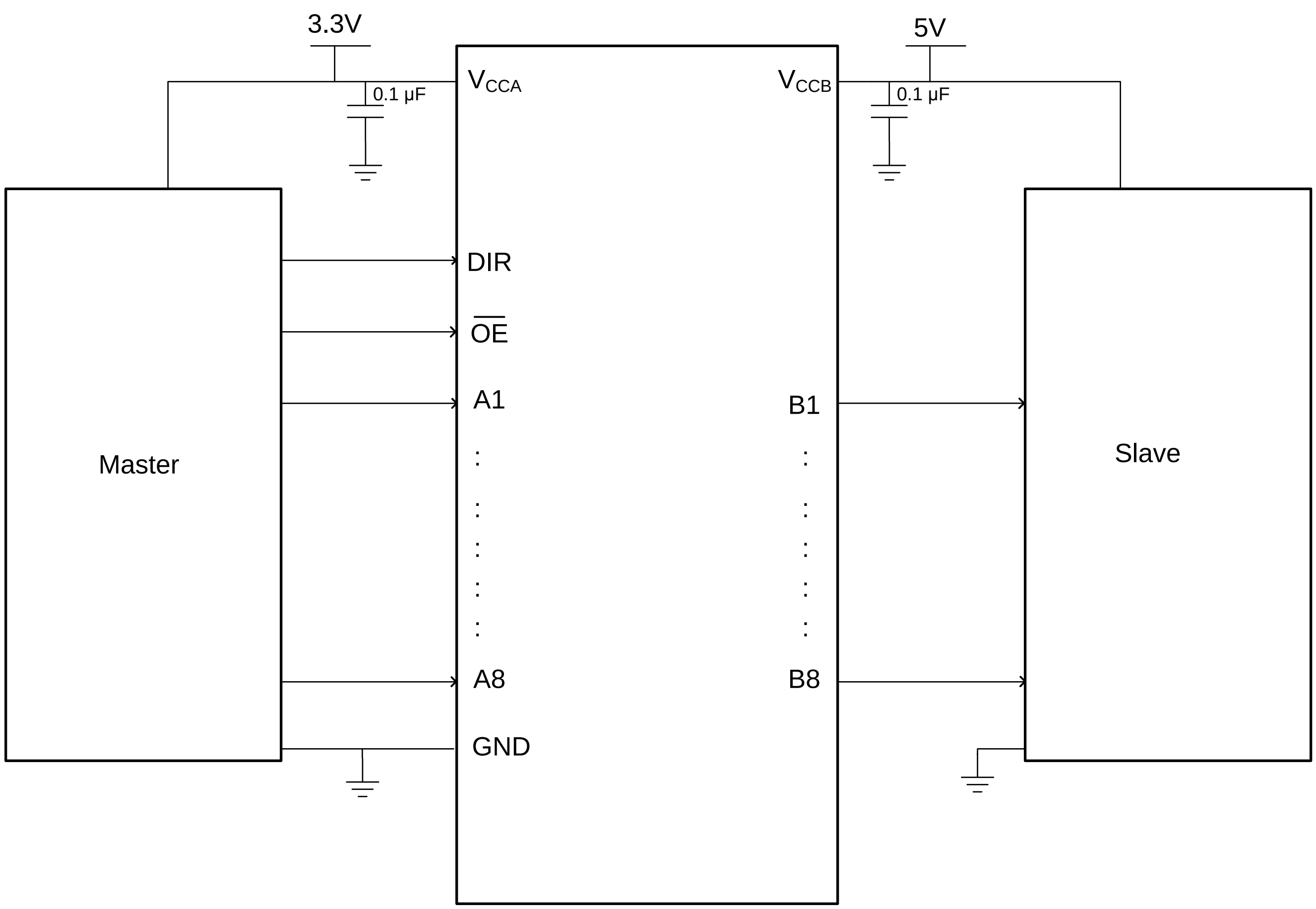


Figure 6. Typical Application

9.2.1 Design Requirements

This device can be used as bidirectional level translator depending on the DIR pin. The application describes the level translation of Master with signals at 3.3 V to slave operating at 5 V. The $\overline{OE}$ pin is low and DIR pin is 3.3-V high.

Typical Application (continued)

9.2.2 Detailed Design Procedure

Use the procedure that follows for the design:

1. Recommended Input Conditions
   - Rise time and fall time specs. See (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Absolute Maximum Output Conditions
   - Load currents should not exceed (I_O max) per output and should not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the *Absolute Maximum Ratings* table.
   - All the voltages on A and B ports should not exceed above V_{CCA} or V_{CCB} to prevent the biasing of Electrostatic discharge (ESD) diodes.

9.2.3 Application Curve

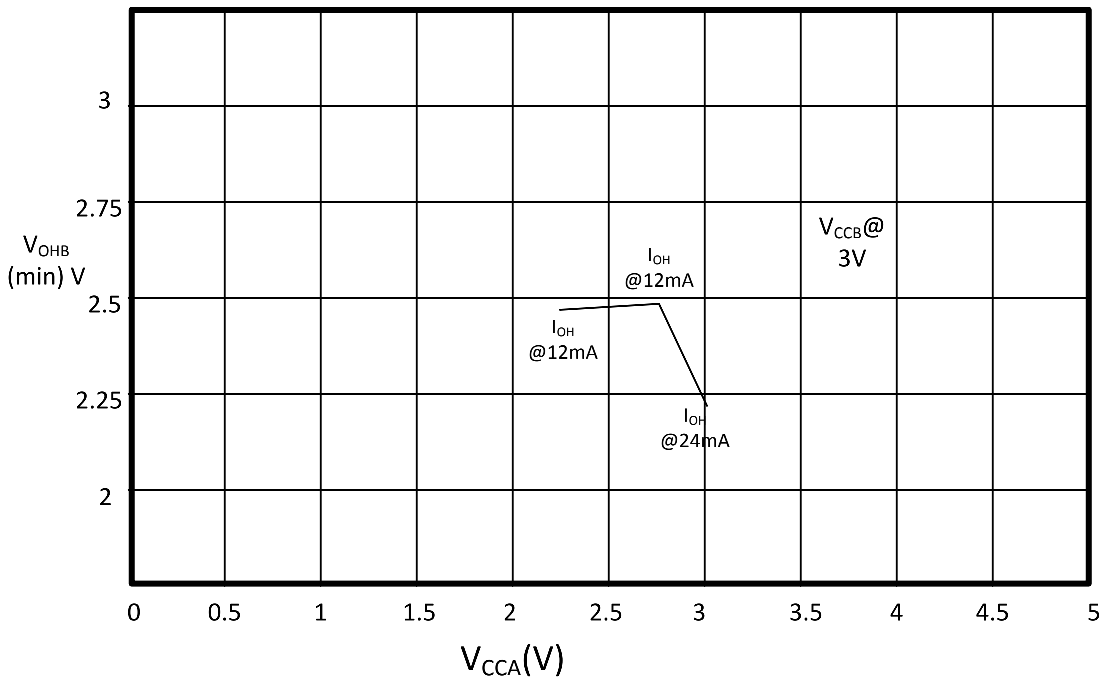


Figure 7. $V_{OHB(min)}$ vs V_{CCA}

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended and if there are multiple V_{CC} pins then 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

11.2 Layout Example

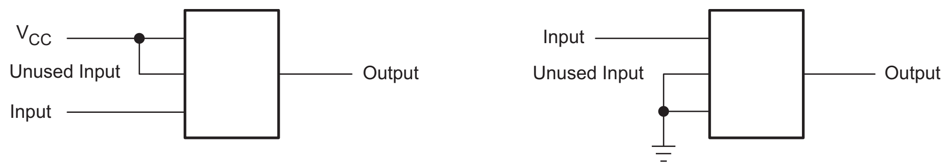


Figure 8. Layout Example

11.3 Power-Up Considerations

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device terminals. To guard against such power-up problems, take these precautions:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie $\overline{OE}$ to V_{CCA} with a pullup resistor so that it ramps with V_{CCA}.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA}. Otherwise, keep DIR low.

Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, SCEA021.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Implications of Slow or Floating CMOS Inputs*, SCBA004
- *Texas Instruments Voltage-Level-Translation Devices*, SCEA021

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
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12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCC3245ADBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245ADBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245ADBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ANSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ANSRE4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ANSRG4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245APW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCC3245APWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWT	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWTG4	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVCC3245A :

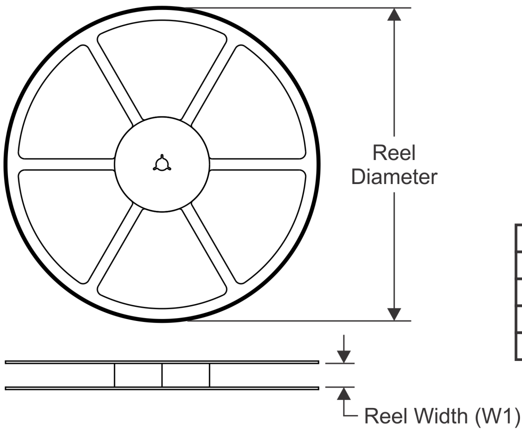
- Enhanced Product: SN74LVCC3245A-EP

NOTE: Qualified Version Definitions:

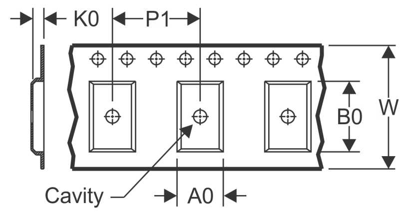
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

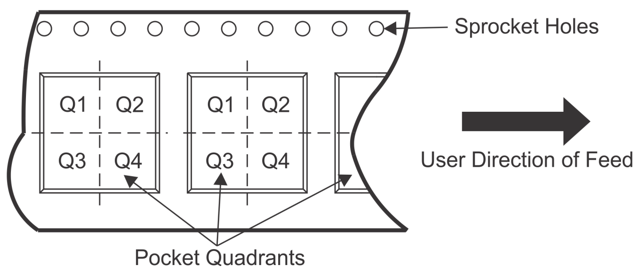


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

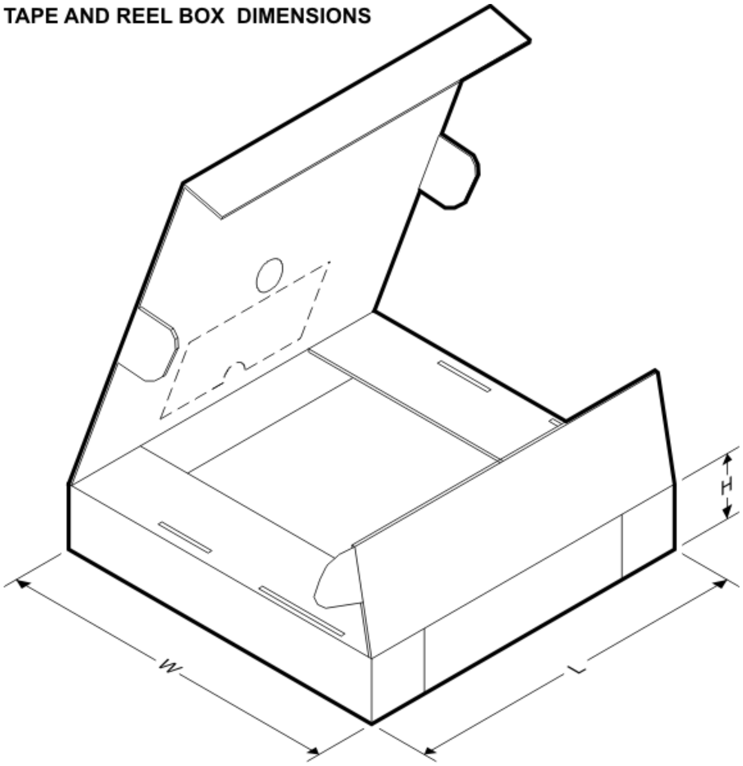
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCC3245ADBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVCC3245ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVCC3245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ADWRG4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ANSR	SO	NS	24	2000	330.0	24.4	8.3	15.4	2.6	12.0	24.0	Q1
SN74LVCC3245APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVCC3245APWT	TSSOP	PW	24	250	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

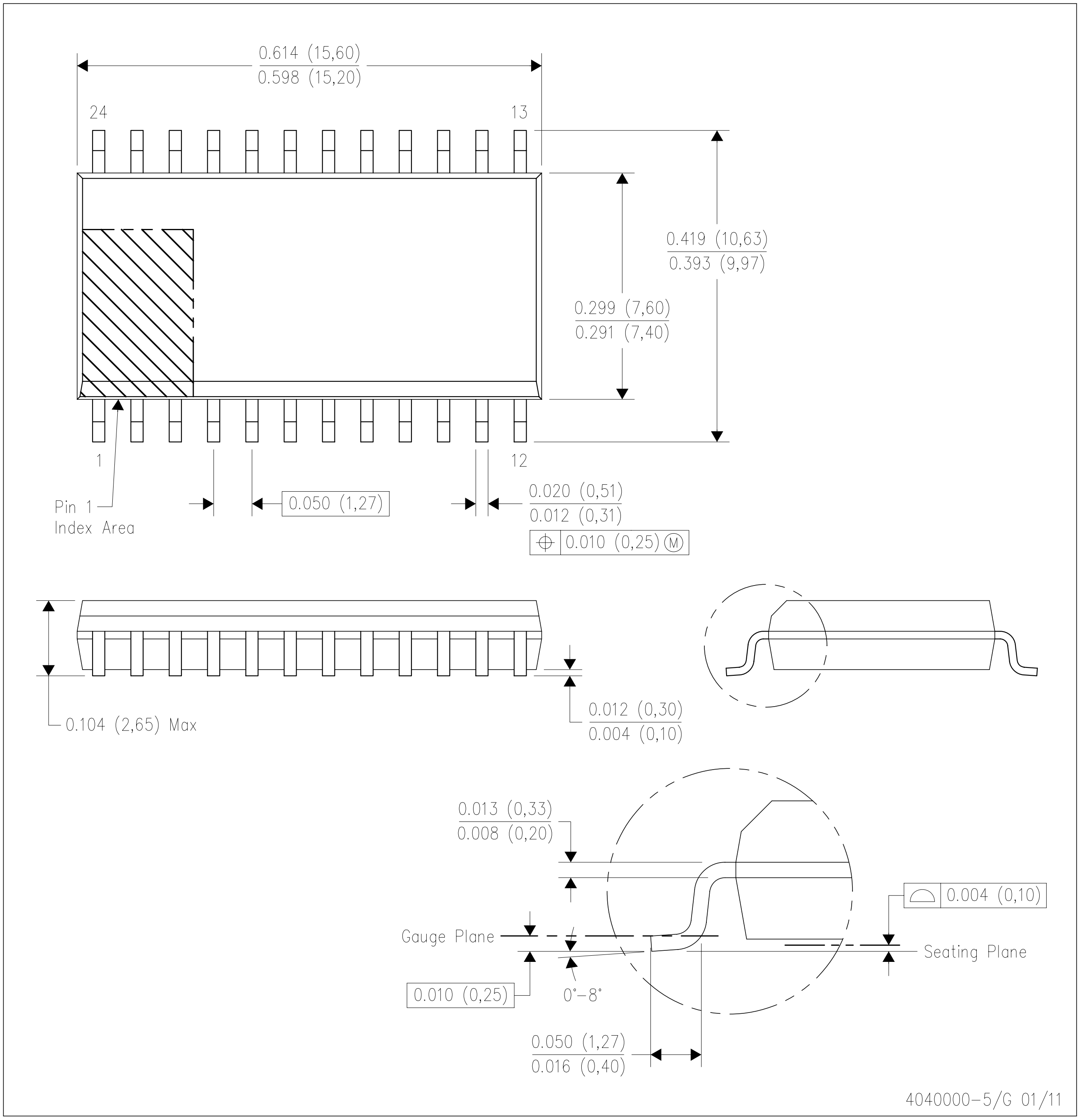
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

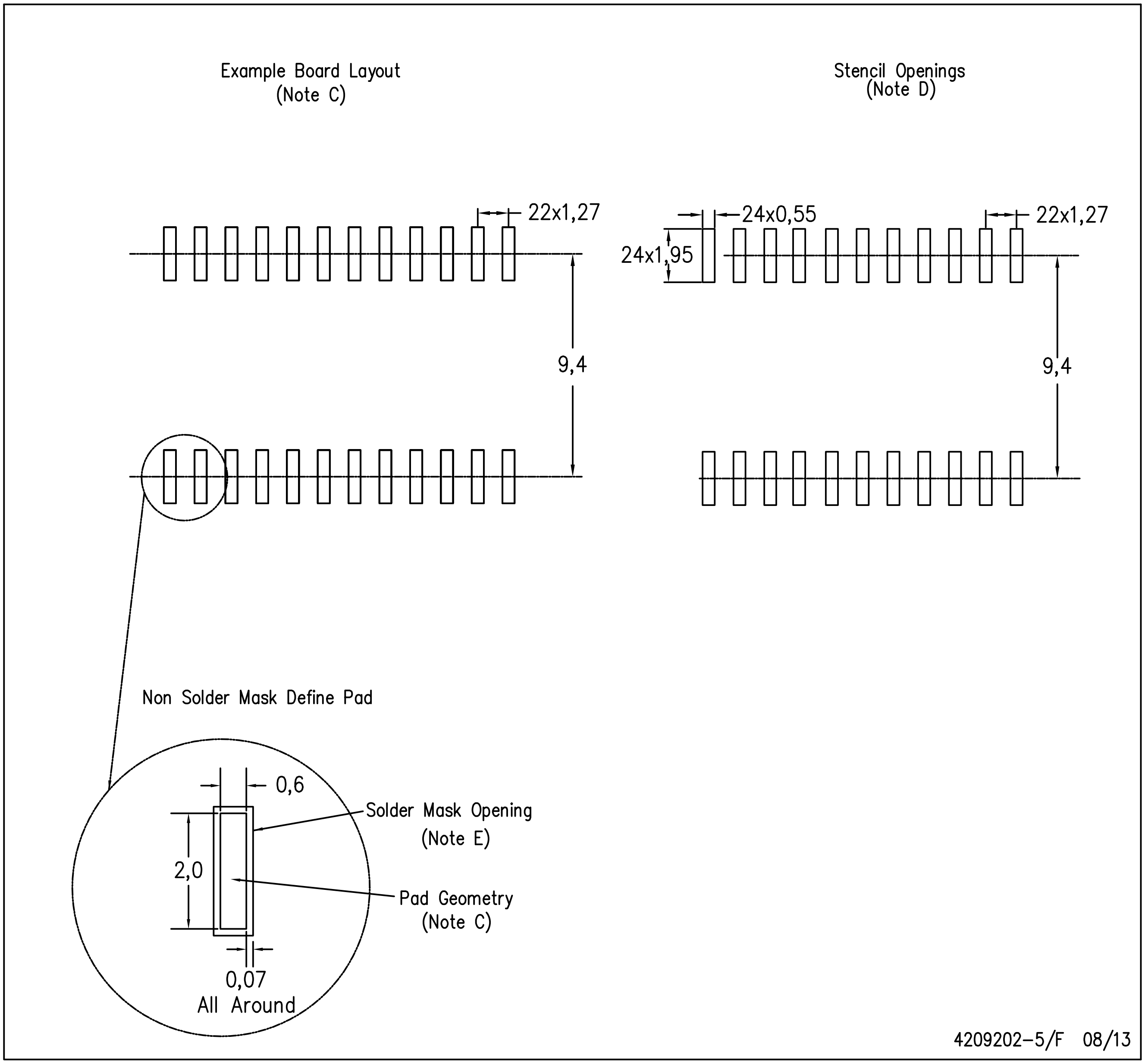
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCC3245ADBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
SN74LVCC3245ADBR	SSOP	DB	24	2000	367.0	367.0	38.0
SN74LVCC3245ADWR	SOIC	DW	24	2000	366.0	364.0	50.0
SN74LVCC3245ADWR	SOIC	DW	24	2000	367.0	367.0	45.0
SN74LVCC3245ADWRG4	SOIC	DW	24	2000	367.0	367.0	45.0
SN74LVCC3245ANSR	SO	NS	24	2000	367.0	367.0	45.0
SN74LVCC3245APWR	TSSOP	PW	24	2000	367.0	367.0	38.0
SN74LVCC3245APWT	TSSOP	PW	24	250	367.0	367.0	38.0

DW (R-PDSO-G24) PLASTIC SMALL OUTLINE



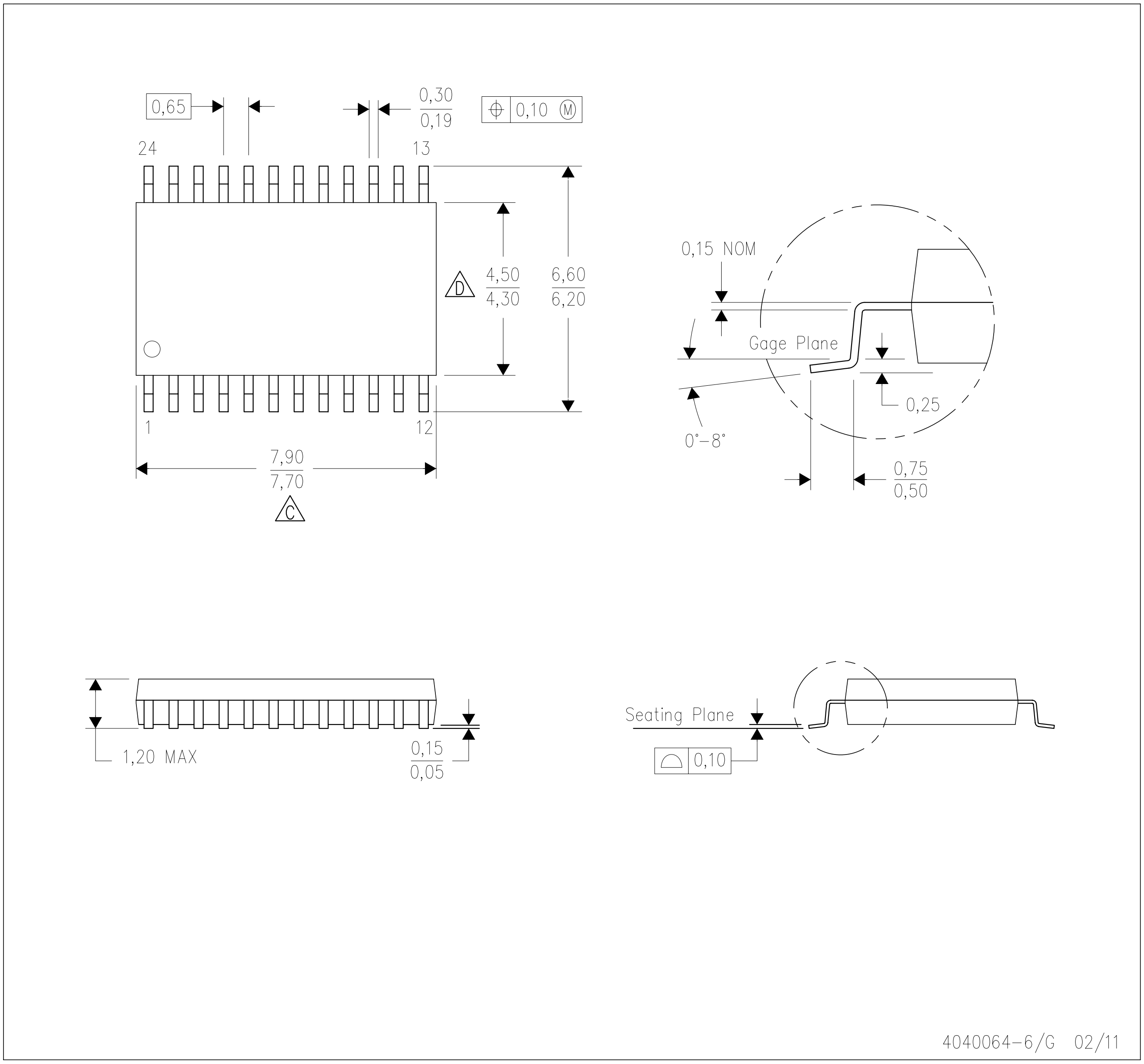
NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



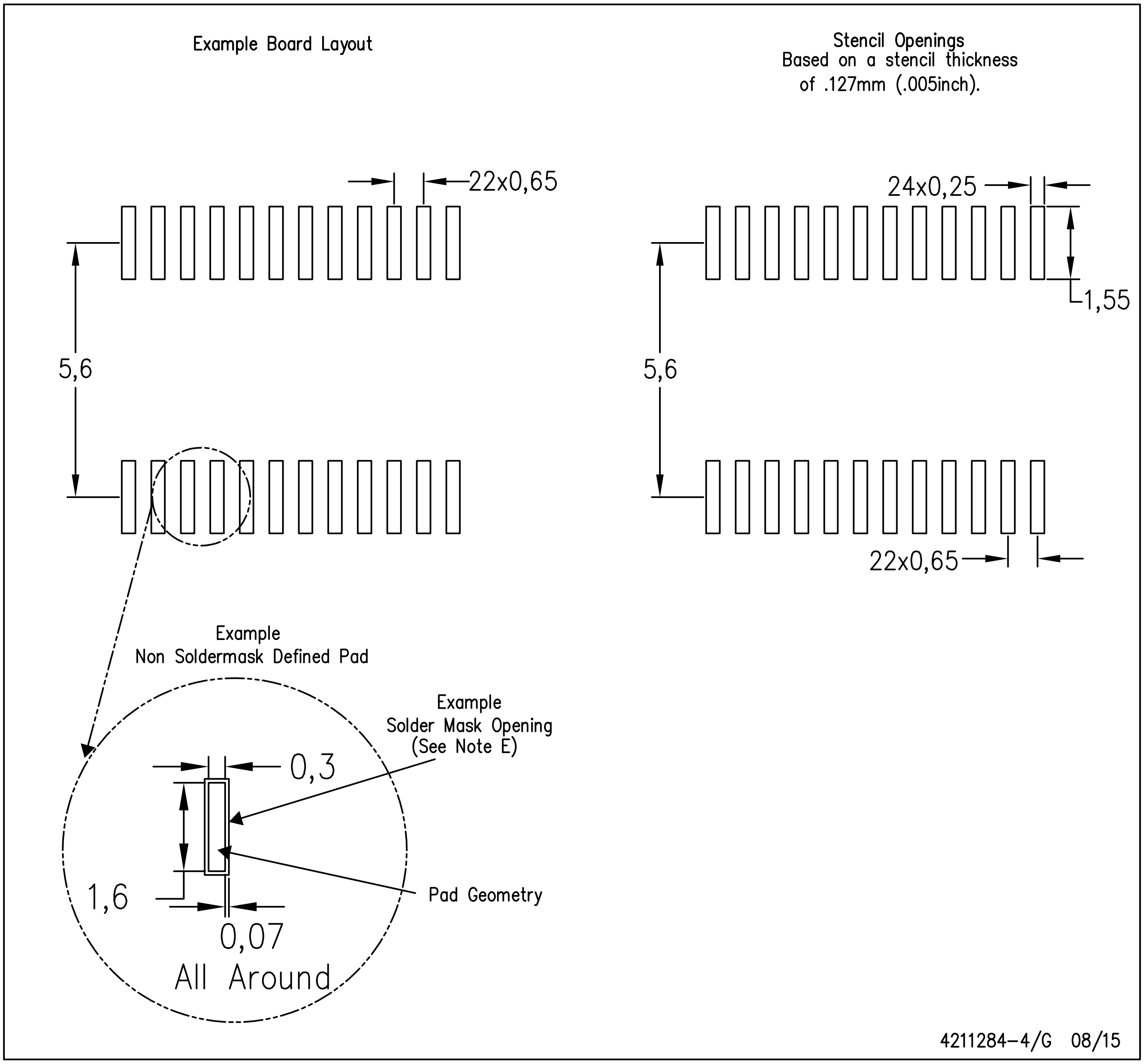
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R-PDSO-G24) PLASTIC SMALL OUTLINE

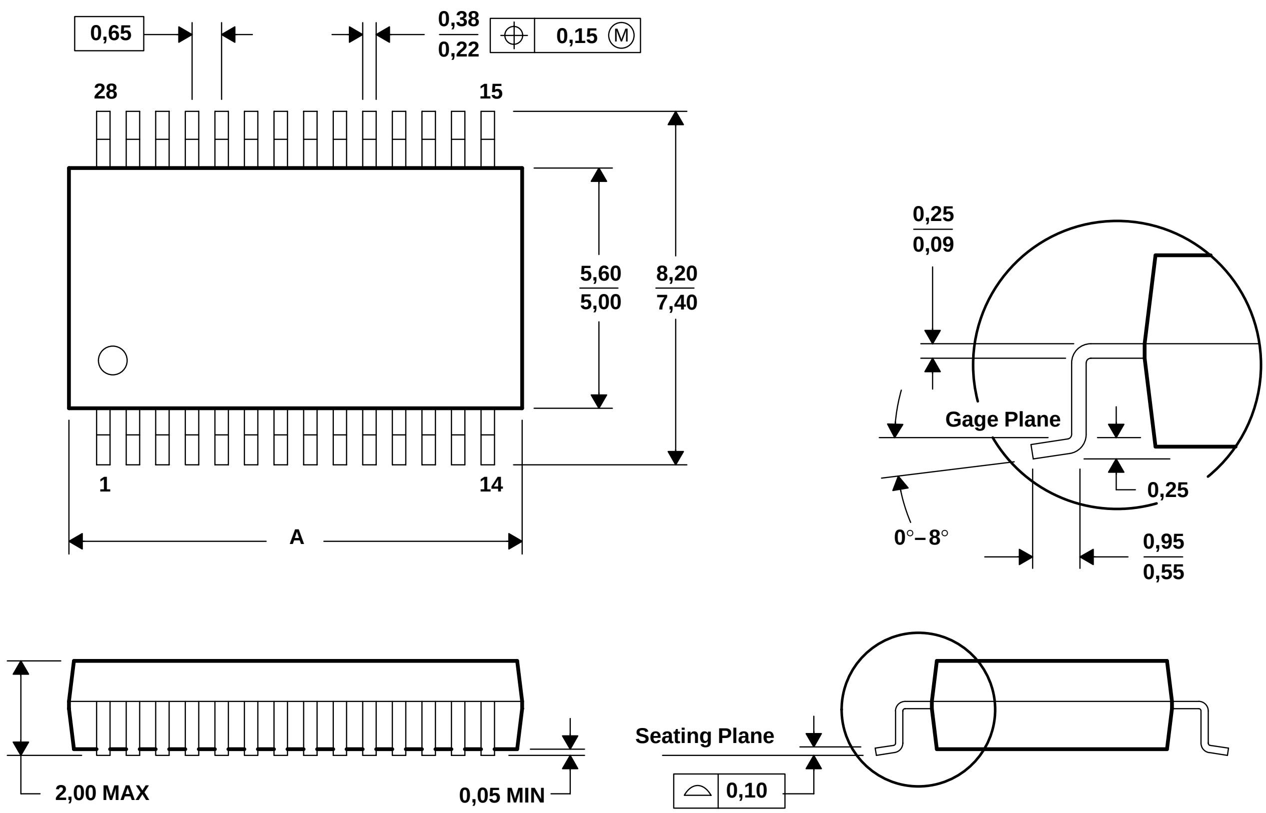


4211284-4/G 08/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

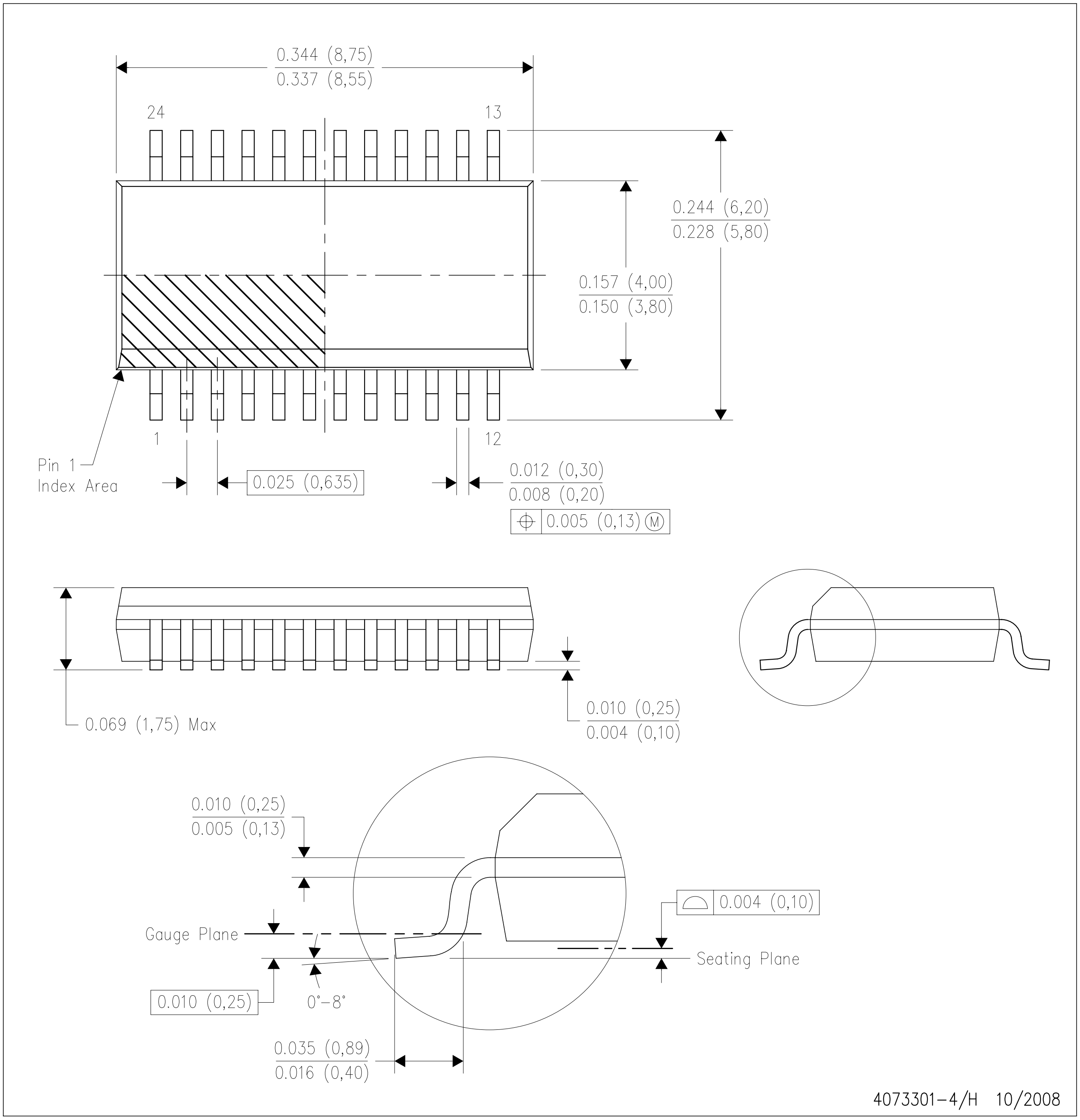


PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE

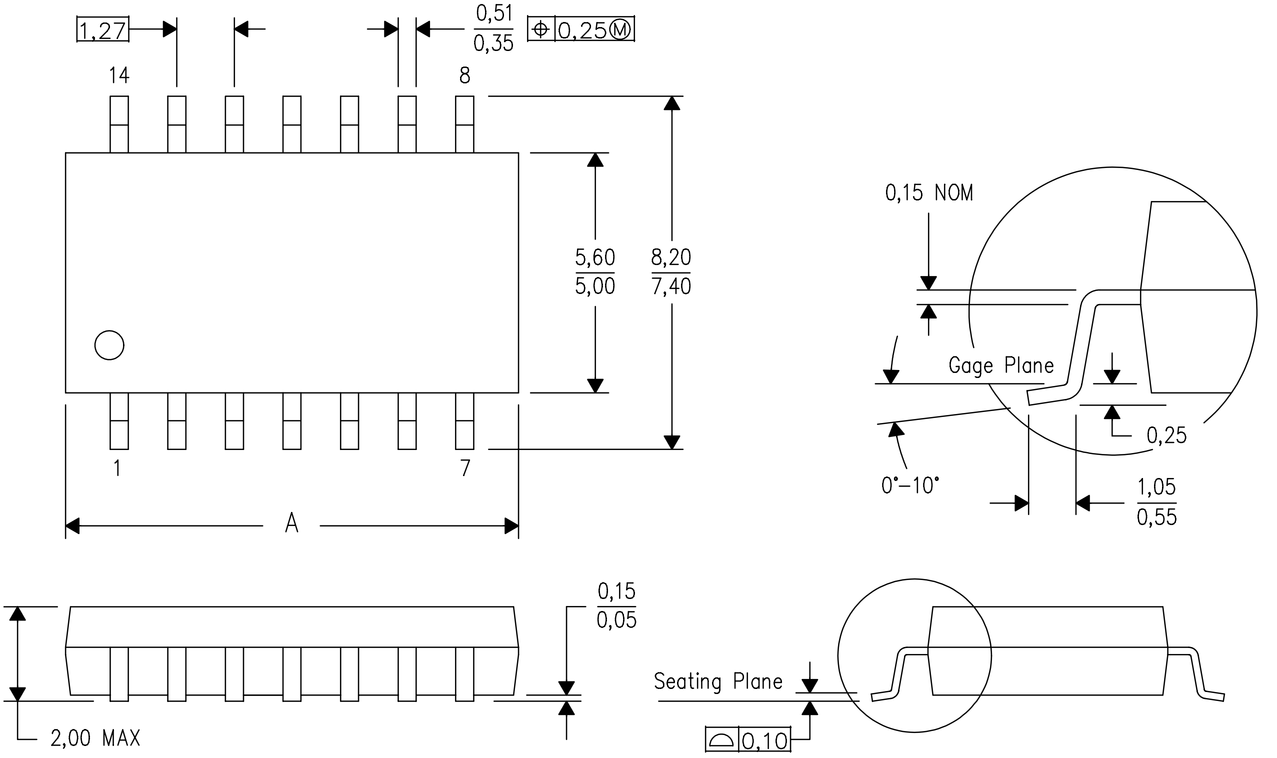


NOTES:

A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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