# SN74LVCH16374A 16-Bit Edge-Triggered D-Type Flip-Flop With 3-State Outputs

## 1 Features

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max $t_{pd}$ of 4.5 ns at 3.3 V
- Typical $V_{OLP}$ (Output Ground Bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) > 2 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- $I_{off}$ Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input and Output Voltages With 3.3-V $V_{CC}$)
- Bus Hold on Data Inputs Eliminates the Need for External Pullup or Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- Servers
- PCs and Notebooks
- Network Switches
- Electronic Points of Sale
- Wearable Health and Fitness Devices
- Toys
- Power Infrastructure

## 3 Description

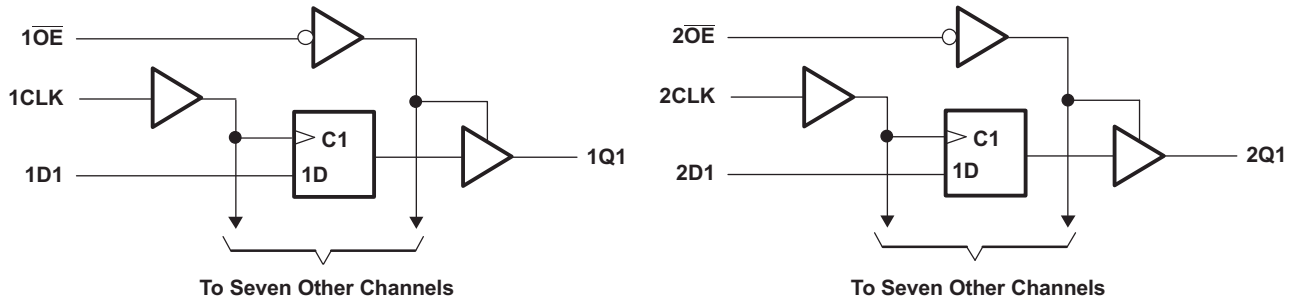
This 16-bit edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74LVCH16374A | SSOP (48) | 15.80 mm × 7.50 mm |
| | TSSOP (48) | 12.50 mm × 6.10 mm |
| | TVSOP (48) | 9.70 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## 4 Simplified Schematic



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## 5 Revision History

**Changes from Revision A (March 2005) to Revision B** **Page**

- Updated document to new TI data sheet format. ... 1
- Deleted Ordering Information table. ... 1
- Changed $I_{off}$ bullet in Features. ... 1
- Added Applications. ... 1
- Added Pin Functions table. ... 3
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- Added Handling Ratings table. ... 6
- Changed MAX operating temperature to 125°C in Recommended Operating Conditions. ... 7
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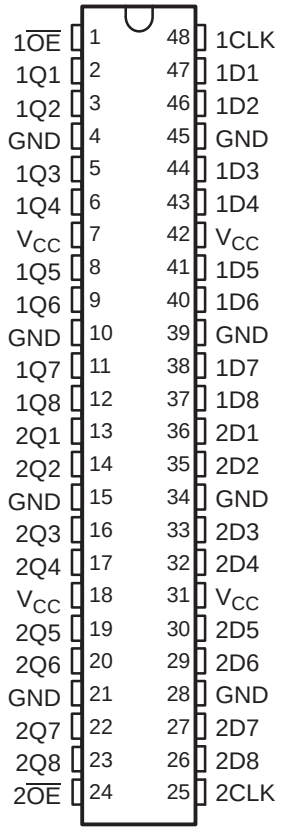
- Added Application and Implementation section. ... 13
- Added Power Supply Recommendations and Layout sections. ... 14

# 6 Pin Configuration and Functions

**DGG, DGV, OR DL PACKAGE**
**(TOP VIEW)**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | 1$\overline{OE}$ | I | Output Enable 1 |
| 2 | 1Q1 | O | 1Q1 Output |
| 3 | 1Q2 | O | 1Q2 Output |
| 4 | GND | — | Ground Pin |
| 5 | 1Q3 | O | 1Q3 Output |
| 6 | 1Q4 | O | 1Q4 Output |
| 7 | $V_{CC}$ | — | Power Pin |
| 8 | 1Q5 | O | 1Q5 Output |
| 9 | 2Q6 | O | 2Q6 Output |
| 10 | GND | — | Ground Pin |
| 11 | 1Q7 | O | 1Q7 Output |
| 12 | 1Q8 | O | 1Q8 Output |
| 13 | 2Q1 | O | 2Q1 Output |
| 14 | 2Q2 | O | 2Q2 Output |
| 15 | GND | — | Ground Pin |
| 16 | 2Q3 | O | 2Q3 Output |
| 17 | 2Q4 | O | 2Q4 Output |
| 18 | $V_{CC}$ | — | Power Pin |

## Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 19 | 2Q5 | O | 2Q5 Output |
| 20 | 2Q6 | O | 2Q6 Output |
| 21 | GND | — | Ground Pin |
| 22 | 2Q7 | O | 2Q7 Output |
| 23 | 2Q8 | O | 2Q8 Output |
| 24 | $2\overline{OE}$ | I | Output Enable 2 |
| 25 | 2CLK | I | Clock 2 Input |
| 26 | 2D8 | I | 2D8 Input |
| 27 | 2D7 | I | 2D7 Input |
| 28 | GND | — | Ground Pin |
| 29 | 2D6 | I | 2D6 Input |
| 30 | 2D5 | I | 2D5 Input |
| 31 | $V_{CC}$ | — | Power Pin |
| 32 | 2D4 | I | 2D4 Input |
| 33 | 2D3 | I | 2D3 Input |
| 34 | GND | — | Ground Pin |
| 35 | 2D2 | I | 2D2 Input |
| 36 | 2D1 | I | 2D1 Input |
| 37 | 1D8 | I | 1D8 Input |
| 38 | 1D7 | I | 1D7 Input |
| 39 | GND | — | Ground Pin |
| 40 | 1D6 | I | 1D6 Input |
| 41 | 1D5 | I | 1D5 Input |
| 42 | $V_{CC}$ | — | Power Pin |
| 43 | 1D4 | I | 1D4 Input |
| 44 | 1D3 | I | 1D3 Input |
| 45 | GND | — | Ground Pin |
| 46 | 1D2 | I | 1D2 Input |
| 47 | 1D1 | I | 1D1 Input |
| 48 | 1CLK | I | Clock 1 Input |

GQL OR ZQL PACKAGE
(TOP VIEW)

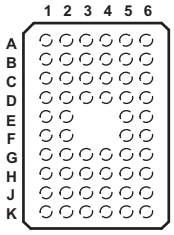



**Table 1. Pin Assignments(1)**
**(56-Ball GQL or ZQL Package)**

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | $1\overline{OE}$ | NC | NC | NC | NC | 1CLK |
| **B** | 1Q2 | 1Q1 | GND | GND | 1D1 | 1D2 |
| **C** | 1Q4 | 1Q3 | $V_{CC}$ | $V_{CC}$ | 1D3 | 1D4 |
| **D** | 1Q6 | 1Q5 | GND | GND | 1D5 | 1D6 |
| **E** | 1Q8 | 1Q7 | | | 1D7 | 1D8 |
| **F** | 2Q1 | 2Q2 | | | 2D2 | 2D1 |
| **G** | 2Q3 | 2Q4 | GND | GND | 2D4 | 2D3 |
| **H** | 2Q5 | 2Q6 | $V_{CC}$ | $V_{CC}$ | 2D6 | 2D5 |
| **J** | 2Q7 | 2Q8 | GND | GND | 2D8 | 2D7 |
| **K** | $2\overline{OE}$ | NC | NC | NC | NC | 2CLK |

(1) NC – No internal connection

GRD OR ZRD PACKAGE
(TOP VIEW)

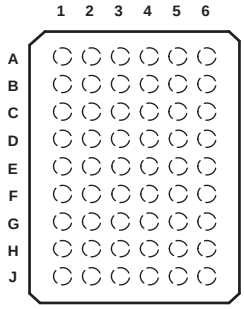



**Table 2. Pin Assignments(1)**
**(54-Ball GRD or ZRD Package)**

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | 1Q1 | NC | $1\overline{OE}$ | 1CLK | NC | 1D1 |
| **B** | 1Q3 | 1Q2 | NC | NC | 1D2 | 1D3 |
| **C** | 1Q5 | 1Q4 | $V_{CC}$ | $V_{CC}$ | 1D4 | 1D5 |
| **D** | 1Q7 | 1Q6 | GND | GND | 1D6 | 1D7 |
| **E** | 2Q1 | 1Q8 | GND | GND | 1D8 | 2D1 |
| **F** | 2Q3 | 2Q2 | GND | GND | 2D2 | 2D3 |
| **G** | 2Q5 | 2Q4 | $V_{CC}$ | $V_{CC}$ | 2D4 | 2D5 |
| **H** | 2Q7 | 2Q6 | NC | NC | 2D6 | 2D7 |
| **J** | 2Q8 | NC | $2\overline{OE}$ | 2CLK | NC | 2D8 |

(1) NC – No internal connection

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range applied to any output in the high or low state(2) (3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CC}$ is provided in the *Recommended Operating Conditions* table.

## 7.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | 0 | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | 0 | 1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | High or low state | 0 | $V_{CC}$ | V |
| | | High-impedance state | 0 | 5.5 | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | –8 | |
| | | $V_{CC}$ = 2.7 V | | –12 | |
| | | $V_{CC}$ = 3 V | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 2.7 V | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | |
| Δt/Δv | Input transition rise or fall rate | | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 7.4 Thermal Information

| THERMAL METRIC(1) | | SN74LVCH16374A | | | UNIT |
|---|---|---|---|---|---|
| | | DL | DGG | DGV | |
| | | 48 PINS | | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 68.4 | 64.3 | 78.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 34.7 | 17.6 | 30.7 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 41.0 | 31.5 | 41.8 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 12.3 | 1.1 | 3.8 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 40.4 | 31.2 | 41.3 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | $I_{OH}$ = –100 µA | | 1.65 V to 3.6 V | $V_{CC}$ – 0.2 | | | V |
| | $I_{OH}$ = –4 mA | | 1.65 V | 1.2 | | | |
| | $I_{OH}$ = –8 mA | | 2.3 V | 1.7 | | | |
| | $I_{OH}$ = –12 mA | | 2.7 V | 2.2 | | | |
| | | | 3 V | 2.4 | | | |
| | $I_{OH}$ = –24 mA | | 3 V | 2.2 | | | |
| $V_{OL}$ | $I_{OL}$ = 100 µA | | 1.65 V to 3.6 V | | | 0.2 | V |
| | $I_{OL}$ = 4 mA | | 1.65 V | | | 0.45 | |
| | $I_{OL}$ = 8 mA | | 2.3 V | | | 0.7 | |
| | $I_{OL}$ = 12 mA | | 2.7 V | | | 0.4 | |
| | $I_{OL}$ = 24 mA | | 3 V | | | 0.55 | |
| $I_I$ | $V_I$ = 0 to 5.5 V | | 3.6 V | | | ±5 | µA |
| $I_{I(hold)}$ | $V_I$ = 0.58 V | | 1.65 V | See(2) | | | µA |
| | $V_I$ = 1.07 V | | | See(2) | | | |
| | $V_I$ = 0.7 V | | 2.3 V | 45 | | | |
| | $V_I$ = 1.7 V | | | –45 | | | |
| | $V_I$ = 0.8 V | | 3 V | 75 | | | |
| | $V_I$ = 2 V | | | –75 | | | |
| | $V_I$ = 0 to 3.6 V(3) | | 3.6 V | | | ±500 | |
| $I_{off}$ | $V_I$ or $V_O$ = 5.5 V | | 0 | | | ±10 | µA |
| $I_{OZ}$ | $V_O$ = 0 to 5.5 V | | 3.6 V | | | ±10 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND | $I_O$ = 0 | 3.6 V | | | 20 | µA |
| | 3.6 V ≤ $V_I$ ≤ 5.5 V(4) | | | | | 20 | |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | 2.7 V to 3.6 V | | | 500 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 5 | | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | 6.5 | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
(2) This information was not available at the time of publication.
(3) This is the bus-hold maximum dynamic current required to switch the input from one state to another.
(4) This applies in the disabled state only.

## 7.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 150 | | 150 | | 150 | | 150 | MHz |
| $t_w$ | Pulse duration, CLK high or low | 3.3 | | 3.3 | | 3.3 | | 3.3 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | 2.4 | | 1.6 | | 1.9 | | 1.9 | | ns |
| $t_h$ | Hold time, data after CLK↑ | 0.8 | | 1 | | 1.1 | | 1.1 | | ns |

## 7.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 150 | | 150 | | 150 | | 150 | | MHz |
| $t_{pd}$ | CLK | Q | 1 | 6.5 | 1 | 4.3 | 1 | 4.9 | 1.5 | 4.5 | ns |
| $t_{en}$ | $\overline{OE}$ | Q | 1 | 6.7 | 1 | 4.7 | 1 | 5.3 | 1.5 | 4.6 | ns |
| $t_{dis}$ | $\overline{OE}$ | Q | 1 | 10.7 | 1 | 5 | 1 | 6.1 | 1.5 | 5.5 | ns |
| $t_{sk(o)}$ | | | | 1 | | 1 | | 1 | | 1 | ns |

## 7.8 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance per flip-flop | Outputs enabled | f = 10 MHz | 47 | 52 | 58 | pF |
| | | Outputs disabled | | 21 | 23 | 24 | |

## 7.9 Typical Characteristics

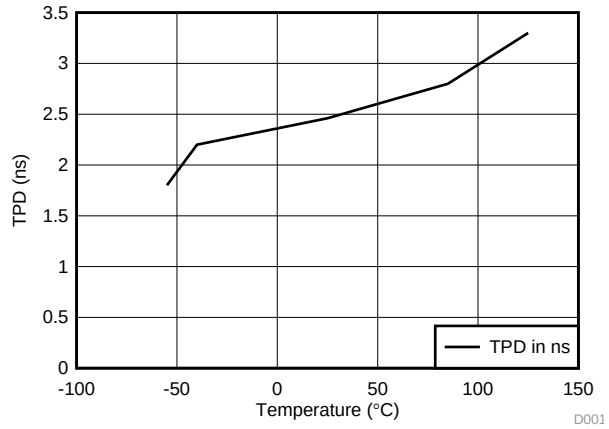



**Figure 1. TPD vs Temperature CLK to Q**

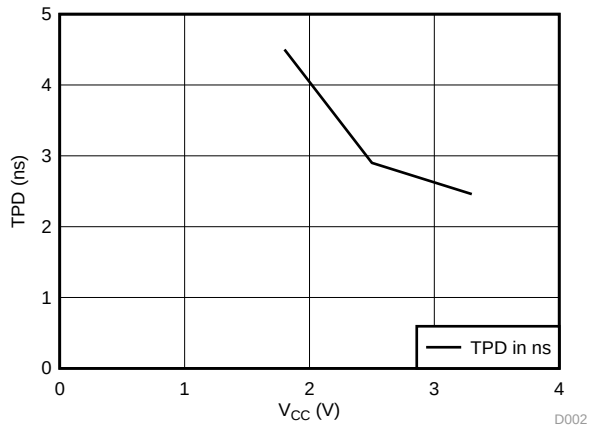
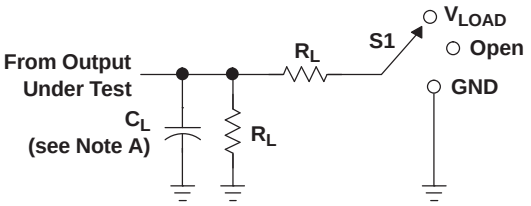



**Figure 2. TPD vs $V_{CC}$ CLK to Q**

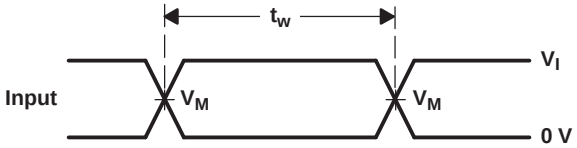
# 8 Parameter Measurement Information



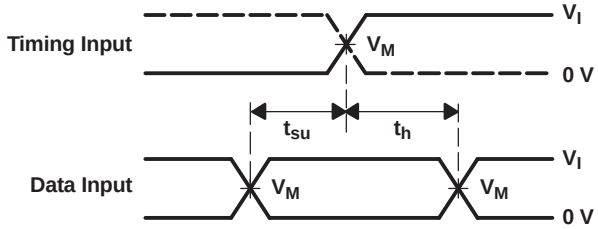

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

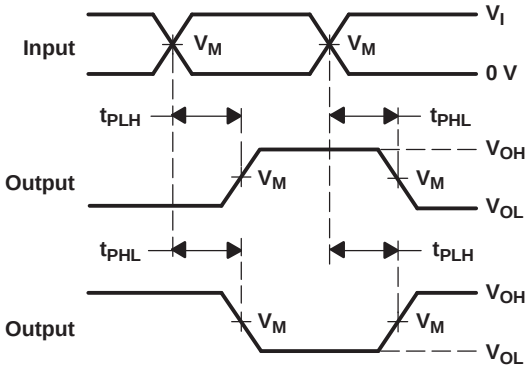
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V ± 0.3 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



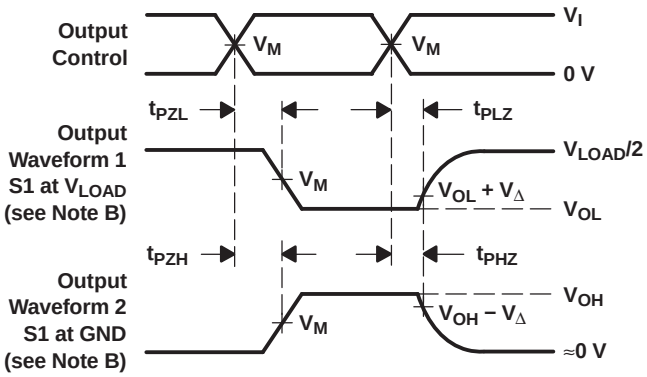

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

# 9 Detailed Description

## 9.1 Overview

This 16-bit edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pull-up components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry holds unused or not driven inputs at a valid logic state. Use of pull-up or pull-down resistors with the bus-hold circuitry is not recommended.

The SN74LVCH16374A is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## 9.2 Functional Block Diagram

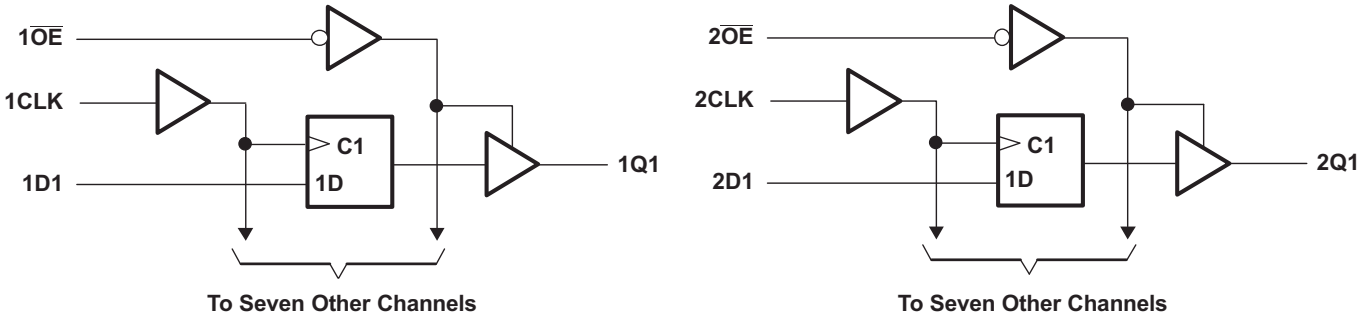



**Figure 4. Logic Diagram (Positive Logic)**

## 9.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65 V to 3.6 V
- Allows down voltage translation
  - Inputs accept voltages to 5.5 V
- $I_{off}$ feature
  - Allows voltages on the inputs and outputs when $V_{CC}$ is 0 V
- Bus Hold on data inputs eliminates the need for external pull-up or pull-down resistors

## 9.4 Device Functional Modes

**Table 3. Function Table (Each Flip-Flop)**

| INPUTS | | | OUTPUT Q |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | $Q_0$ |
| H | X | X | Z |

# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The SN74LVCH16374A device is a high-drive CMOS device that can be used for a multitude of bus-interface type applications where the data needs to be retained or latched. The SN74LVCH16374A device can produce 24 mA of drive current at 3.3 V; thus, making it ideal for driving multiple outputs and appropriate for high-speed applications up to 150 MHz. The inputs are 5.5-V tolerant allowing it to translate down to $V_{CC}$. The $I_{off}$ feature allows voltages on the inputs and outputs when $V_{CC}$ is 0 V. The Bus Hold feature eliminates the need for external pull-up or pull-down resistors on unused or floating inputs.

## 10.2 Typical Application

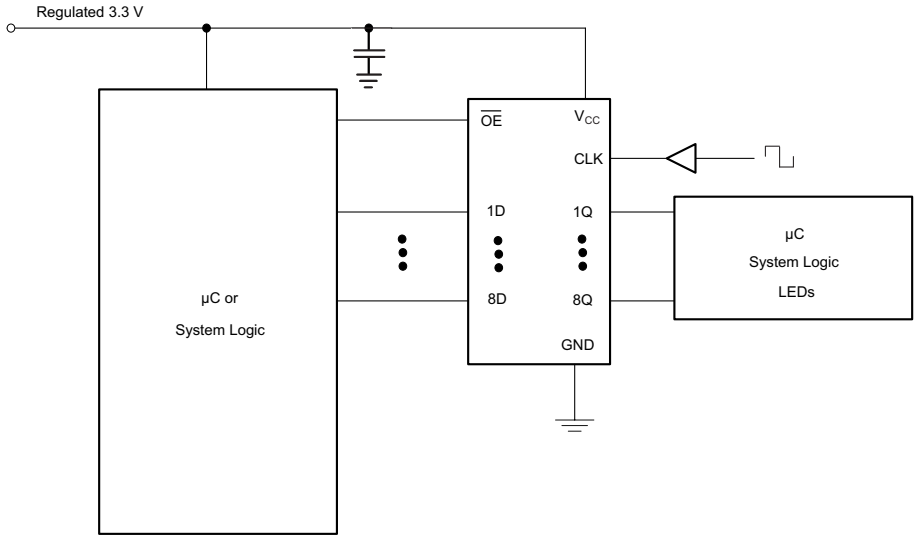



**Figure 5. Typical Application Schematic**

### 10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

### 10.2.2 Detailed Design Procedure

1. Recommended input conditions
   - Rise time and fall time specs: See (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - Specified High and low levels: See ($V_{IH}$ and $V_{IL}$) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC}$.
2. Recommend output conditions
   - Load currents should not exceed 50 mA per output and 100 mA total for the part.
   - Outputs should not be pulled above $V_{CC}$.

## Typical Application (continued)

### 10.2.3 Application Curves

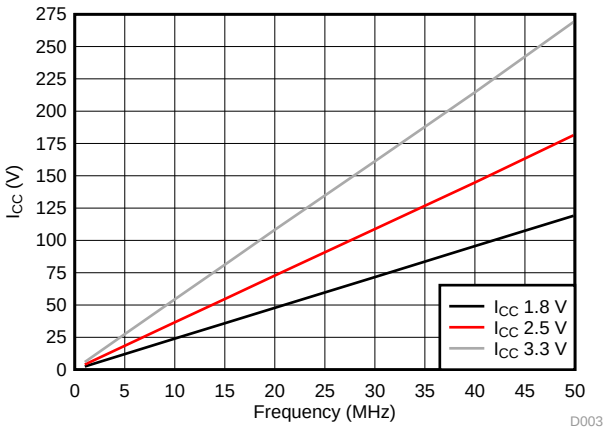



**Figure 6. $I_{CC}$ vs Frequency**

## 11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF bypass capacitor is recommended. If there are multiple $V_{CC}$ pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in Figure 7 are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver unless the part has bus hold.

### 12.2 Layout Example

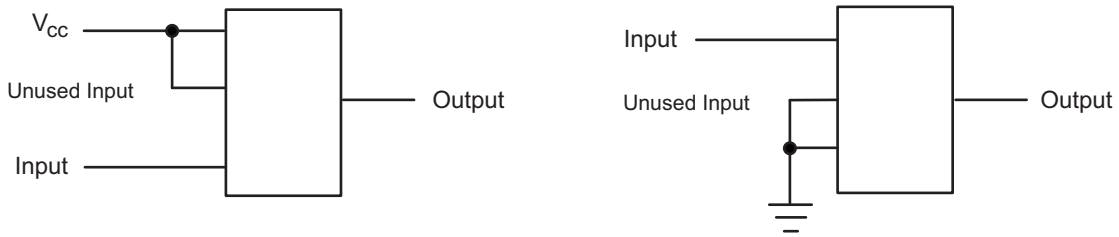



**Figure 7. Layout Diagram**

# 13 Device and Documentation Support

## 13.1 Trademarks

Widebus is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 74LVCH16374ADGGG4 | ACTIVE | TSSOP | DGG | 48 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | LVCH16374A | Samples |
| 74LVCH16374ADGGRG4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVCH16374A | Samples |
| 74LVCH16374ADLRG4 | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVCH16374A | Samples |
| SN74LVCH16374ADGG | ACTIVE | TSSOP | DGG | 48 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | LVCH16374A | Samples |
| SN74LVCH16374ADGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVCH16374A | Samples |
| SN74LVCH16374ADGVR | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LDH374A | Samples |
| SN74LVCH16374ADL | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVCH16374A | Samples |
| SN74LVCH16374ADLR | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVCH16374A | Samples |
| SN74LVCH16374AZQLR | ACTIVE | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | LDH374A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

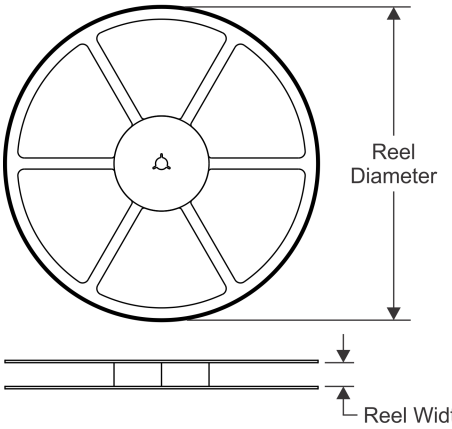
**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

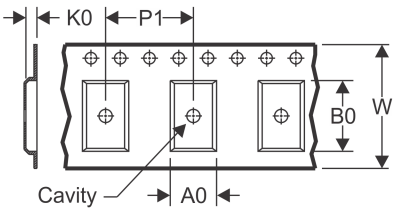
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

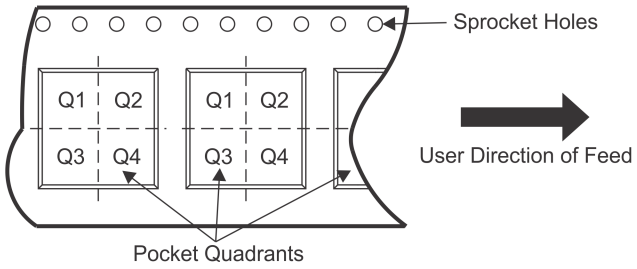



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

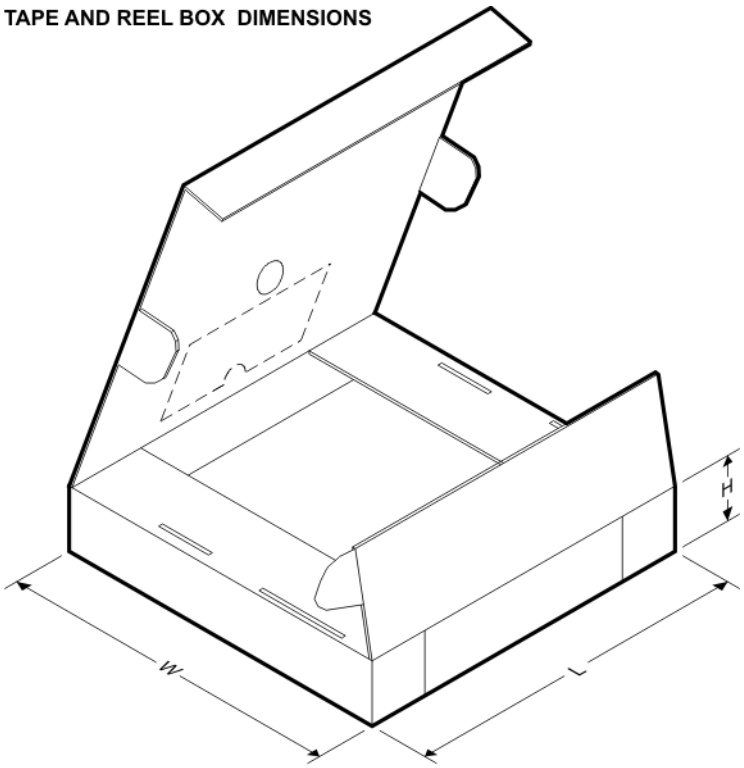
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVCH16374ADGGR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74LVCH16374ADGVR | TVSOP | DGV | 48 | 2000 | 330.0 | 16.4 | 7.1 | 10.2 | 1.6 | 12.0 | 16.0 | Q1 |
| SN74LVCH16374ADLR | SSOP | DL | 48 | 1000 | 330.0 | 32.4 | 11.35 | 16.2 | 3.1 | 16.0 | 32.0 | Q1 |
| SN74LVCH16374AZQLR | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | 330.0 | 16.4 | 4.8 | 7.3 | 1.5 | 8.0 | 16.0 | Q1 |

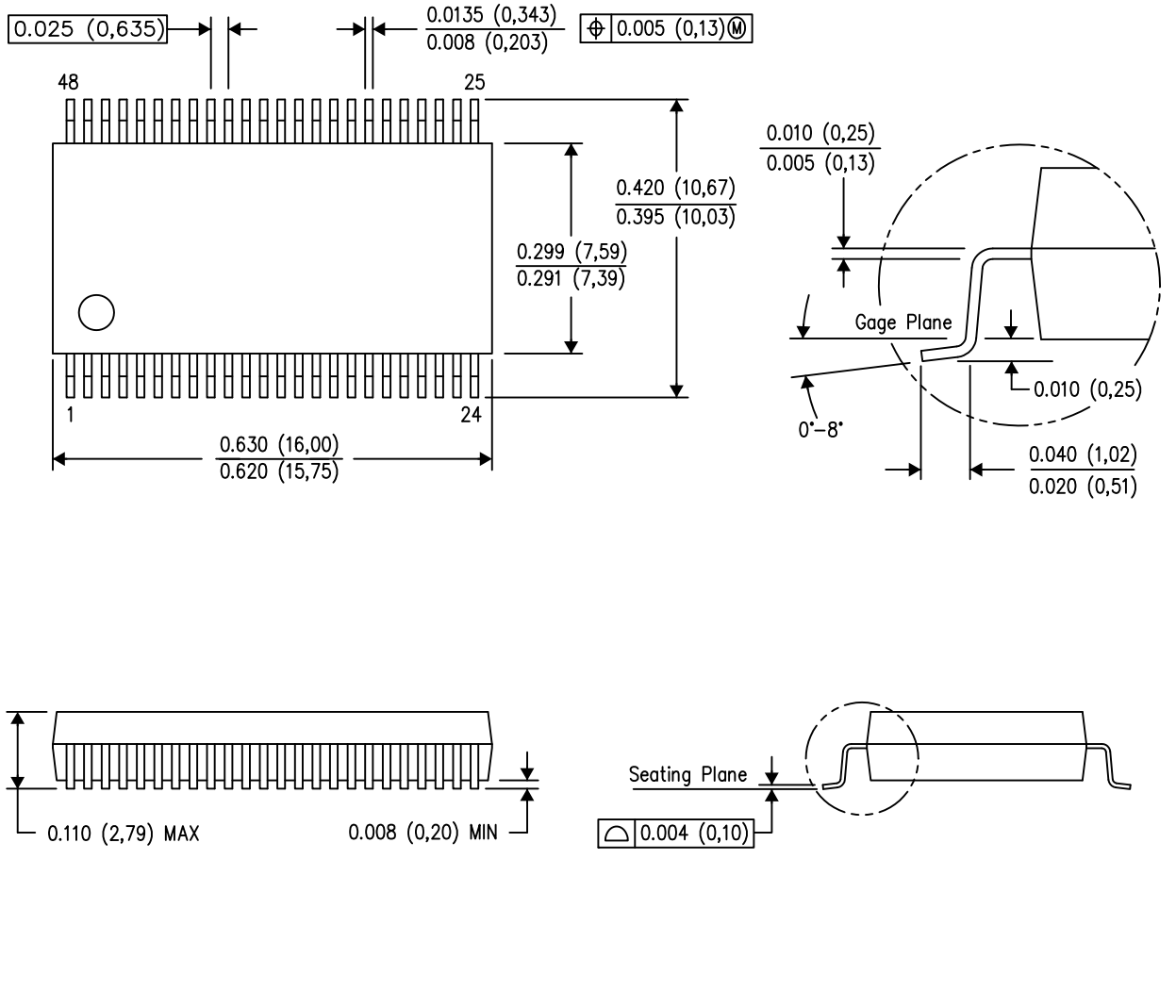
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVCH16374ADGGR | TSSOP | DGG | 48 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVCH16374ADGVR | TVSOP | DGV | 48 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVCH16374ADLR | SSOP | DL | 48 | 1000 | 367.0 | 367.0 | 55.0 |
| SN74LVCH16374AZQLR | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | 336.6 | 336.6 | 28.6 |

DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE

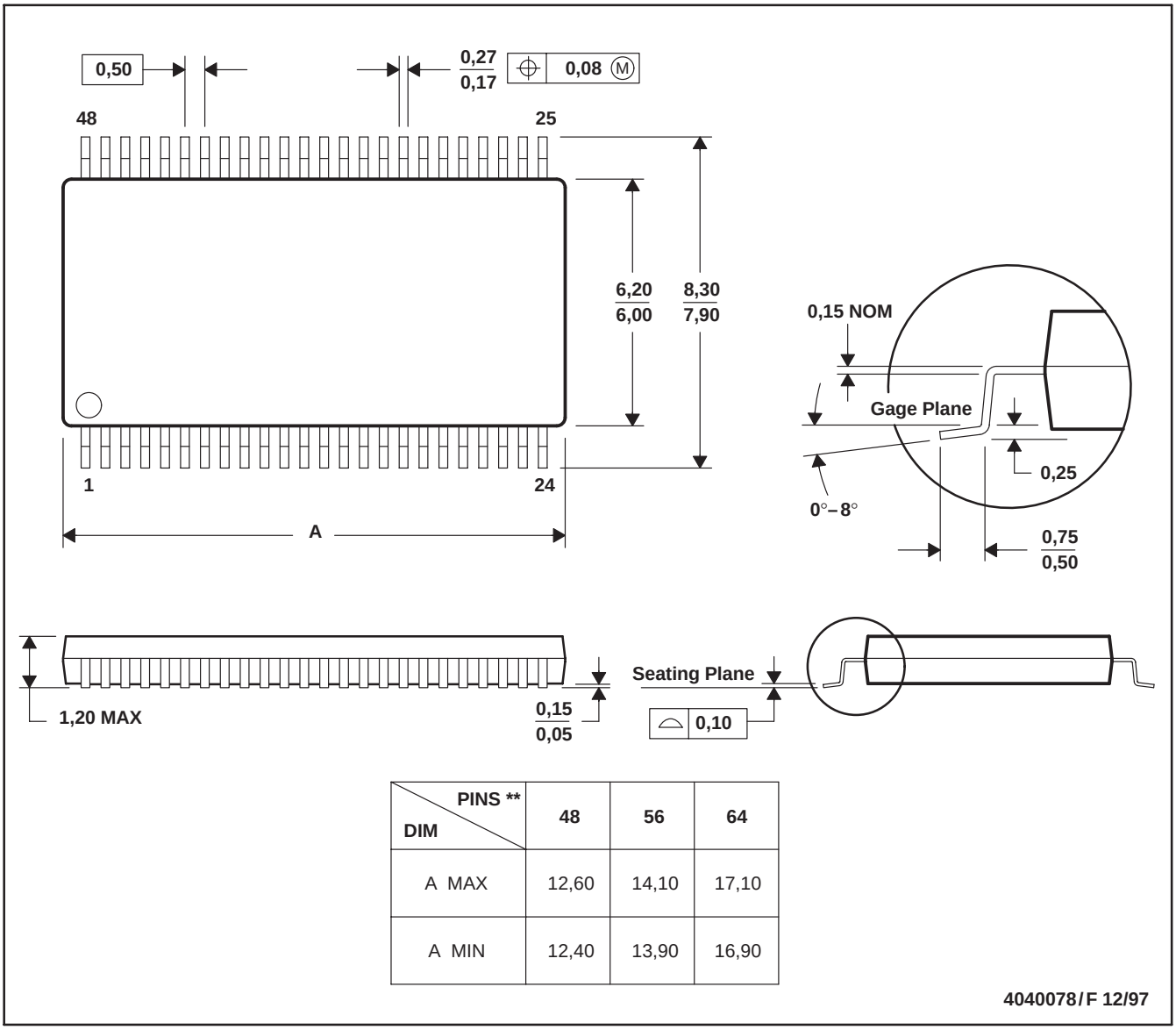



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

PowerPAD is a trademark of Texas Instruments.

**DGG (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**




| DIM \ PINS ** | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

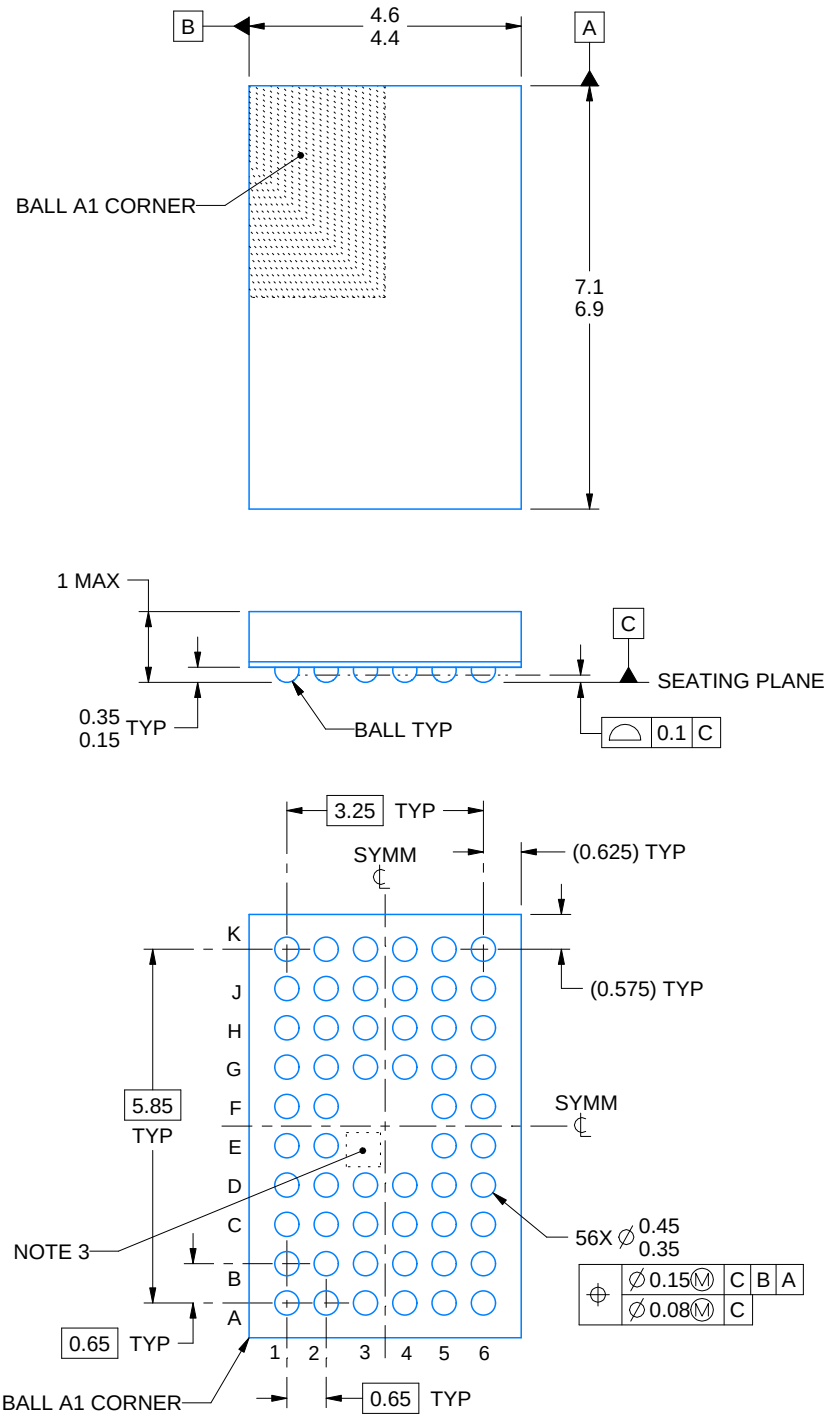
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

# PACKAGE OUTLINE

## ZQL0056A

## JRBGA - 1 mm max height

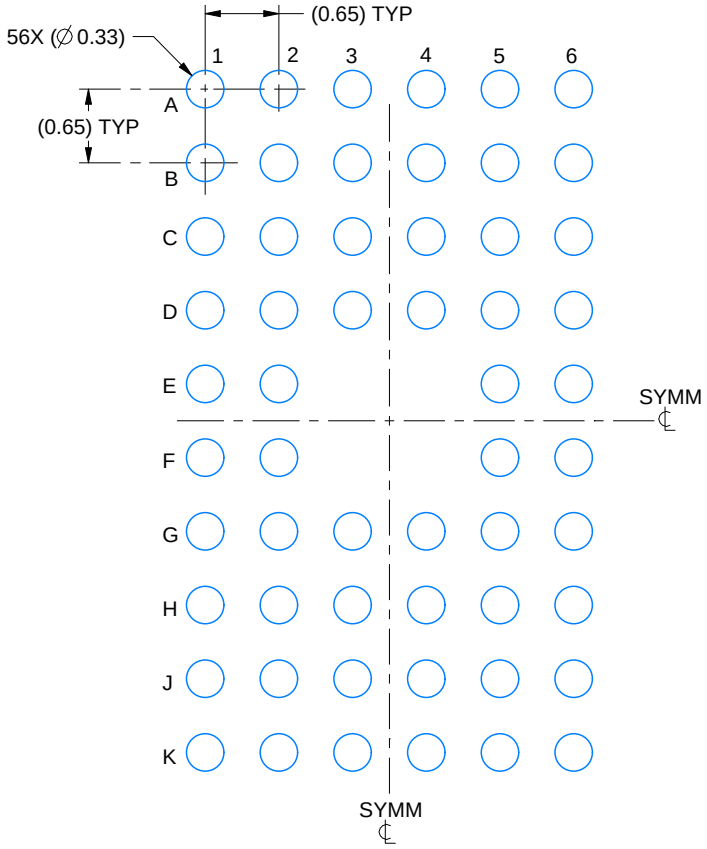
PLASTIC BALL GRID ARRAY



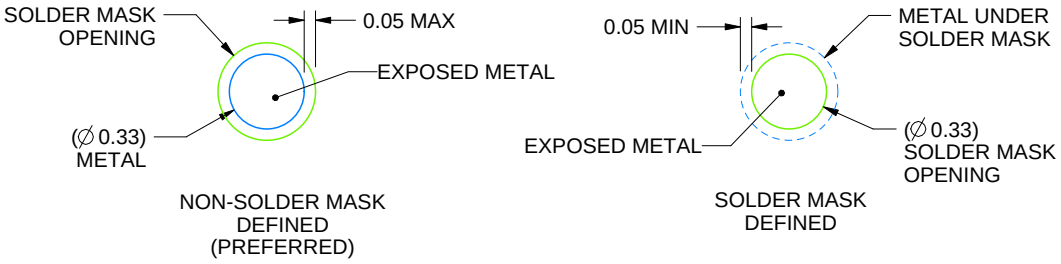

4219711/B 01/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. No metal in this area, indicates orientation.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS
NOT TO SCALE

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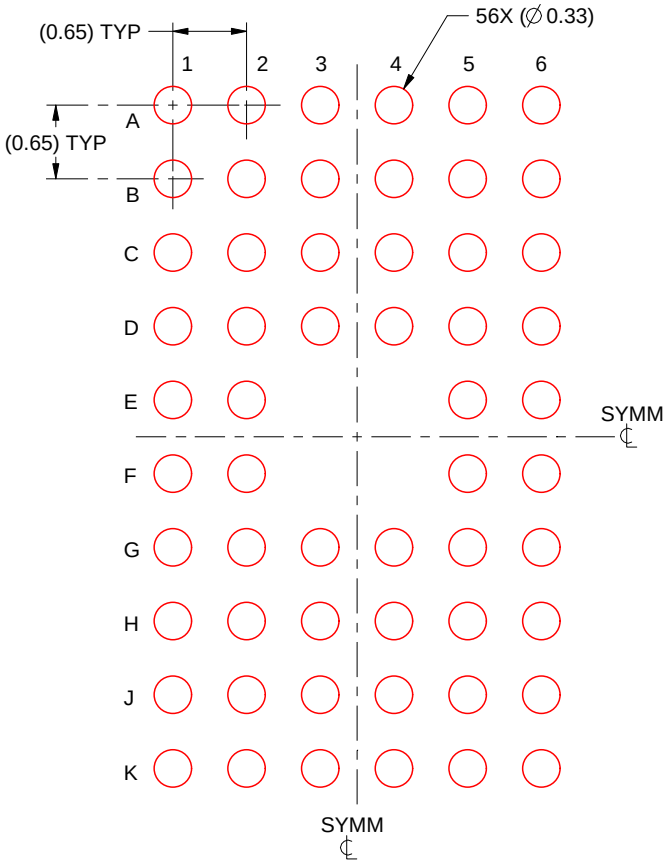
NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4219711/B 01/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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