

SN54LVTH541, SN74LVTH541 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS682G – MARCH 1997 – REVISED OCTOBER 2003

- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Unregulated Battery Operation Down to 2.7 V
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

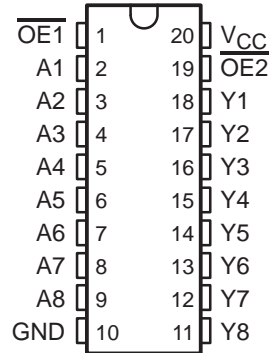
description/ordering information

These octal buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

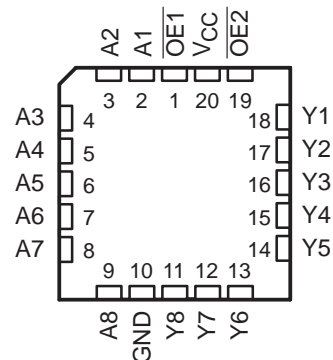
The 'LVTH541 devices are ideal for driving bus lines or buffer-memory address registers. These devices feature inputs and outputs on opposite sides of the package that facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all outputs are in the high-impedance state.

SN54LVTH541 . . . J OR W PACKAGE
SN74LVTH541 . . . DB, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LVTH541 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| -40°C to 85°C | SOIC – DW | Tube | SN74LVTH541DW | LVTH541 |
| | | Tape and reel | SN74LVTH541DWR | |
| | SOP – NS | Tape and reel | SN74LVTH541NSR | LVTH541 |
| | SSOP – DB | Tape and reel | SN74LVTH541DBR | LXH541 |
| -55°C to 125°C | TSSOP – PW | Tube | SN74LVTH541PW | LXH541 |
| | | Tape and reel | SN74LVTH541PWR | |
| | CDIP – J | Tube | SNJ54LVTH541J | SNJ54LVTH541J |
| | CFP – W | Tube | SNJ54LVTH541W | SNJ54LVTH541W |
| | LCCC – FK | Tube | SNJ54LVTH541FK | SNJ54LVTH541FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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SN54LVTH541, SN74LVTH541

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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description/ordering information (continued)

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

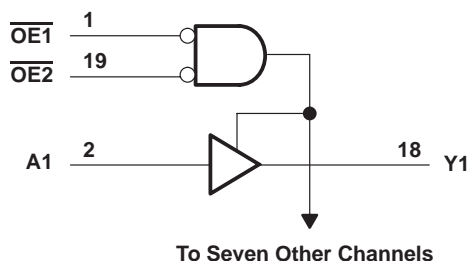
When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE

| INPUTS | | | OUTPUT |
|------------------|------------------|---|--------|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

logic diagram (positive logic)



SN54LVTH541, SN74LVTH541 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high state, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, I_O : SN54LVTH541 | 96 mA |
| SN74LVTH541 | 128 mA |
| Current into any output in the high state, I_O (see Note 2): SN54LVTH541 | 48 mA |
| SN74LVTH541 | 64 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | –50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Package thermal impedance, θ_{JA} (see Note 3): DB package | 70°C/W |
| DW package | 58°C/W |
| NS package | 60°C/W |
| PW package | 83°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

| | SN54LVTH541 | | SN74LVTH541 | | UNIT |
|--|-------------|-----|-------------|-----|------|
| | MIN | MAX | MIN | MAX | |
| V_{CC} Supply voltage | 2.7 | 3.6 | 2.7 | 3.6 | V |
| V_{IH} High-level input voltage | 2 | | 2 | | V |
| V_{IL} Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I Input voltage | | 5.5 | | 5.5 | V |
| I_{OH} High-level output current | | –24 | | –32 | mA |
| I_{OL} Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ Input transition rise or fall rate | | 10 | | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ Power-up ramp rate | 200 | | 200 | | μs/V |
| T_A Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LVTH541, SN74LVTH541

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WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54LVTH541 | | | SN74LVTH541 | | | UNIT | |
|----------------------|--|--|----------------------|------|-----|--------------|------|-----|---------------|---------------|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | | |
| V_{IK} | $V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$ | | -1.2 | | | -1.2 | | | V | |
| V_{OH} | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$ | | $V_{CC}-0.2$ | | | $V_{CC}-0.2$ | | | V | |
| | $V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$ | | 2.4 | | | 2.4 | | | | |
| | $V_{CC} = 3\text{ V}$ | $I_{OH} = -24\text{ mA}$ | 2 | | | 2 | | | | |
| V_{OL} | $V_{CC} = 2.7\text{ V}$ | $I_{OL} = 100\text{ }\mu\text{A}$ | | | | 0.2 | | | V | |
| | | $I_{OL} = 24\text{ mA}$ | | | | 0.5 | | | | |
| | $V_{CC} = 3\text{ V}$ | $I_{OL} = 16\text{ mA}$ | | | | 0.4 | | | | |
| | | $I_{OL} = 32\text{ mA}$ | | | | 0.5 | | | | |
| | | $I_{OL} = 48\text{ mA}$ | | | | 0.55 | | | | |
| | | $I_{OL} = 64\text{ mA}$ | | | | 0.55 | | | | |
| I_I | | $V_{CC} = 0\text{ or }3.6\text{ V}$, $V_I = 5.5\text{ V}$ | 10 | | | 10 | | | μA | |
| | Control inputs | $V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$ | ± 1 | | | ± 1 | | | | |
| | Data inputs | $V_{CC} = 3.6\text{ V}$ | $V_I = V_{CC}$ | 1 | | | 1 | | | |
| $V_I = 0$ | | | -5 | | | -5 | | | | |
| I_{off} | | $V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$ | | | | ± 100 | | | μA | |
| $I_{I(\text{hold})}$ | Data inputs | $V_{CC} = 3\text{ V}$ | $V_I = 0.8\text{ V}$ | 75 | | | 75 | | | μA |
| | | | $V_I = 2\text{ V}$ | -75 | | | -75 | | | |
| | | $V_{CC} = 3.6\text{ V}\ddagger$, $V_I = 0\text{ to }3.6\text{ V}$ | | | | ± 500 | | | | |
| I_{OZH} | | $V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$ | 5 | | | 5 | | | μA | |
| I_{OZL} | | $V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$ | -5 | | | -5 | | | μA | |
| I_{OZPU} | | $V_{CC} = 0\text{ to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, OE = don't care | $\pm 100^*$ | | | ± 100 | | | μA | |
| I_{OZPD} | | $V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ V to }3\text{ V}$, OE = don't care | $\pm 100^*$ | | | ± 100 | | | μA | |
| I_{CC} | | $V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$ | Outputs high | 0.19 | | | 0.19 | | | mA |
| | | | Outputs low | 5 | | | 5 | | | |
| | | | Outputs disabled | 0.19 | | | 0.19 | | | |
| $\Delta I_{CC}\S$ | | $V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$ | 0.2 | | | 0.2 | | | mA | |
| C_i | | $V_I = 3\text{ V or }0$ | 3 | | | 3 | | | pF | |
| C_o | | $V_O = 3\text{ V or }0$ | 7 | | | 7 | | | pF | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH541 | | | | SN74LVTH541 | | | | UNIT | |
|-----------|--------------------------------------|----------------|---|-----|-------------------------|-----|---|------|-----|-------------------------|------|-----|
| | | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | | $V_{CC} = 2.7\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | TYP† | MAX | MIN | | MAX |
| t_{PLH} | A | Y | 1 | 3.7 | | 4 | 1.1 | 2.4 | 3.5 | | 3.9 | ns |
| t_{PHL} | | | 1 | 3.7 | | 4 | 1.1 | 2.4 | 3.5 | | 3.9 | |
| t_{PZH} | $\overline{OE1}$ or $\overline{OE2}$ | Y | 1.4 | 5.3 | | 6.3 | 1.5 | 3.5 | 5.2 | | 6.2 | ns |
| t_{PZL} | | | 1.4 | 5.4 | | 6 | 1.5 | 3.7 | 5.3 | | 5.9 | |
| t_{PHZ} | $\overline{OE1}$ or $\overline{OE2}$ | Y | 1.4 | 5.8 | | 6.1 | 1.5 | 3.9 | 5.6 | | 5.9 | ns |
| t_{PLZ} | | | 1.4 | 5.4 | | 5.7 | 1.5 | 3 | 5 | | 5.3 | |

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

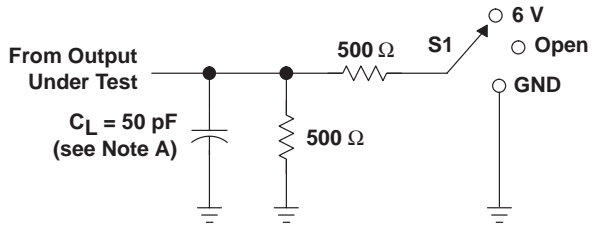
SN54LVTH541, SN74LVTH541

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WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION

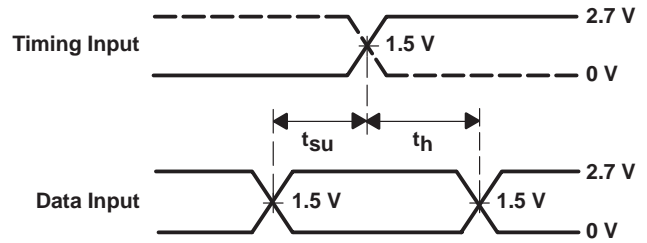


LOAD CIRCUIT

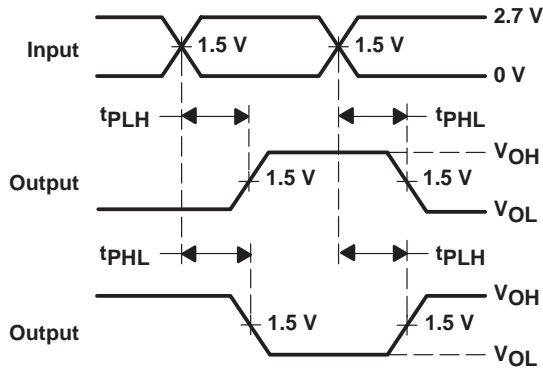
| TEST | S1 |
|-------------------|------|
| t_{PHL}/t_{PLH} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



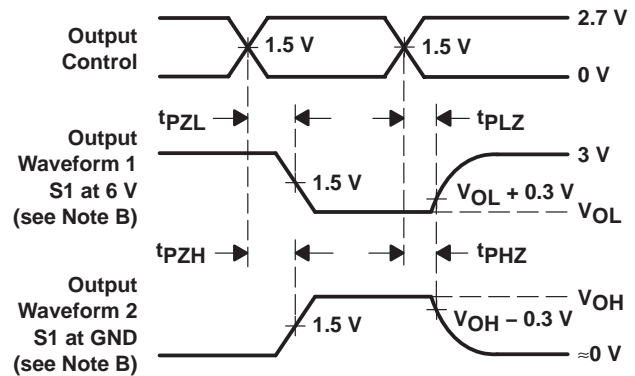
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVTH541DBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH541 | Samples |
| SN74LVTH541DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH541 | Samples |
| SN74LVTH541DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH541 | Samples |
| SN74LVTH541DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH541 | Samples |
| SN74LVTH541DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH541 | Samples |
| SN74LVTH541DWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH541 | Samples |
| SN74LVTH541NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH541 | Samples |
| SN74LVTH541PW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH541 | Samples |
| SN74LVTH541PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH541 | Samples |
| SN74LVTH541PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH541 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVTH541DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVTH541DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVTH541NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LVTH541PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVTH541DBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVTH541DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVTH541NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVTH541PWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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