28-BIT TO 56-BIT REGISTERED BUFFER WITH ADDRESS PARITY TEST ONE PAIR TO FOUR PAIR DIFFERENTIAL CLOCK PLL DRIVER

FEATURES

- **JEDEC SSTE32882 Compliant**
- **1-to-2 Register Outputs and 1-to-4 Clock Pair Outputs Support Stacked DDR3 DIMMs**
- **Chip Select Inputs Prevent Data Outputs from Changing State and Minimize System Power Consumption**
- **1.5-V Phase Lock Loop Clock Driver Buffers One Differential Clock Pair (CK and $\overline{CK}$) and Distributes to Four Differential Outputs**
- **1.5-V CMOS Inputs**
- **Checks Parity on Command and Address (CS-gated) Data Inputs**
- **Supports LVCMOS Switching Levels on $\overline{RESET}$ Input**
- **$\overline{RESET}$ Input:**
  - **Disables Differential Input Receivers**
  - **Resets All Registers**
  - **Forces All Outputs into Pre-defined States**
- **Optimal Pinout for DDR3 DIMM PCB Layout**
- **Supports Four Chip Selects**
- **Single Register Backside Mount Support**

APPLICATIONS

- **DDR3 Registered DIMMs up to DDR3-1333**
- **Single-, Dual- and Quad-Rank RDIMM**

DESCRIPTION/ORDERING INFORMATION

This JEDEC SSTE32882-compliant, 28-bit 1:2 or 26-bit 1:2 and 4-bit 1:1 registering clock driver with parity is designed for operation on DDR3 Registered DIMMs up to DDR3-1333 with V_{DD} of 1.5 V.

All inputs are 1.5-V, CMOS-compatible. All outputs are 1.5-V CMOS drivers optimized to drive DRAM signals on terminated traces in DDR3 RDIMM applications. Clock outputs Yn and $\overline{Yn}$ and control net outputs DxCKEn, $\overline{DxCSn}$, and DxODTn can each be driven with a different strength and skew to optimize signal integrity, compensate for different loading, and balance signal travel speed.

The SN74SSQE32882 has two basic modes of operation associated with the Quad Chip Select Enable ($\overline{QCSEN}$) input.

First, when the $\overline{QCSEN}$ input pin is open or pulled high, the component has two chip select inputs, $\overline{DCS0}$ and $\overline{DCS1}$, and two copies of each chip select output, $\overline{QACS0}$, $\overline{QACS1}$, $\overline{QBCS0}$ and $\overline{QBCS1}$. This mode is the *QuadCS disabled* mode. Alternatively, when the $\overline{QCSEN}$ input pin is pulled low, the component has four chip select inputs $\overline{DCS}[3:0]$, and four chip select outputs, $\overline{QCS}[3:0]$. This mode is the *QuadCS enabled* mode.

When $\overline{QCSEN}$ is high or floating, the device also supports an operating mode that allows a single device to be mounted on the back side of a DIMM array. This device can then be configured to keep the input bus termination (IBT) feature enabled for all input signals independent of MIRROR. The SN74SSQE32882. operates from a differential clock (CK and $\overline{CK}$). Data are registered at the crossing of CK going high and $\overline{CK}$ going low. This data can either be re-driven to the outputs or used to access internal control registers. Details are covered in the Function Tables (each flip-flop) with $\overline{QCSEN}$ = low.

Input bus data integrity is protected by a parity function. All address and command input signals are summed; the last bit of the sum is then compared to the parity signal delivered by the system at the PAR_IN input one clock cycle later. If these two values do not match, the device pulls the open drain output $\overline{ERROUT}$ low. The control signals (DCKE0, DCKE1, DODT0, DODT1, and $\overline{DCS}[n:0]$) are not part of this computation.

The SN74SSQE32882 implements different power-saving mechanisms to reduce thermal power dissipation and to support system power-down states. Power consumption is further reduced by disabling unused outputs.

The package design is optimal for high-density DIMMs. By aligning input and output positions towards DIMM finger-signal ordering and SDRAM ballout, the device de-scrambles the DIMM traces and allows low crosstalk designs with low interconnect latency. Edge-controlled outputs reduce ringing and improve signal eye opening at the SDRAM inputs.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_{CASE}	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C - T_{case} (see Table 1)	176ZAL	Tape and Reel	SN74SSQE32882ZALR	TE32882E
	176ZCJ	Tape and Reel	SN74SSQE32882ZCJR	TE32882E

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted). (1)

PARAMETER			VALUE	UNIT
V_{DD}	Supply voltage		–0.4 to +1.975	V
V_I	Receiver input voltage	See (2) and (3)	–0.4 to V_{DD} + 0.5	V
V_{REF}	Reference voltage		–0.4 to V_{DD} + 0.5	V
V_O	Driver output voltage	See (2) and (3)	–0.4 to V_{DD} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$	–50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$	±50	mA
I_O	Continuous output current	$0 < V_O < V_{DD}$	±50	mA
I_{CCC}	Continuous current through each V_{DD} or GND pin		±100	mA
T_{stg}	Storage temperature		–65 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 2.2 V maximum.

Table 1. Case Temperature vs Speed Node

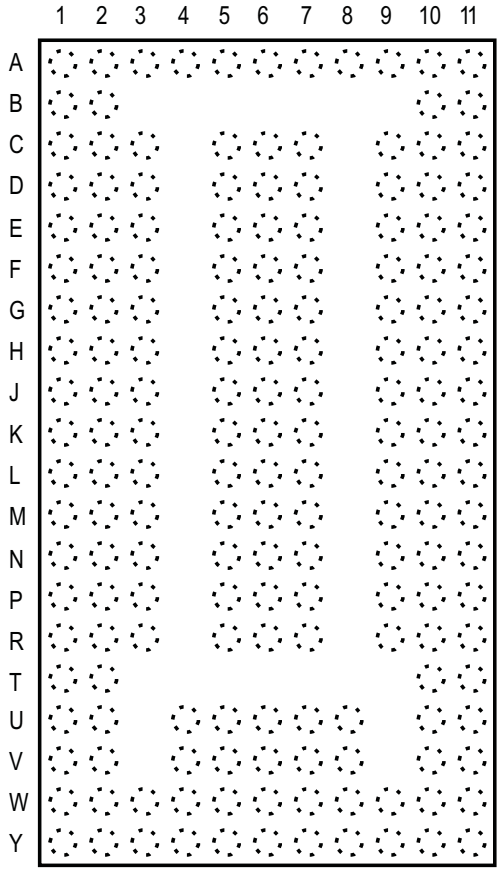
PARAMETER		DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	UNIT
T_{case}	Maximum case temperature (1)	+109	+108	+106	+103	°C

(1) The temperature values fit to JEDEC RAW cards A, B, and C. The user must keep T_{case} below the specified values in order to keep the junction temperature below +125°C. Other combinations of features and termination resistors can require lower case temperature and extra cooling. These combinations depend on the specific application.

PACKAGE INFORMATION

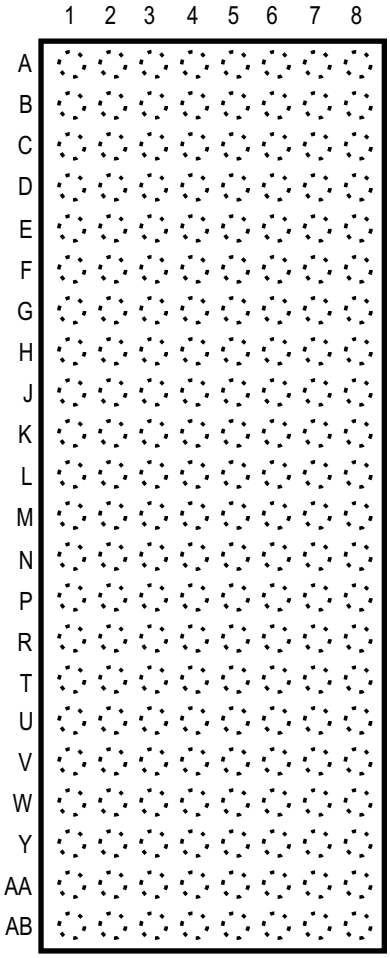
ZAL Package

The package is an 8-mm × 13.5-mm, 176-pin ball grid array (BGA) with 0.65-mm ball pitch in an 11 × 20 grid. The device pinout supports outputs on the outer two left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in such a way that two devices can be placed back-to-back for four rank modules while the data inputs share the same vias. Each input and output is located close to an associated no-ball position or on the outer two rows to allow for low-cost via technology combined with the small, 0.65-mm ball pitch.



ZCJ Package

The package is an 6-mm × 15-mm, 176-pin ball grid array (BGA) with 0.65-mm ball pitch in an 8 × 22 grid. The device pinout supports outputs on the outer two left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in such a way that two devices can be placed back-to-back for four rank modules while the data inputs share the same vias.



NOTE:

To request more information on SN74SSQE32882 DDR3 Register/PLL please contact support@ti.com .

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA00441ZALR	NRND	NFBGA	ZAL	176	2000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 85	TE32882E	
SN74SSQE32882ZALR	NRND	NFBGA	ZAL	176	2000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 85	TE32882E	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

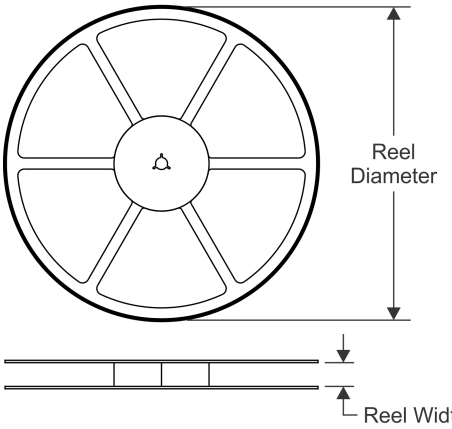
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

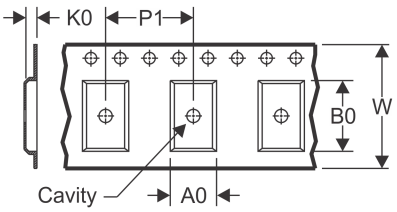
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

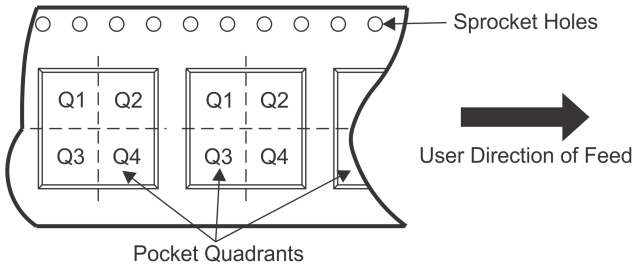


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

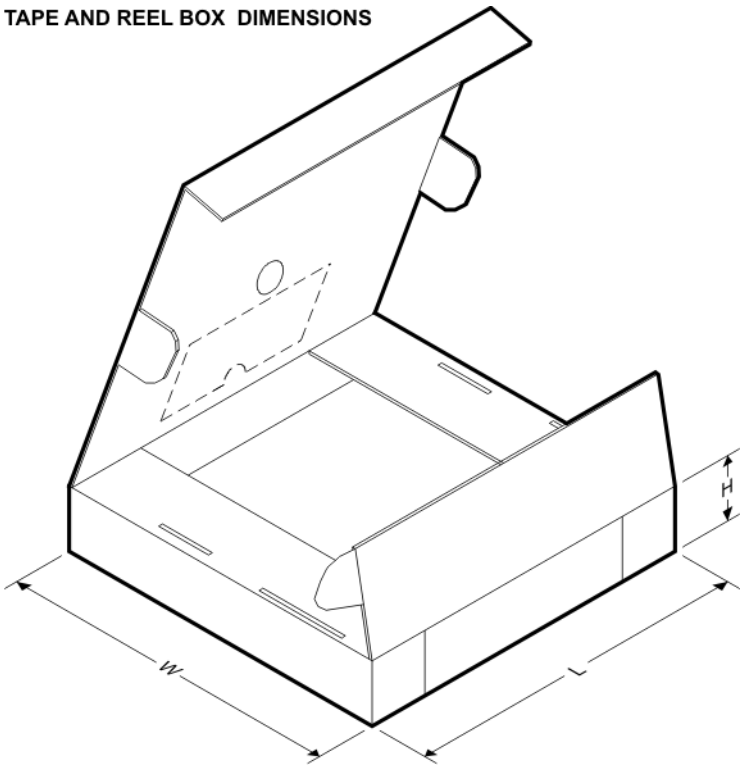
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSQE32882ZALR	NFBGA	ZAL	176	2000	330.0	24.4	8.3	13.8	1.8	12.0	24.0	Q1

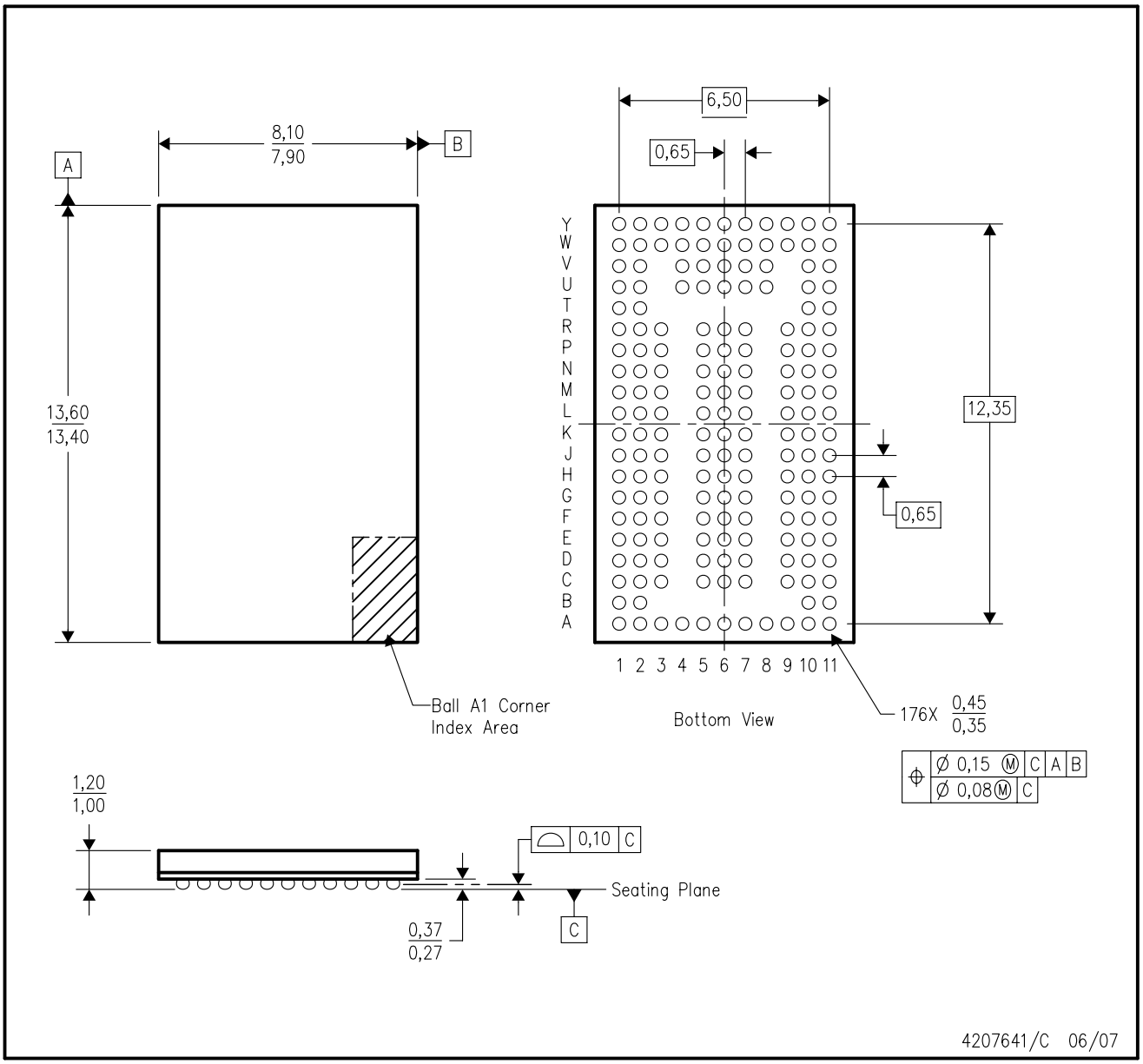
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSQE32882ZALR	NFBGA	ZAL	176	2000	336.6	336.6	31.8

ZAL (R–PBGA–N176) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This package is lead–free.

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