DisplayPort 1:1 Dual-Mode Repeater

Check for Samples: SN75DP120

FEATURES

- **DP Signal Repeater Supporting Dual-Mode DisplayPort DP1.1a (DP++) Signaling**
- **Supports Data Rates up to 2.7Gbps**
- **Participates in DP Link Training to set Output Voltage and Pre-Emphasis Levels**
- **Automatic Selectable Equalization for Improved Signal Integrity**
- **Integrated HPD Inversion and Level Translation Required on Some Source Platforms**
- **Enhanced ESD: 11 kV HBM on All Pins**
- **Enhanced Commercial Temperature Range: 0°C to 85°C**
- **36 Pin 6 × 6 QFN Package**

APPLICATIONS

- **Personal Computer Market**
  - **Desktop PC**
  - **Notebook PC**
  - **PC Docking Station**
  - **PC Standalone Video Card**

DESCRIPTION

The SN75DP120 is a single port Dual-Mode DisplayPort (DP++) repeater that regenerates the DP high speed digital link.

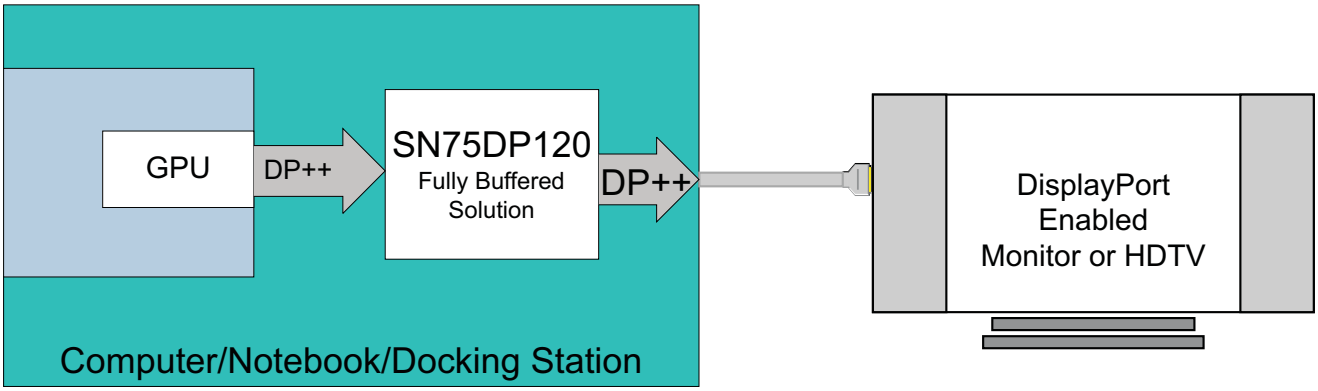
Four levels of differential output voltage swing (VOD) and four levels of pre-emphasis are supported in accordance with the DisplayPort specification version 1.1a.The device monitors the AUX channel and automatically adjusts the output signaling levels in response to link training commands. The SN75DP120 also supports multiple selectable levels of equalization to provide improved signal integrity in cases where the input link has a high level of loss. The equalization level will be automatically selected based on link training. The equalization in the DP120 is optimized to compensate losses of up to 6dB for frequencies up to 1.35GHz. This corresponds to approximately 18–24 inches of FR4 trace with 4–6mil width.

A built in level translator for the hot plug detect (HPD) line and level translator / inverter for the cable adapter detect line (CAD) allow for a reduction of the overall circuitry needed for a DisplayPort source system.

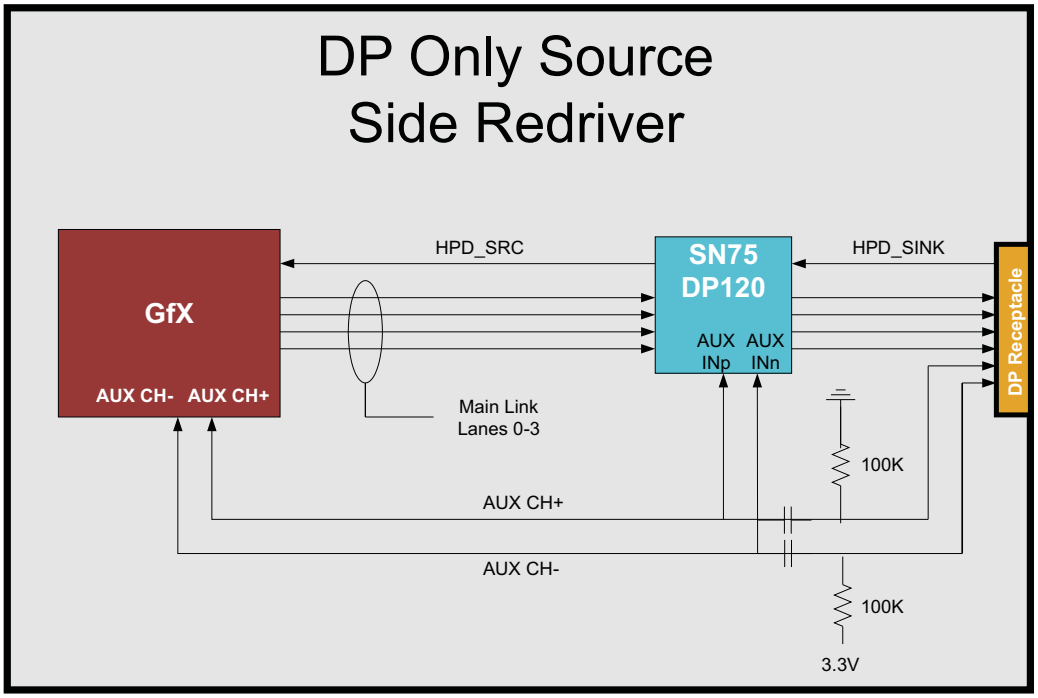
When not in use, the SN75DP120 device supports an ultra low power shutdown mode. In this mode the main link outputs are disabled and pulled to GND, and the device draws less then 40 µW of power.

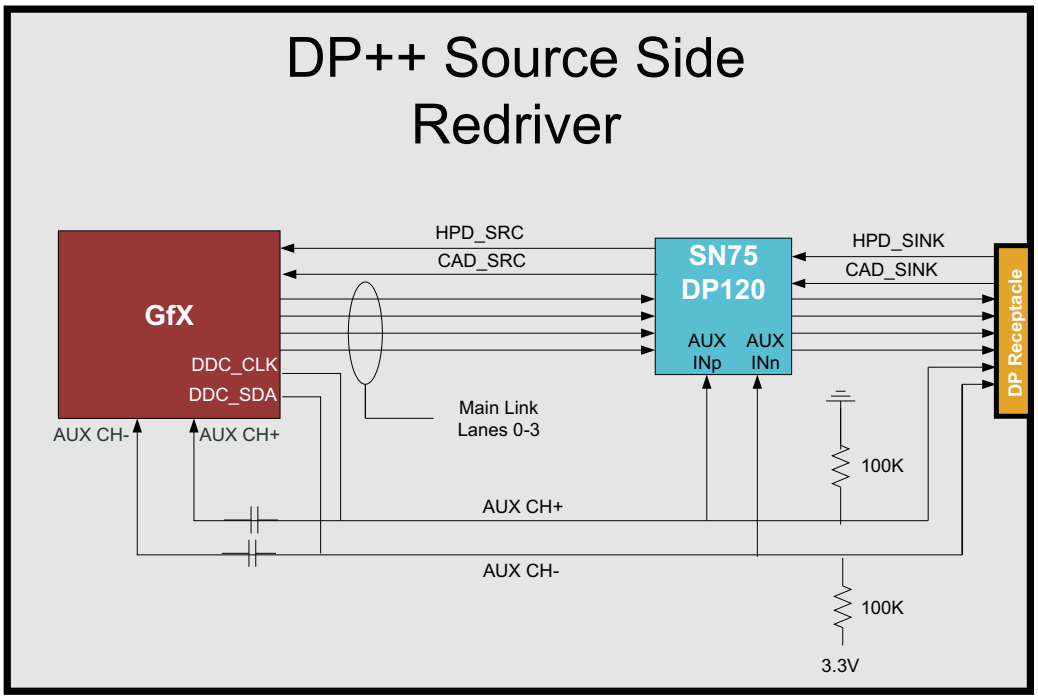
The device is characterized for an extended operational temperature range from 0°C to 85°C.

TYPICAL APPLICATION

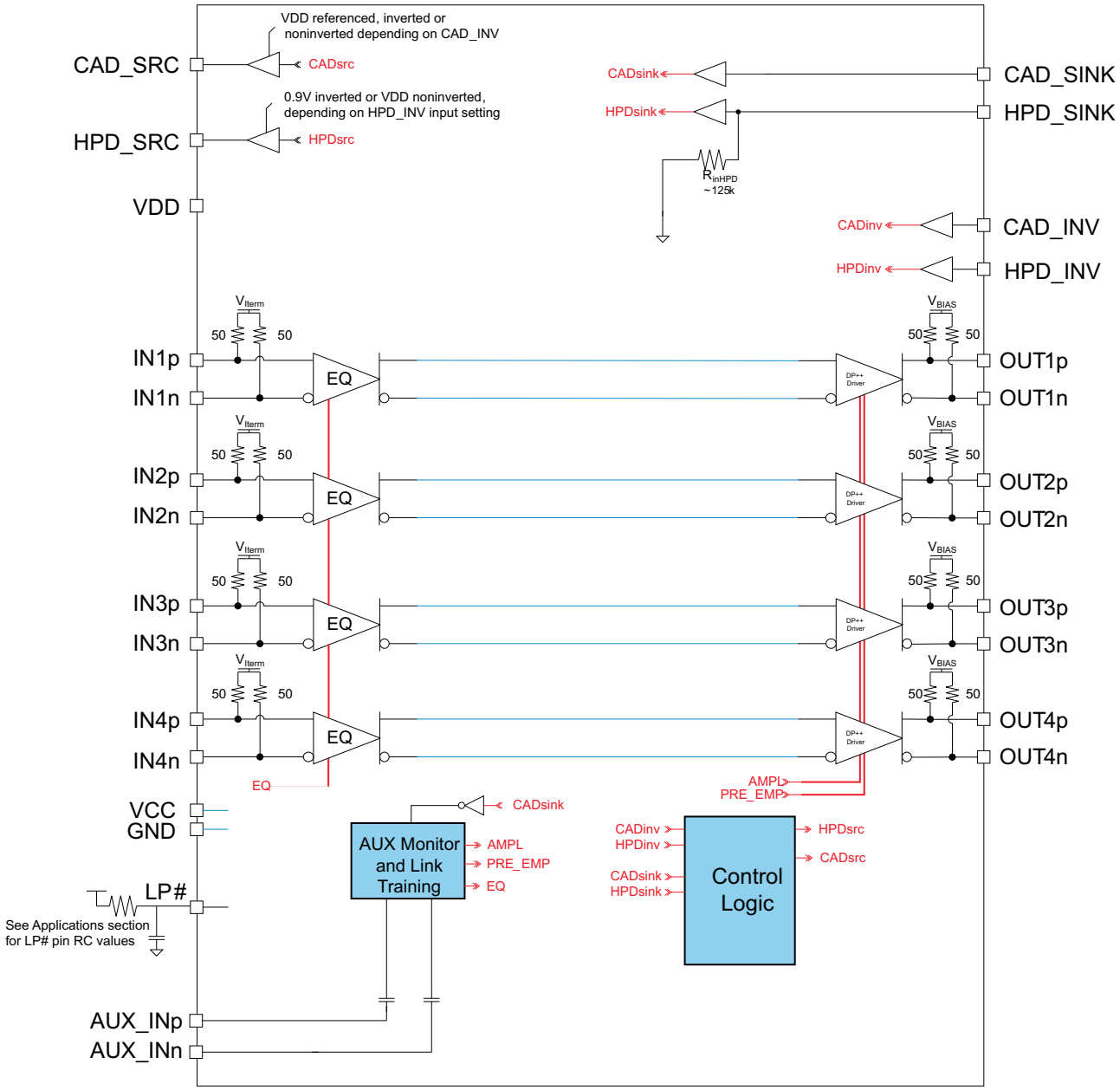


TYPICAL IMPLEMENTATION

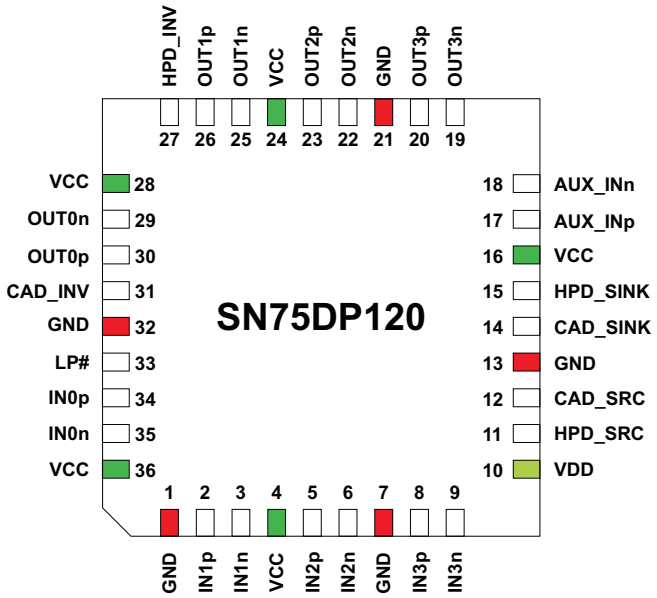




DATA FLOW BLOCK DIAGRAM



RHH PACKAGE (TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
SIGNAL	NO.		
MAIN LINK INPUT PINS			
IN0p/n	34, 35	$I_{[100\Omega\ diff]}$	DisplayPort Main Link Channel 0 Differential Input
IN1p/n	2, 3		DisplayPort Main Link Channel 1 Differential Input
IN2p/n	5, 6		DisplayPort Main Link Channel 2 Differential Input
IN3p/n	8, 9		DisplayPort Main Link Channel 3 Differential Input
MAIN LINK OUTPUT PINS			
OUT0p/n	30, 29	$O_{[100\Omega\ diff]}$	DisplayPort Main Link Channel 0 Differential Output
OUT1p/n	26, 25		DisplayPort Main Link Channel 1 Differential Output
OUT2p/n	23, 22		DisplayPort Main Link Channel 2 Differential Output
OUT3p/n	20, 19		DisplayPort Main Link Channel 3 Differential Output
HOT PLUG DETECT PINS			
HPD_SRC	11	$O_{[3.3V/0.9V\ SE]}$	Hot Plug Detect Output to the DisplayPort Source The polarity and output level of HPD_SRC is set by the HPD_INV pin
HPD_SINK	15	$I_{[CMOS]}$ w/ 125kΩ pulldown	Hot Plug Detect Input from DisplayPort Sink
AUXILIARY DATA PINS			
AUX_INp/n	17, 18	I/O	Bidirectional DisplayPort Auxiliary Data Line
CABLE ADAPTER DETECT PINS			
CAD_SRC	12	$O_{[CMOS]}$	Cable Adapter Detect Output to the DisplayPort Source The polarity of CAD_SRC is set by the CAD_INV pin.
CAD_SINK	14	$I_{[CMOS]}$	DisplayPort Cable Adapter Detect Input; No pulldown resistor on this pin.
CONTROL PINS(1)			
LP#	33	$I_{[CMOS]}$	Low Power Shutdown Mode When LP# = H; Device in Active Mode When LP# = L; Device in Shutdown mode. All main link outputs are disabled and pulled to GND; Inputs ignored. HPD_SRC follows HPD_SINK. An external capacitor may be required on this pin if it is connected to VCC by a pullup resistor. See Application Information section.

(1) (H) Logic High; (L) Logic Low

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
SIGNAL	NO.		
CAD_INV	31	I [CMOS] w/ weak pulldown	CAD output polarity Inversion When CAD_INV = H; CAD_SRC is INVERSE logic of CAD_SINK When CAD_INV = L; CAD_SRC is NON-INVERSE logic of CAD_SINK
HPD_INV	27	I [CMOS] w/ weak pulldown	HPD output polarity Inversion When HPD_INV = H; HPD_SRC is set to INVERSE logic of HPD_SINK, and HPD_SRC VOH is fixed at 0.8V to 1.1V, i.e. not referenced to VDD When HPD_INV = L; HPD_SRC is set to NON-INVERSE logic of HPD_SINK, and HPD_SRC VOH is referenced to VDD
SUPPLY AND GROUND PINS			
VDD	10		HPD_SRC (when HPD_INV = H) and CAD_SRC Supply
VCC	4, 16, 24, 28, 36		3.3V Supply
GND	1, 7, 13, 21, 32		Ground

STATUS DETECT AND OPERATING MODES FLOW DIAGRAM

The SN75DP120 switches between power saving and active modes in the following way:

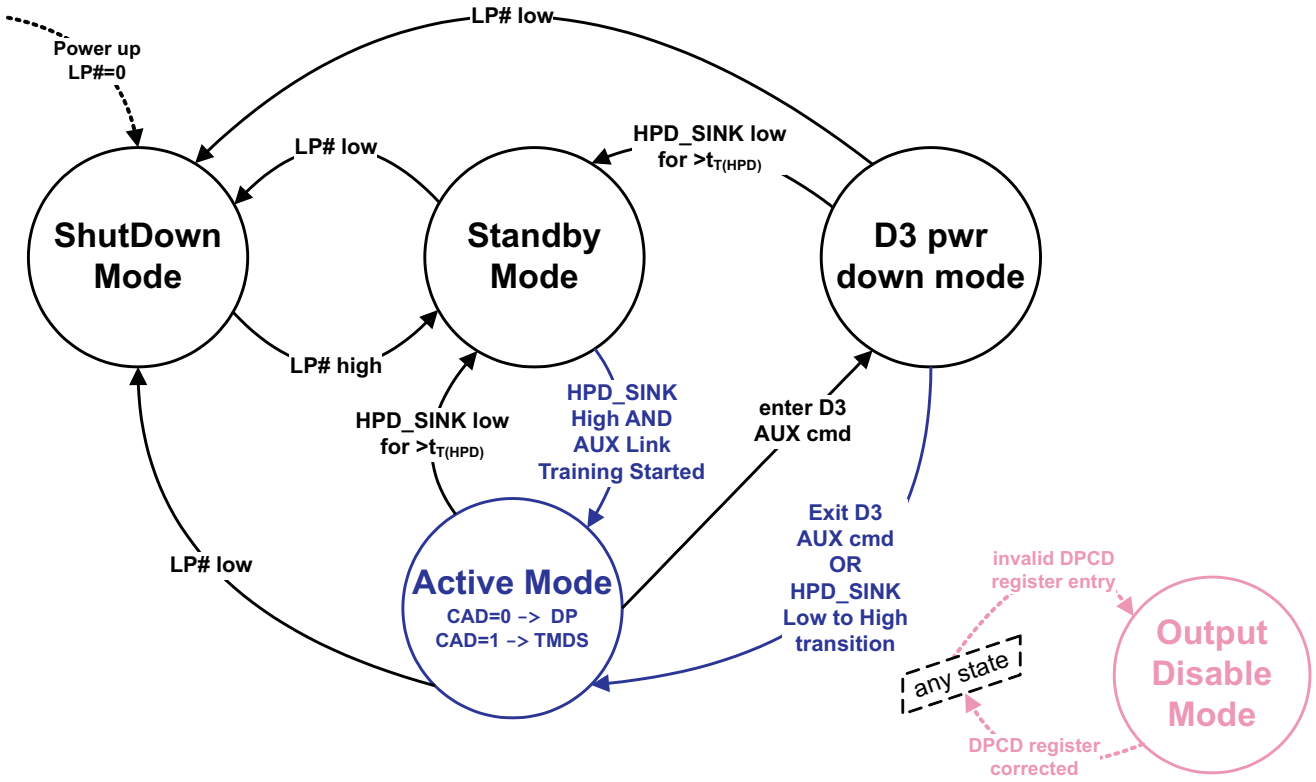


Figure 1. SN75DP120 Operational Modes Flow Chart

Table 1. Description of SN75DP120 Modes

MODE	CHARACTERISTICS	CONDITIONS
ShutDown Mode	Least amount of power consumption (most circuitry turned off); HPD_SRC reflects HPD_SINK state, all other outputs are high impedance and all other inputs are ignored. **DPCD registers and logic are held reset to default values**	LP# is low
Standby Mode	Low power consumption; main link inputs and outputs are disabled, AUX monitoring is enabled	LP# is high; HPD_SINK low for longer than $t_{T(HPD)}$
D3 Power Down Mode	Low power consumption; main link inputs and outputs disabled, AUX monitoring is enabled	LP# is high; AUX command requested DP sink to enter D3 power saving mode
Active Mode	Data transfer (normal operation); The device is either in TMDS mode (CAD_SINK=high) or DP mode (CAD_SINK=low); In DP mode, the AUX monitor is actively monitoring for link training, and the output signal swing, input equalization level and lane count depend on the link training. At power-up all main link outputs are disabled by default. AUX Link training is necessary to overwrite the DPCD registers to enable main link outputs. In TMDS mode, the output signal swing will be 600mVp-p, and transactions on the AUX lines will be ignored.	LP# is high; HPD_SINK is high HPD_SINK can also be low for less than $t_{T(HPD)}$ (e.g. sink interrupt request to source) Link Training has begun or completed
Output Disable Mode	DPCD write commands on the AUX bus detected by the SN75DP120 will also write to the local DP120 DPCD register. The local DPCD registers should always be written with valid entries. If register 101h or 103h is written with an invalid value, the SN75DP120 disables the OUTx main link output signals, forcing the DP sink to issue an interrupt. The DP source can now re-train the link using valid DPCD register values. As soon as all DPCD registers contain a valid entry, the SN75DP120 switches back into the appropriate mode of operation. For a list of valid and invalid DPCD register entries refer to Table 3 and the DP1.1a specification Table 2-52 and Table 3-12.	EN is high DPCD register 101h or 103h entry is invalid

Table 2. Transition Between Operational Modes

MODE TRANSITION	USE CASE	TRANSITION SPECIFICS
Shutdown → Standby	Activate DP120	1. LP# transitions from low to high 2. Receiver enters Standby mode 3. AUX listener turns on and begins to monitor the AUX lines
Standby → Active	Turn on main link (monitor plugged in)	1. HPD_SINK input asserts high 2. Main link outputs turn on
Active → D3	DP source requests temporary power down for power savings	1. Receive D3 entry command on AUX 2. Main link inputs and outputs are disabled 3. AUX monitor remains active
D3 → Active	Exit temporary power down	1. AUX channel receives D3 exit command or HPD_SINK transitions from low to high 2. Enable main link
D3 → Standby	Exit temporary power down	1. HPD_SINK de-asserted to low for longer than $t_{T(HPD)}$
Active → Standby	turn off main link (monitor unplugged)	1. HPD_SINK de-asserted for longer than $t_{T(HPD)}$ 2. Main link inputs and outputs are disabled
Active/Standby → Shutdown	Turn off DP120	1. LP# pulled low 2. AUX, Main link inputs and outputs are disabled 3. Most IC circuitry is shut down for ultra low power consumption 4. HPD_SRC reflects HPD_SINK
Any State → Output Disable Mode	Invalid DPCD write value to register 101h or 103h	1. OUTx becomes disabled

Table 2. Transition Between Operational Modes (continued)

MODE TRANSITION	USE CASE	TRANSITION SPECIFICS
Output Disable Mode → Any State	DPCD register values correct to a valid register entry	1. Appropriate mode is re-entered

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
SN75DP120RHHR	DP120	36-pin QFN reel (large)
SN75DP120RHHT	DP120	36-pin QFN reel (small)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE / UNIT
Supply voltage range(2)	VDD	–0.3 V to 4.0 V
Supply voltage range	VCC	–0.3 V to 4.0 V
Voltage range	Main Link I/O (INx, OUTx)	–0.3 V to VCC + 0.3 V
	Main Link I/O (INx, OUTx) differential voltage	1.5V
	HPD_SINK and CAD_SINK	–0.3 V to 5.5 V
	HPD_SRC and CAD_SRC	–0.3 V to VCC + 0.3 V
	Auxiliary (AUX_IN)	–0.3 V to 5.5 V
	Control pins	–0.3 V to 4.0 V
Electrostatic discharge	Human body model(3)	11 kV
	Charged-device model(4)	±1500 V
	Machine model(5)	±200 V
Continuous power dissipation		See Dissipation Rating Table

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-E
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-D
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \leq 25°C$	DERATING FACTOR (1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
36-pin QFN (RHH)	Low-K	1250 mW	12.5 mW/°C	500 mW
	High-K	3095 mW	30.95 mW/°C	1238 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX (1)	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	4x4 Thermal vias under PowerPAD		4.35		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			20.3		°C/W
P_N	Device power in Active Mode	LP# = VCC, ML: VOD = 1200mVp-p, 2.7Gbps PRBS; AUX: VID = 1000mVp-p, 1Mbps PRBS; VDD= 3.6V, VCC=3.6V Highest power level. All lanes running at largest VOD swing.			720	mW
P_{PDWN}	Device Power under D3 Power Down Mode or Standby	LP# = VCC, ML: VID = 0mVp-p, AUX: VID = 0mVp-p; VDD= 3.6V, VCC=3.6V			44	mW
P_{LP}	Device power dissipation in Shutdown mode	LP# = 0V, VDD= 3.6V, VCC=3.6V, HPD_INV = NC, 0V			40	µW
		LP# = 0V, VDD= 3.6V, VCC=3.6, HPD_INV=VCC			2.5	mW

(1) The maximum rating is simulated under VDD, VCC = 3.6V.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	HPD_SRC and CAD_SRC reference voltage; HPD_SRC Ref voltage only when HPD_INV = 0V	1.62		3.6	V
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	0		85	°C
MAIN LINK DIFFERENTIAL PINS (INX, OUTX)					
V_{ID}	Peak-to-peak input differential voltage	0.20		1.40	Vp-p
d_R	Data rate			2.7	Gbps
R_t	Termination resistance	40	50	60	Ω
V_{CM}	Output common mode voltage	0		2	V
AUXILIARY PINS (AUX_IN)					
V_I	Input voltage	0		5.25	V
$d_{R(AUX)}$	Auxiliary data rate			1	Mbps
HPD_SINK AND CAD_SINK					
V_{IH}	High-level input voltage	1.9		3.6	V
V_{IL}	Low-level input voltage	0		0.8	V
CONTROL PINS (LP#, HPD_INV, CAD_INV)					
V_{IH}	High-level input voltage	1.9		3.6	V
V_{IL}	Low-level input voltage	0		0.8	V

DEVICE POWER

The SN75DP120 main and AUX link is designed to run from a single supply voltage of 3.3V. However since the device has a built in level shifter, another supply voltage (VDD) is needed to set the voltage level of HPD_SRC and CAD_SRC pins.

NOTE

An external capacitor may be required on LP# pin if that pin is tied to the supply through a pullup resistor. The capacitor specifies a proper power on reset for the device. See Applications section for recommended resistor and capacitor values.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current under active operating mode	LP# = VCC, ML: VOD = 1200mVp-p, 2.7Gbps PRBS; AUX: VID = 1000mVp-p, 1Mbps PRBS; VDD= 3.6V, VCC=3.6V		165	200	mA
I_{PDWN}	Device power under power down mode (D3) or standby main link disabled	LP# = VCC, ML: VID = 0mVp-p, AUX: VID = 0mVp-p; VDD= 3.6V, VCC=3.6V		8	12	mA
I_{LP}	Low power current	LP# = 0V, VDD= 3.6V, VCC=3.6V HPD_INV, CAD_INV = NC, 0V		1	10	µA
		LP# = 0V, VDD= 3.6V, VCC=3.6V HPD_INV=VCC		400	640	
I_{DD}	Supply current	VDD = 3.6V, HPD_INV = VDD			4	mA
t_{PWDNEX}	D3 Powerdown or standby mode exit time	Total time for the device to exit from D3 or standby state to active mode		1.2	1.8	µs

HOT PLUG AND CABLE ADAPTER DETECT

The SN75DP120 has an integrated 125KΩ pull down on the HPD_SINK input pin. The HPD and CAD timing diagrams in this section are for the non-inverting case. The same timing diagrams apply for the inverting case except the output is inverted. The VOH level of CAD_SRC follows that of VDD irrespective of CAD_INV setting. However VOH for HPD_SRC depends on HPD_INV setting. When HPD_INV is low or left floating, HPD_SRC VOH follows that of VDD. When HPD_INV = H then HPD_SRC VOH is set to 0.8V – 1.1V irrespective of VDD.

Explanation of HPD power management and interrupt behavior of the SN75DP120 is located in the Application Information section at the end of the datasheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HPD_INV, CAD_INV = L						
$V_{OH3.3}$	High-level output voltage (CAD_SRC and HPD_SRC)	VDD = 3.3 V, I_{OH} = –100 µA, CAD_SINK, HPD_SINK = H	3			V
$V_{OH2.5}$	High-level output voltage (CAD_SRC and HPD_SRC)	VDD = 2.5 V, I_{OH} = –100 µA, CAD_SINK, HPD_SINK = H	2.25			V
$V_{OH1.8}$	High-level output voltage (CAD_SRC and HPD_SRC)	VDD = 1.8 V, I_{OH} = –100 µA, CAD_SINK, HPD_SINK = H	1.62		1.8	V
$V_{OL3.3}$	High-level output voltage (CAD_SRC and HPD_SRC)	VDD = 3.3 V, I_{OL} = 100 µA, CAD_SINK, HPD_SINK = L			0.1	V
$V_{OL2.5}$	Low-level output voltage (CAD_SRC and HPD_SRC)	VDD = 2.5 V, I_{OL} = 100 µA, CAD_SINK, HPD_SINK = L			0.1	V
$V_{OL1.8}$	Low-level output voltage (CAD_SRC and HPD_SRC)	VDD = 1.8 V, I_{OL} = 100 µA, CAD_SINK, HPD_SINK = L			0.1	V
HPD_INV = H						
$V_{OH1.1}$	High-level output voltage (HPD_SRC)	I_{OH} = –100 µA, HPD_SINK = L	0.8	0.9	1.1	V
$V_{OL1.1}$	Low-level output voltage (HPD_SRC)	I_{OH} = 100 µA, HPD_SINK = H			0.1	V
I_{IH}	High-level input current (HPD_SINK, CAD_SINK, HPD_INV, CAD_INV)	V_{IH} = 2.0 V, V_{DD} = 3.6 V (Leakage includes pull down resistor)	–5		35	µA
I_L	lLow-level input current (HPD_SINK, CAD_SINK, HPD_INV, CAD_INV)	V_{IL} = 0.8 V, V_{DD} = 3.6 V (Leakage includes pull down resistor)	–5		35	µA
R_{HPDIN}	Weak pull down resistor on HPD_SINK		100	125	150	kΩ

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD(CAD)}$	Propagation delay	VDD = 3.3 V, See Figure 2 and Figure 5		6.4	22	ns
$t_{PD(HPD)}$	Propagation delay	VDD = 3.3 V, See Figure 2 and Figure 3, C_L = 20 pF		6.4	22	ns
$t_{T(HPD)}$	HPD logic shut off time	VDD = 3.3 V, See Figure 4	250		550	ms

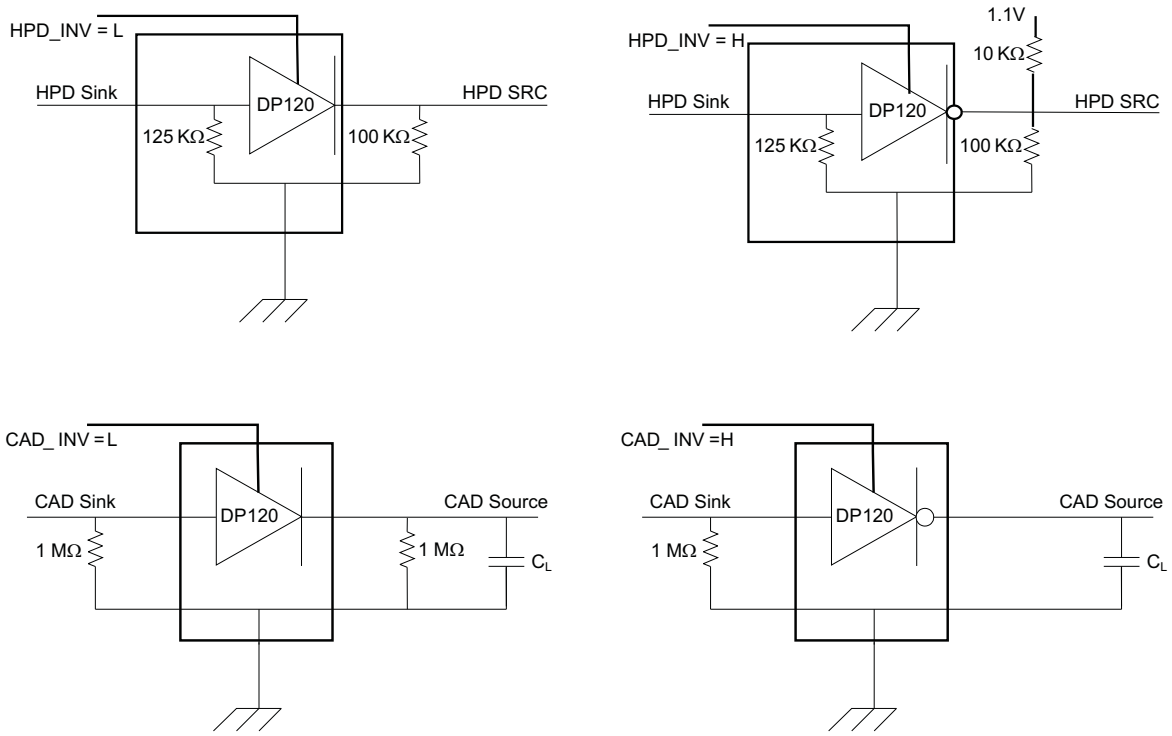


Figure 2. HPD and CAD Test Circuits

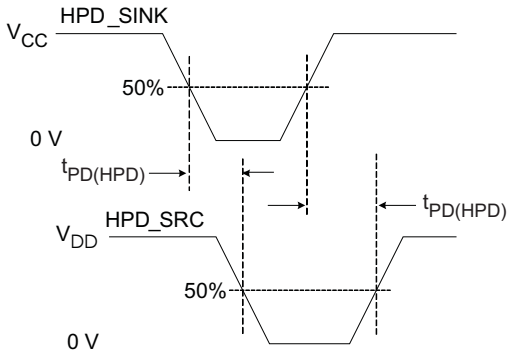


Figure 3. HPD Timing Diagram #1 (HPD_INV = L)

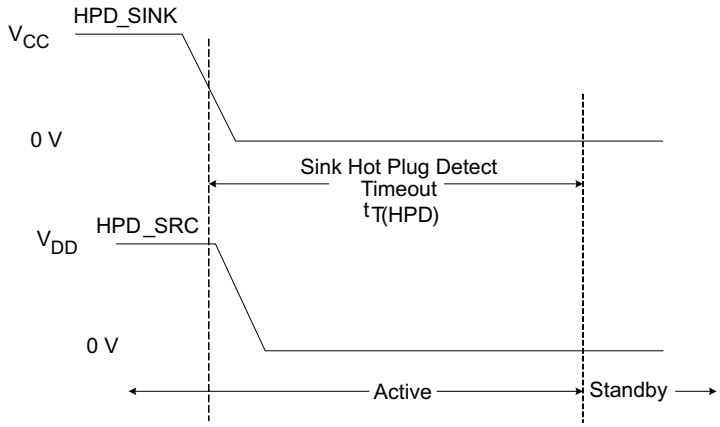


Figure 4. HPD Timing Diagram #2 (HPD_INV = L)

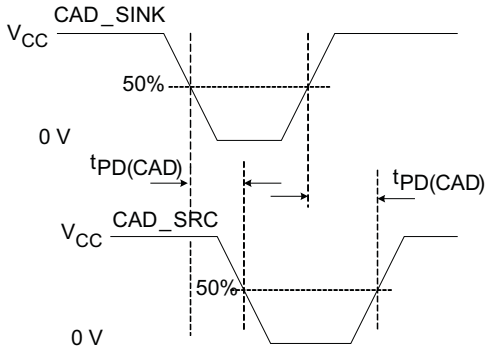


Figure 5. CAD Timing Diagram

DisplayPort Auxiliary Pins

The SN75DP120 is designed to monitor the bidirectional auxiliary signals in DP mode and participates in link training. The SN75DP120 adjusts the output swing, output pre-emphasis, and the EQ setting of every main link port. The SN75DP120 AUX monitor configures the output based on the DPCD addresses below.

The AUX channel is monitored for the Display Port D3 standby command. Upon detecting the D3 command, the SN75DP120 will go into a low power standby state with the AUX activity monitor remaining active.

Table 3. DPCD Lookup Table

ADDRESS	NAME	DESCRIPTION
00100h	LINK_BW_SET	Main Link Bandwidth Setting Bits 7:0 = link bandwidth setting • 06h = 1.62Gbps per lane (default) • 0Ah = 2.7Gbps per lane *Note: Setting the register value in register 0100h to anything else but 0Ah puts the device into 1.62Gbps mode.*
00101h	LANE_COUNT_SET	Determines the number of lanes to be enabled Bits 4:0 = lane count • 1h = one lane • 2h = two lanes • 4h = four lanes *Note: Any other register value in register 0101h bit 4:0 is invalid and disables all OUTx lanes until the register value is changed back to a valid entry. Default all lanes are disabled.*

Table 3. DPCD Lookup Table (continued)

ADDRESS	NAME	DESCRIPTION
00103h	TRAINING_LANE0_SET	Sets the VOD and pre-emphasis levels for lane 0 Bits 1:0 = voltage swing • 00 = voltage swing level 0 (default) • 01 = voltage swing level 1 • 10 = voltage swing level 2 • 11 = voltage swing level 3 Bits 4:3 = pre-emphasis level • 00 = pre-emphasis level 0 (default) • 01 = pre-emphasis level 1 • 10 = pre-emphasis level 2 • 11 = pre-emphasis level 3 *Note: The following combinations of output swing and pre-emphasis are not allowed for register 103h bits [1:0]/[4:3]: 01/11, 10/10, 10/11, 11/01, 11/10, 11/11; setting the DPCD register to any of these invalid combinations disables all OUTx lanes until the register value is changed back to a valid entry.*
00104h	TRAINING_LANE1_SET	Sets the VOD and pre-emphasis levels for lane 1, Same definition as lane 0
00105h	TRAINING_LANE2_SET	Sets the VOD and pre-emphasis levels for lane 2, Same definition as lane 0
00106h	TRAINING_LANE3_SET	Sets the VOD and pre-emphasis levels for lane 3, Same definition as lane 0
00600h	SET_POWER	Sets the power mode of the device Bits 1:0 = Power mode • 01 = Normal mode (default) • 10 = Power down mode (D3 or Standby Mode) When power down mode is selected, the main link and all analog circuits are shut down to minimize power consumption. The AUX channel is still monitored. Upon detecting a D3 exit command or if CAD_SNK goes high, the device exits the power down mode. The device will also exit D3 if HPD_SNK goes low for longer than $t_{T(HPD)}$, which indicates that the DP sink was disconnected. *Note: Setting the register to the invalid combination 0600h[1:0]=00 or 11 is ignored by the device and the device remains in normal mode.*

ELECTRICAL CHARACTERISTICS

over recommended operating (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ID}	Differential input voltage		0.25		1.6	Vp-p
$V_{ID(HYS)}$	Differential input hysteresis			50		mV
I_H	High-level input current		–1		1	µA
I_L	Low-level input current		–1		1	µA
T_{jit}	Maximum allowable UI variation within a single transaction				0.1	UI

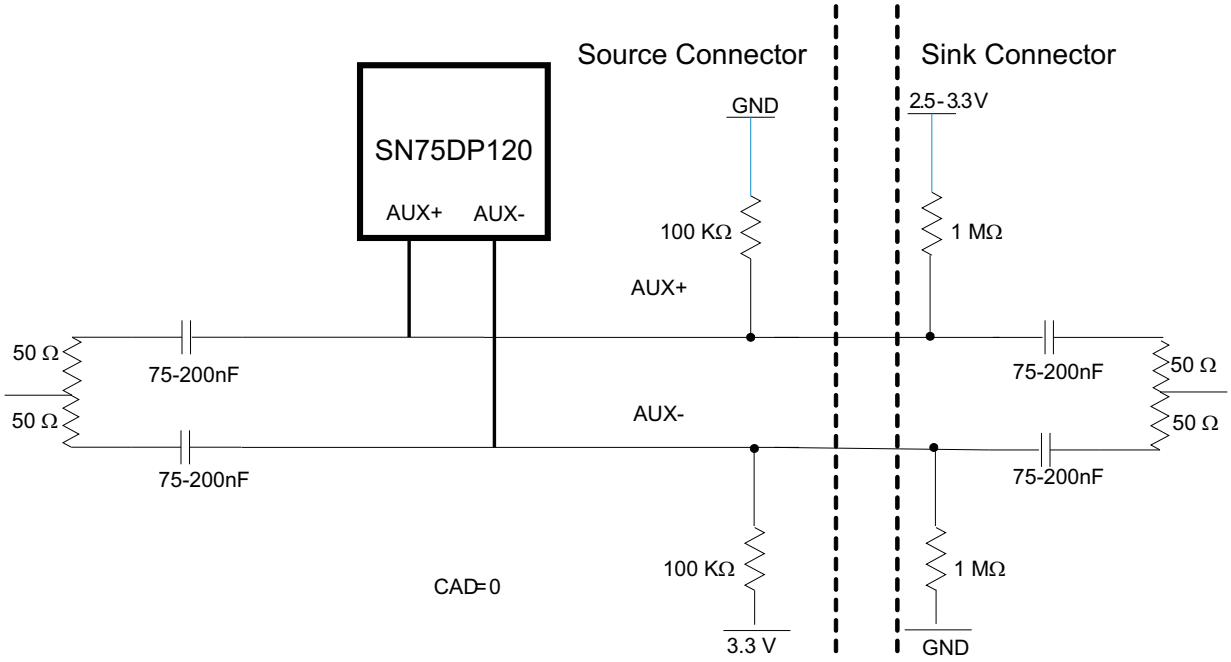


Figure 6. Auxiliary Channel Measurement

DisplayPort Main Link Pins

The SN75DP120 is designed to support DisplayPort's high speed differential main link with four levels of output voltage swing and four levels of pre-emphasis. The main link I/Os of the SN75DP120 are designed to be compliant to the DisplayPort 1.1a specification.

ELECTRICAL CHARACTERISTICS

over recommended operating (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTx (Mainlink Outputs)							
$V_{ODpp(1)}$	Output differential peak-to-peak voltage Level 1	PRBS7 pattern at 1.67 Gbps and 2.7 Gbps, Measured at TP1 in Figure 8			400		mVp-p
$V_{ODpp(2)}$	Output differential peak-to-peak voltage Level 2				600		mVp-p
$V_{ODpp(3)}$	Output differential peak-to-peak voltage Level 3				800		mVp-p
$V_{ODpp(4)}$	Output differential peak-to-peak voltage Level 4				1200		mVp-p
$V_{ODpp(5)}$	Output differential peak-to-peak voltage TMDS mode	CAD_SINK = 3.6V			600		mVp-p
$V_{ODpp(CTS1.1)}$	Output differential peak-to-peak voltage for DP Compliance v1.1	Level 3 (800mVpp), Pattern used is PRBS7, Measured at TP2 in Figure 8, Per Eye Mask Test in CTS1.1	1.67 Gbps	400			mVp-p
			2.7 Gbps	350			
ΔV_{ODpp1}	Output differential peak-to-peak voltage increase from Level 1 to Level 2	Measured at TP2, $\Delta V_{ODppn} = 20*\log(V_{ODpp2(n+1)} / V_{ODpp2(n)})$, Refer to Section 3.2 in DP CTS1.1		1.8	3.3	5.0	dB
ΔV_{ODpp2}	Output differential peak-to-peak voltage increase from Level 2 to Level 3			1.1	2.7	4.1	dB
ΔV_{ODpp3}	Output differential peak-to-peak voltage increase from Level 3 to Level 4			1.8	3.4	5.0	dB

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{PRE(0)}$	Driver output pre-emphasis 0 dB Level	See Figure 3-3 in DP CTS1.1, PRBS7 pattern at 1.67 Gbps and 2.7 Gbps, Measured at TP1	All VOD levels			0	dB
$V_{PRE(1)}$	Driver output pre-emphasis 3.5 dB Level		VOD = VODpp(1), VODpp(2), VODpp(3)		3.5		dB
$V_{PRE(2)}$	Driver output pre-emphasis 6 dB level		VOD = VODpp(1), VODpp(2)		6.0		dB
$V_{PRE(3)}$	Driver output pre-emphasis 9.5 dB level		VOD = VODpp(1)		9.5		dB
$V_{PRE2(0)}$	Driver output pre-emphasis 0dB level	Measured at TP2				0	dB
ΔV_{PRE1}	Pre-emphasis delta	Measured at TP2, At each supported pre-emphasis level: Δ VPREn = VPRE2(n+1) - VPRE2(n)		2.5			dB
ΔV_{PRE2}				1.9			dB
ΔV_{PRE3}				1.9			dB
V_{PRE_NPP}	Pre-emphasis non-transition peak-to-peak voltage range	All supported pre-emphasis levels, Measured at TP2				40	mV-pp
R_{OUT2}	Driver output impedance			40	50	60	Ω
R_{INT}	Input termination impedance			40	50	60	Ω
V_{Iterm}	Input termination voltage			0		2	V
V_{Oterm}	Output common mode voltage			0		2	V
V_{TXACCM}	Output AC common mode voltage	Measured at 1.62Gbps and 2.7Gbps (All output and pre-emphasis levels), Measured at TP2				20	mVrms
$I_{TXSHORT}$	Output short circuit current limit	OUT pins shorted to GND				50	mA
$I_{RXSHORT}$	Input short circuit current limit	IN pins shorted to GND				50	mA

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{R/F(DP)}$	Differential Output edge rate (20%–80%)	No pre-emphasis, 800mV differential swing, Measured at TP1, PRBS7		60		150	ps
$t_{PD(ML)}$	Propagation delay time	d_R = 2.7Gbps, No pre-emphasis, 800 mV differential voltage swing, See Figure 9				450	ps
$t_{SK(1)}$	Output Intra-pair skew	d_R = 2.7Gbps, No pre-emphasis, 800 mV differential voltage swing, PRBS7, See Figure 10				15	ps
$t_{SK(2)}$	Output Inter-pair skew(1)	d_R = 2.7Gbps, No pre-emphasis, 800 mV differential voltage swing, PRBS7				40	ps
$t_{DPJIT1(PP)}$	Peak-to-peak output residual jitter at Pkg Pins	No pre-emphasis, All levels differential voltage swing, PRBS7. Vid = 400 mVpp TTP3-TTP2 in Figure 11	d_R = 2.7 Gbps			10	ps
			d_R = 1.62 Gbps			10	
$t_{DPJIT2(PP)}$	Peak-to-peak output residual jitter	No pre-emphasis, All levels differential voltage swing, PRBS7. Vid = 400 mVpp, TTP4-TTP1 in Figure 11	d_R = 2.7 Gbps			0.08	UI
			d_R = 1.62 Gbps			0.06	
$t_{SK(in)}$	Intra-pair skew at the input package pins	d_R = 2.7 Gbps				100	ps
		d_R = 1.62 Gbps				300	
$T_{TMDSJIT1(PP)}$	Peak-to-peak output residual jitter at Pkg Pins	d_R = 2.25 Gbps, CAD_SINK = H , Input Vid = 600 mVp-p, No pre-emphasis, See Figure 12				10	ps
$T_{TMDSJIT2(PP)}$	Peak-to-peak output residual jitter	d_R = 2.25 Gbps CAD_SINK = H, Input Vid = 600 mVp-p, No pre-emphasis, See Figure 12				0.1	UI

(1) $t_{SK(2)}$ is the magnitude of the time difference between $t_{PD(ML)}$ of any two mainlink outputs on a single device.

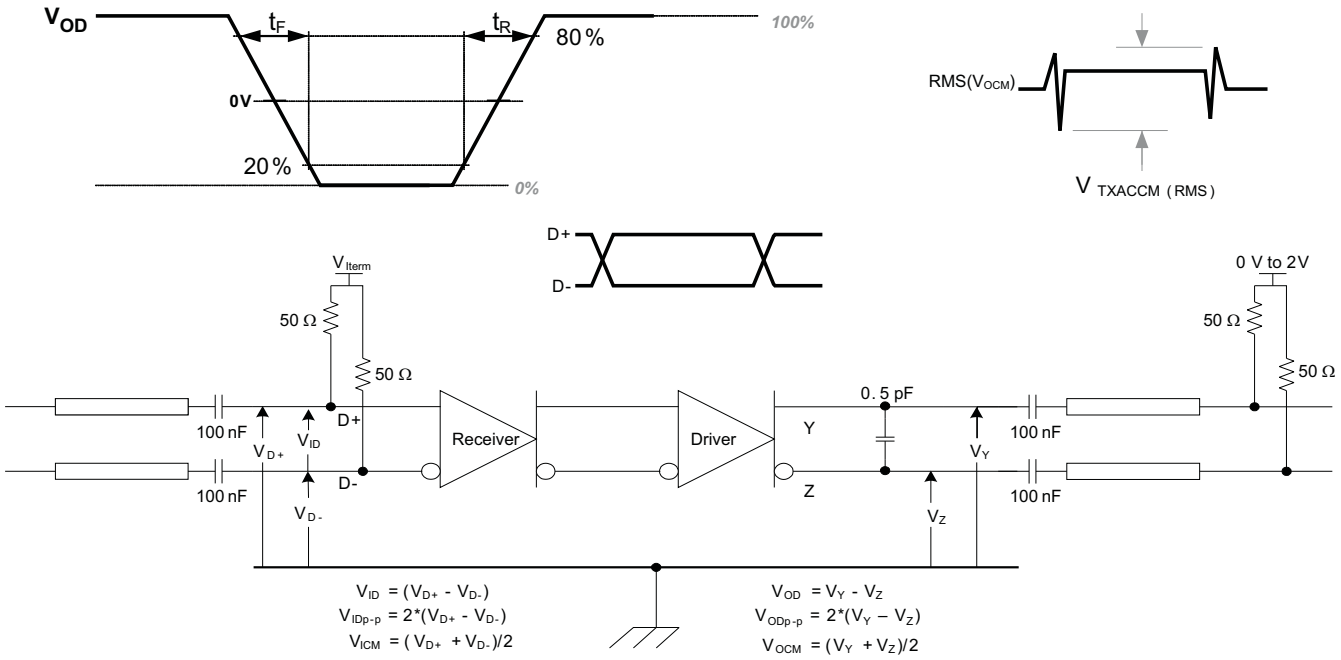


Figure 7. Main Link Test Circuit and Definitions

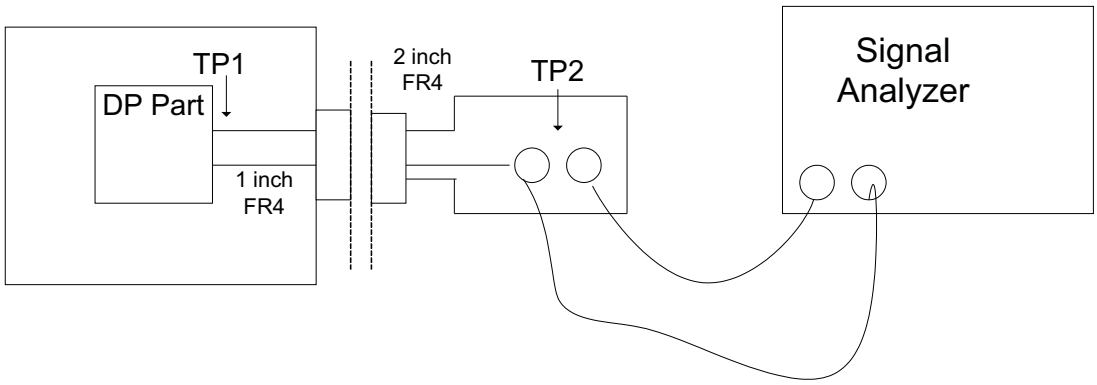


Figure 8. Display Port Compliance Setup

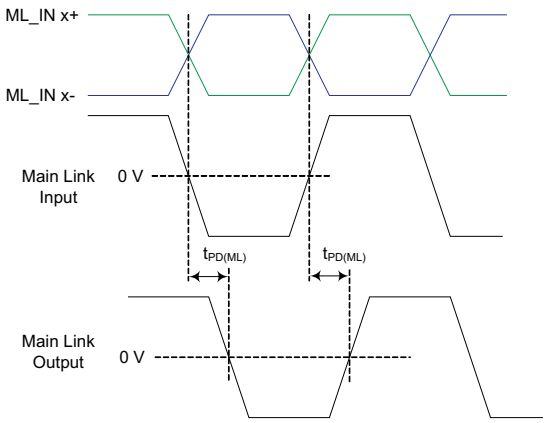
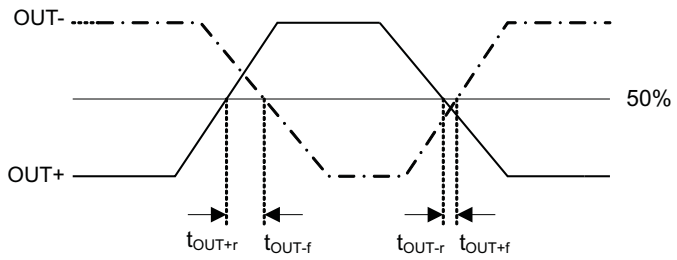
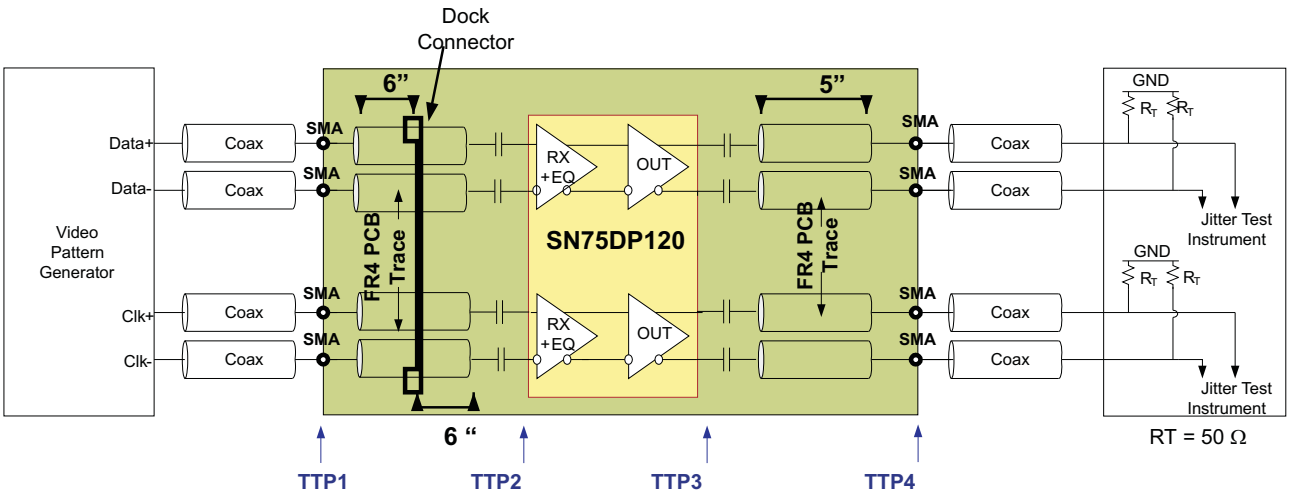


Figure 9. Main Link Delay Measurement



$$t_{sk(1)} = 0.5 * | (t_{OUT+r} - t_{OUT-f}) + (t_{OUT+f} - t_{OUT-r}) |$$

Figure 10. Intra-Pair Skew Measurement

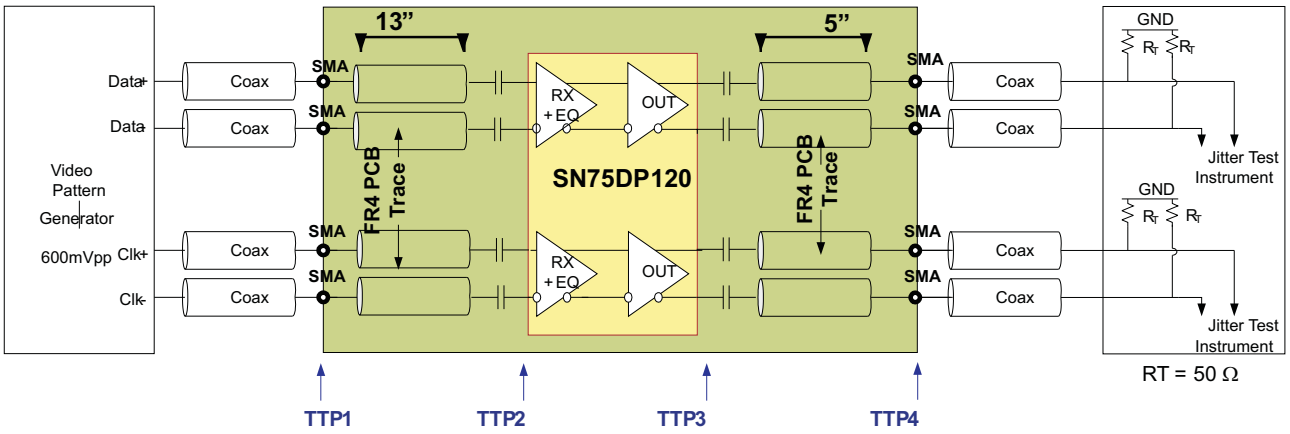


(1) All jitter measured at BER of 10-e9.

(2) Residual jitter reflects the total jitter measured at TTP4 minus the jitter at TTP1.

(3) 5 inches on the output represents 2 inches of trace, plus connector, plus 2 more inches of trace.

Figure 11. Jitter Measurement Setup – DP Mode



(1) All jitter measured at BER of 10-e9.

(2) Residual jitter reflects the total jitter measured at TTP4 minus the jitter at TTP1.

(3) Input trace of 13 inches represents 6 inches trace, connector, and additional 6 inches of trace.

(4) Output trace of 5 inches represents 2 inches of trace, connector, and 2 inches of trace.

(5) Input edge rate from Video Pattern Generator is 50ps (20%–80%) with output level 600mVpp.

(6) CAD_SINK is H and DP120 output levels are set to 600mVp-p level.

Figure 12. Jitter Measurement Setup – TMDS Mode

TYPICAL CHARACTERISTICS

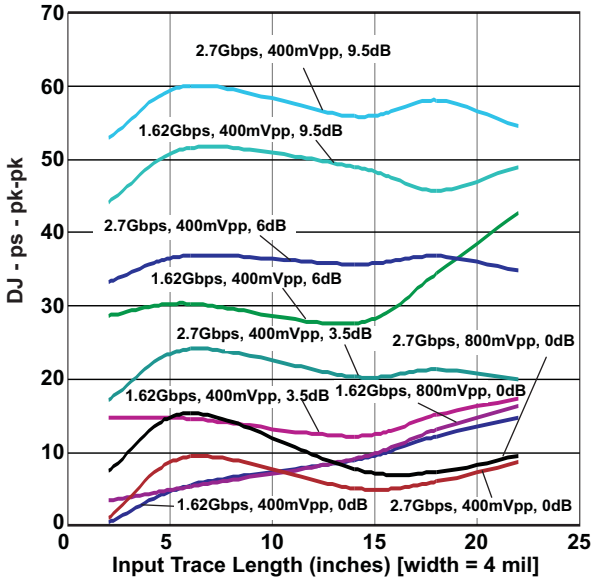


Figure 13. Output Jitter vs Input Trace Length

TYPICAL CHARACTERISTICS (continued)

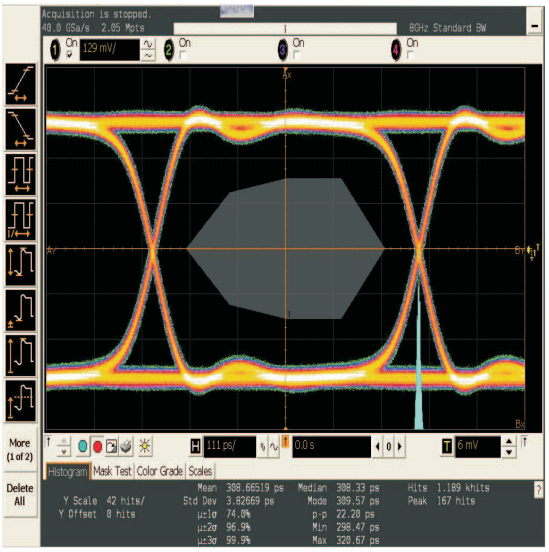


Figure 14. Eye Diagram at TP2 with 22 Inch FR4 Input Trace Output Set at 800mV$_{pp}$, 0dB at RBR (1.62 Gbps), with DP Source Compliance Eyemask

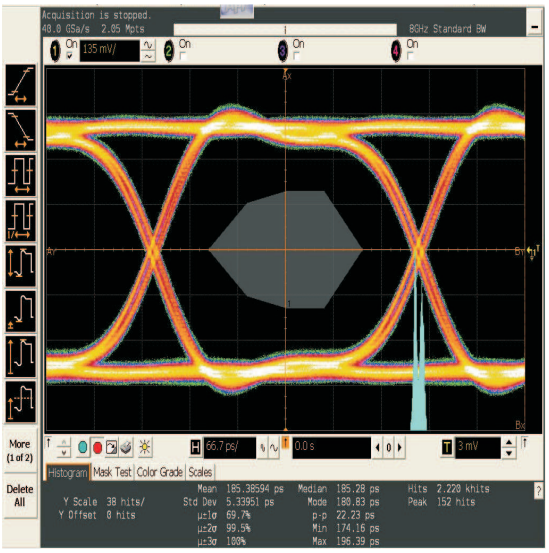


Figure 15. Eye Diagram at TP2 with 22 Inch FR4 Input Trace Output Set at 800mV$_{pp}$, 0dB at HBR (2.7 Gbps), with DP Source Compliance Eyemask

APPLICATION INFORMATION

POWER ON RESET

On power up, the interaction of the LP# pin and power on ramp could result in digital circuits not being set correctly. The device should not be enabled until the power on ramp has settled to 3V or higher to guarantee a correct power on reset of the digital circuitry. If LP# cannot be held low by microcontroller or other circuitry until the power on ramp has settled, then a pullup resistor and external capacitor are required to hold the device in the low power reset state.

To use LP# as a reset pin, the pullup resistor should be connected from VCC to LP# and the capacitor from LP# pin to GND. The RC time constant should be larger than 5 times of the power on ramp time (0 to VCC). The pullup resistor should be less than 100KΩ. The following table shows example of power on ramp time and R and C values.

Table 4. Recommended LP# RC Values

POWER ON RAMP	R	C
100 µs	6 kΩ	0.1 µF
0.5 ms	40 kΩ	0.1 µF
1 ms	100 kΩ	0.1 µF
5 ms	100 kΩ	0.5 µF
10 ms	100 kΩ	1 µF

HPD POWER MANAGEMENT AND INTERRUPT BEHAVIOR

The power management of the SN75DP120 is controlled by the state of the HPD_SINK pin as well as the low power (LP#) pin. When HPD_SINK is LOW for $t_{T(HPD)}$ the SN75DP120 will enter a standby state. In this state main link outputs will be high impedance and shutdown to conserve power. When HPD_SINK goes high the device will enter the normal operational state.

The LP# pin puts the SN75DP120 in its lowest power mode, shutdown, when LP# is low. In this state, almost all circuitry is shutdown with inputs and outputs at high impedance. HPD is still active, however, and HPD_SRC will follow HPD_SINK.

1. HPD and Main Link behavior
   - **Case one:** In this case HPD_SINK is initially LOW and the low power pin is also LOW. In this initial state the device is in a low power mode. Once the HPD input goes to a HIGH state the device will remain in the low power mode with both the main link and auxiliary I/O in a high impedance state. Refer Figure 16. However the HPD_SRC signal is not gated by the LP# pin. HPD_SRC will follow HPD_SINK after the propagation delay $t_{PD(HPD)}$.
   - **Case two:** In this case HPD_SINK is initially LOW and the low power pin is HIGH. In this initial state the device is in a standby mode. Once the HPD input goes to a HIGH state the device will come out of the standby mode and will enter active mode enabling the main link. The HPD output to the source will follow the logic state of the input HPD. See Figure 17, where HPD_INV = L.

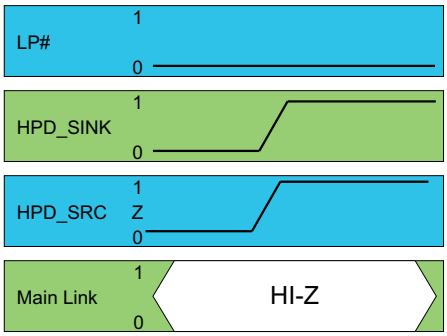


Figure 16.

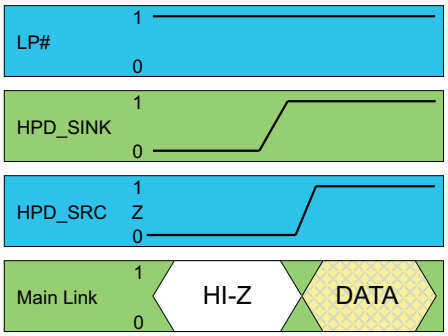


Figure 17.

2. HPD Interrupt and Time Out
   – In this case the HPD_SINK input is initially HIGH. The HPD_SRC output logic state will follow the state of the HPD_SINK input (when HPD_INV = L). If the HPD_SINK input pulses LOW, as may be the case if the Sink device is requesting an interrupt, the HPD_SRC output to the source will also pulse Low for the same duration of time with a slight delay (see Figure 18). The delay of this signal through the SN75DP120 is specified as $t_{PD(HPD)}$. If the duration of the LOW pulse exceeds $t_{T(HPD)}$ the device will assume that an unplug event has occurred and enter the low power state (see Figure 19). Once the HPD_SINK input goes high again the device will return to the active state as indicated in Figure 17.

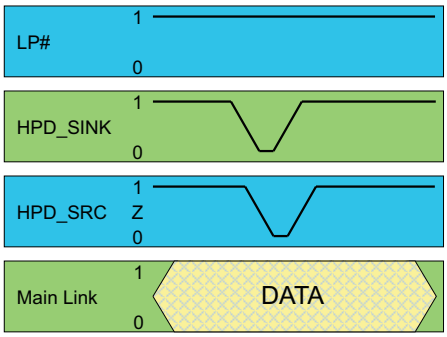


Figure 18.

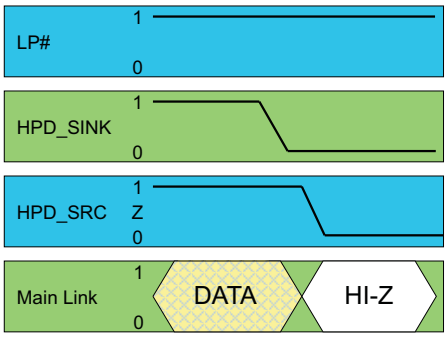


Figure 19.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN75DP120RHHR	ACTIVE	VQFN	RHH	36	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 85	DP120	Samples
SN75DP120RHHT	ACTIVE	VQFN	RHH	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 85	DP120	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

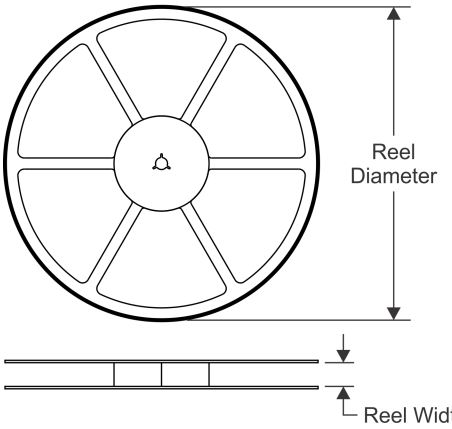
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

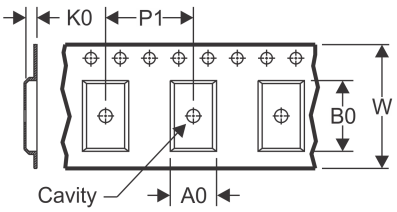
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

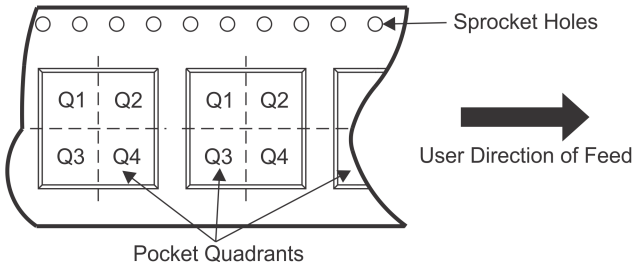


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

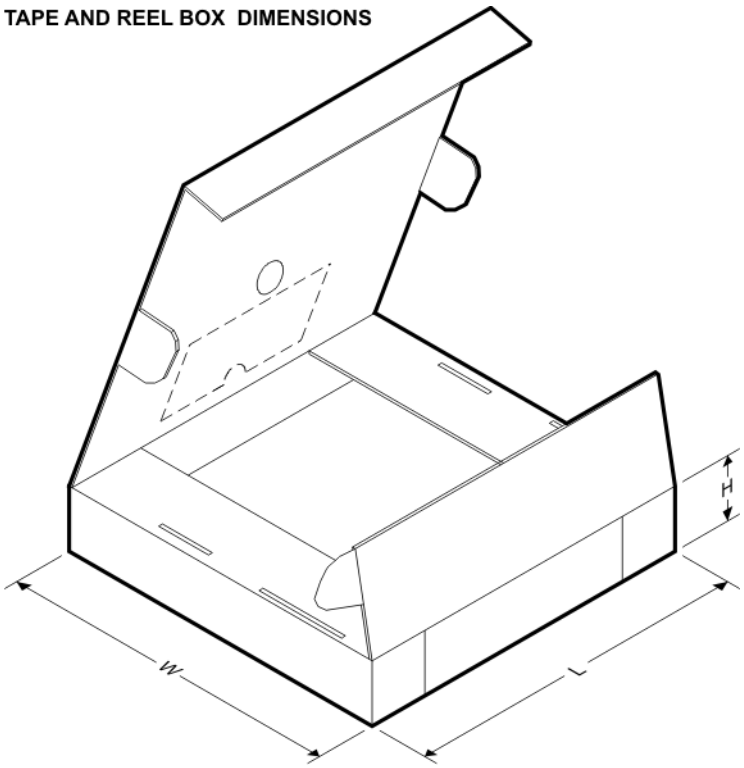
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75DP120RHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
SN75DP120RHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

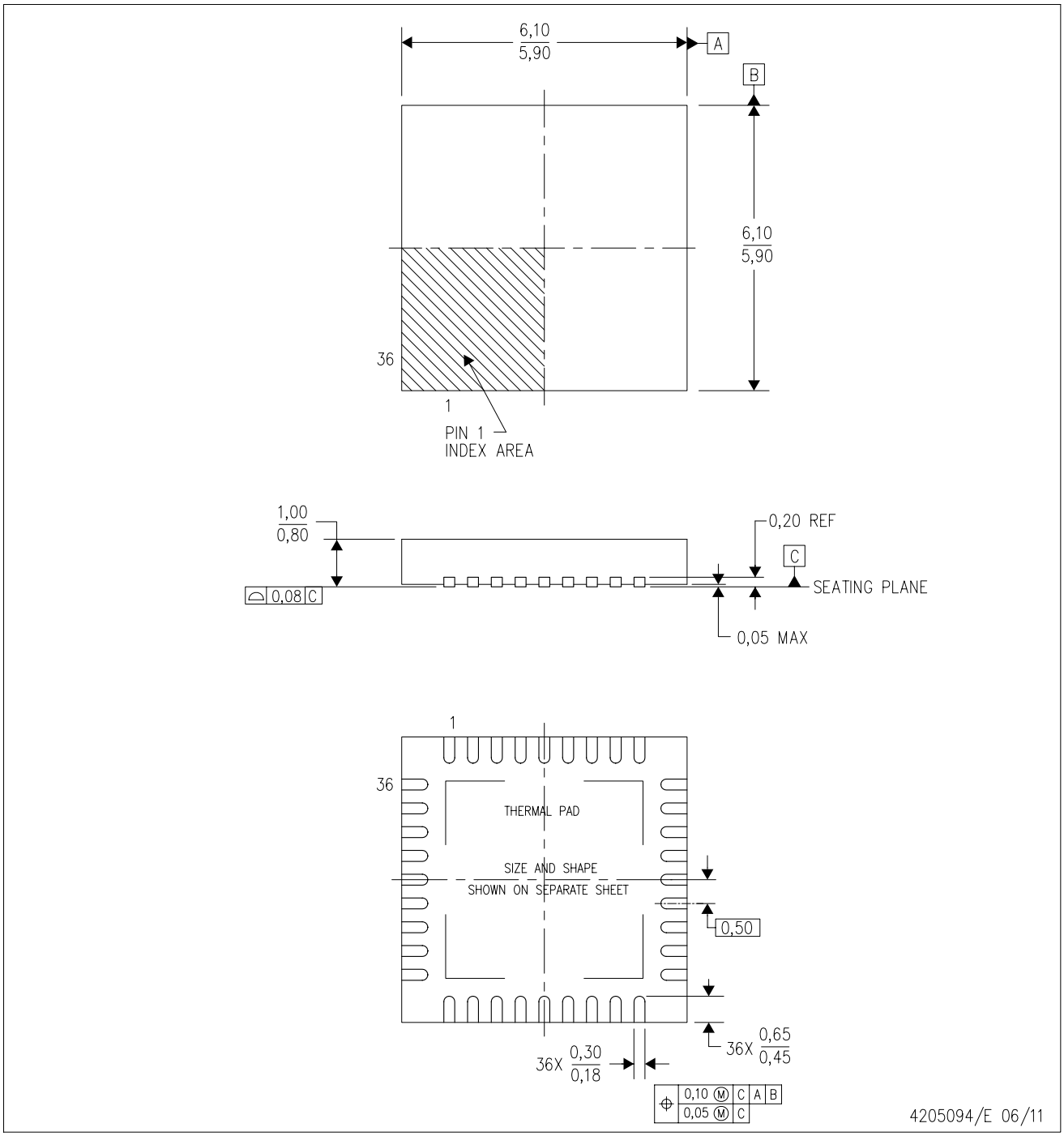
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75DP120RHHR	VQFN	RHH	36	2500	367.0	367.0	38.0
SN75DP120RHHT	VQFN	RHH	36	250	210.0	185.0	35.0

RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

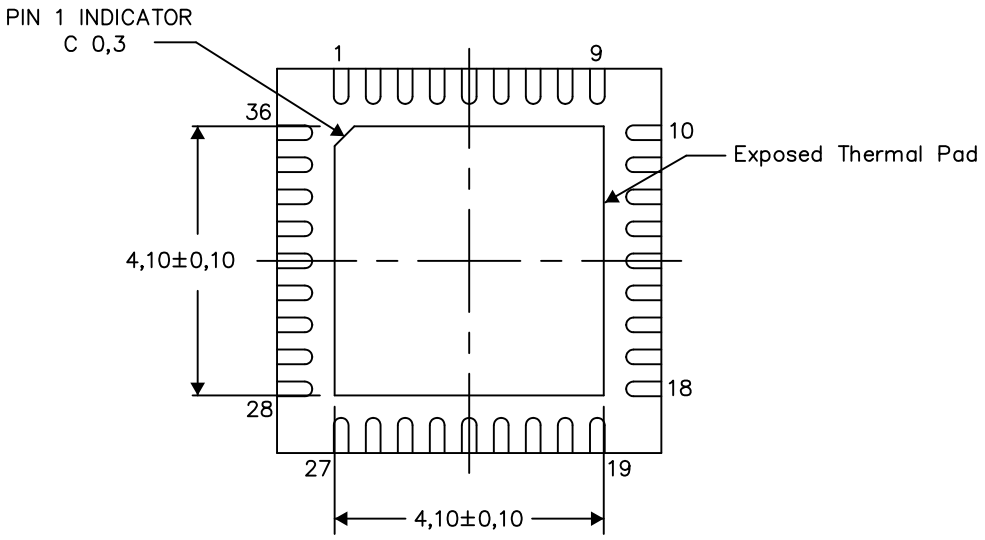
RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



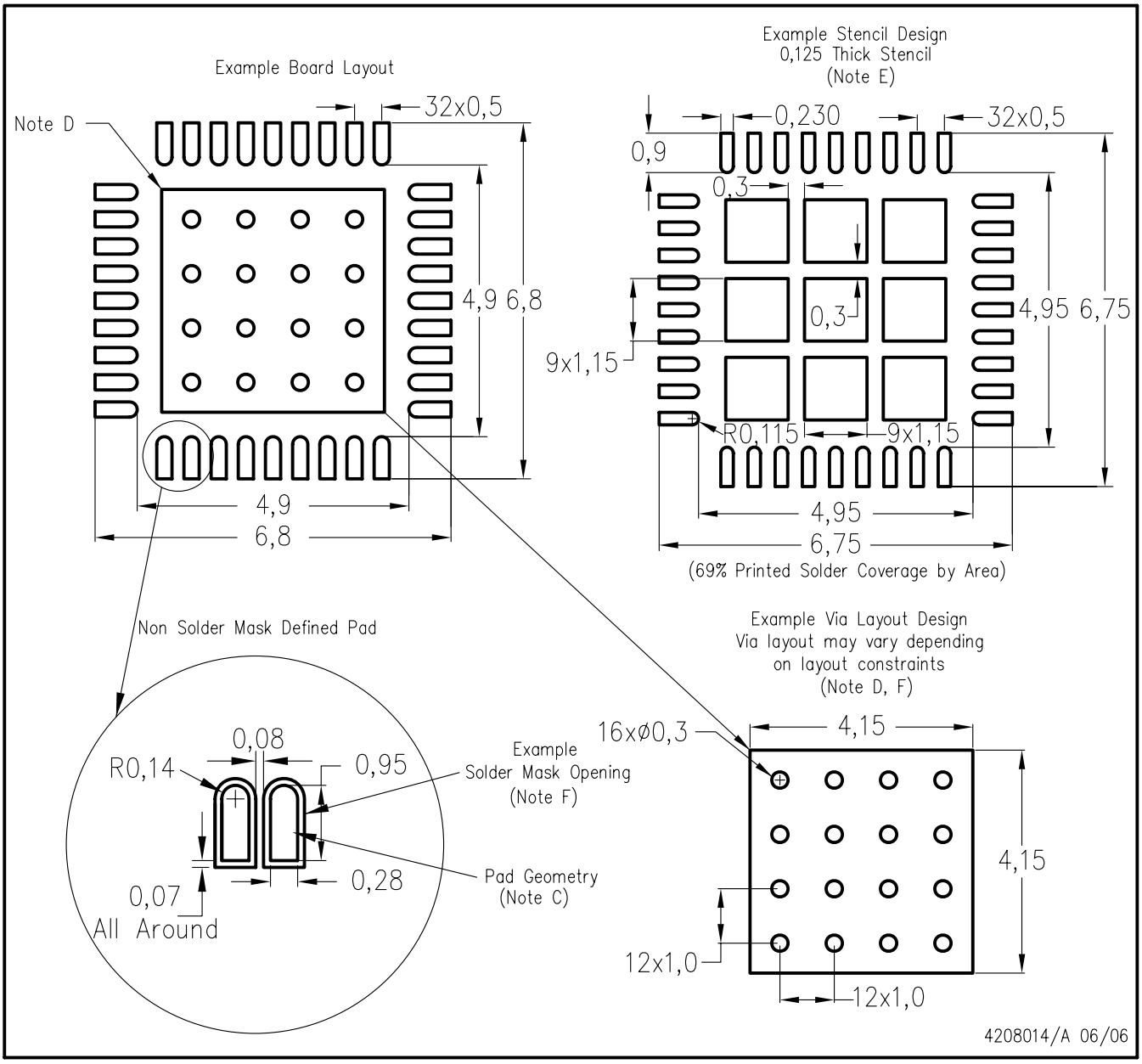
Bottom View

Exposed Thermal Pad Dimensions

4206362–3/L 10/12

NOTE: All linear dimensions are in millimeters

RHH (S–PQFP–N36)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265