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Vishay Siliconix

N-Channel 150 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A)	Q _g (TYP.)			
150	0.0090 at V _{GS} = 10 V	128	63 nC			
150	0.0105 at V _{GS} = 7.5 V	119	63 110			



Ordering Information:

SUM80090E-GE3 (lead (Pb)-free and halogen-free)

FEATURES

- ThunderFET® power MOSFET
- Maximum 175 °C junction temperature
- 100 % Rq and UIS tested
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912



APPLICATIONS

- Power supplies:
 - Uninterruptible power supplies
 - AC/DC switch-mode power supplies
 - Lighting
- Synchronous rectification
- DC/DC converter
- · Motor drive switch
- DC/AC inverter
- · Solar micro inverter

- N-Channel MOSFET
- Class D audio amplifier
- · Battery management

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	LIMIT	UNIT			
Drain-Source Voltage	V _{DS}	150	V			
Gate-Source Voltage	V _{GS}	± 20	v			
Continuous Drain Current /T 150 °C	T _C = 25 °C		128			
Continuous Drain Current (T _J = 150 °C)	T _C = 125 °C	I _D	74	A		
Pulsed Drain Current (t = 100 μs)	I _{DM}	240	^			
Avalanche Current	L = 0.1 mH	I _{AS}	60			
Single Avalanche Energy ^a	L=0.1 mn	E _{AS}	180	mJ		
Mayimum Daway Dissinction 3	T _C = 25 °C	В	375 ^b	W		
Maximum Power Dissipation ^a	T _C = 125 °C	P _D	125 ^b	vv		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +175	°C		

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	LIMIT	UNIT		
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	40	°C/W		
Junction-to-Case (Drain)	R _{thJC}	0.4	C/VV		

Notes

- a. Duty cycle $\leq 1 \%$.
- b. See SOA curve for voltage derating.
- c. When mounted on 1" square PCB (FR4 material).



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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	150	-	-	V	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	2	-	5	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 250	nA	
		$V_{DS} = 150 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1		
Zero Gate Voltage Drain Current	I _{DSS}	V_{DS} = 150 V, V_{GS} = 0 V, T_J = 125 °C	-	-	100	- μA	
		$V_{DS} = 150 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 175 ^{\circ}\text{C}$	-	-	2	mA	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	90	-	-	Α	
Drain Source On State Begisters 2	В	V _{GS} = 10 V, I _D = 30 A	-	0.0075	0.0090	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 7.5 \text{ V}, I_D = 30 \text{ A}$	-	0.0084	0.0105		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 30 A	-	52	-	S	
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 75 V, f = 1 MHz	-	3425	-	pF	
Output Capacitance	C _{oss}		-	535	-		
Reverse Transfer Capacitance	C _{rss}		-	26	-		
Total Gate Charge ^c	Qg		-	63	95		
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 60 \text{ A}$	-	19.5	-	nC	
Gate-Drain Charge ^c	Q_{gd}		-	20.5	-		
Gate Resistance	R_g	f = 1 MHz	1.5	3	5	Ω	
Turn-On Delay Time ^c	t _{d(on)}		-	15	30		
Rise Time ^c	t _r	$V_{DD} = 75 \text{ V}, R_L = 1.25 \Omega$	-	114	220		
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong 60 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	28	56	ns	
Fall Time ^c	t _f		-	8	16		
Drain-Source Body Diode Ratings ar	nd Characteris	stics ^b (T _C = 25 °C)					
Pulsed Current (t = 100 μs)	I _{SM}		-	-	240	Α	
Forward Voltage ^a	V _{SD}	I _F = 30 A, V _{GS} = 0 V	-	0.73	1.2	٧	
Reverse Recovery Time	t _{rr}		-	110	220	ns	
Peak Reverse Recovery Charge	I _{RM(REC)}	$I_F = 30 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$	-	10	20	Α	
Reverse Recovery Charge	Q _{rr}	7		0.5	1	μC	

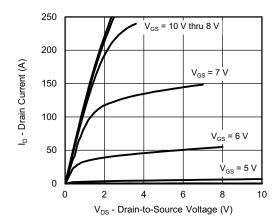
Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

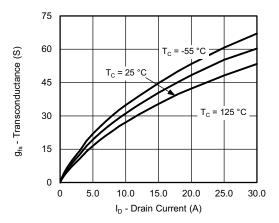
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



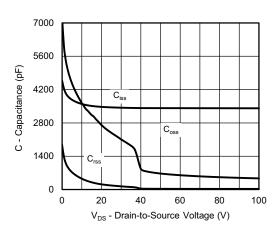
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



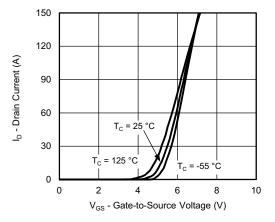
Output Characteristics



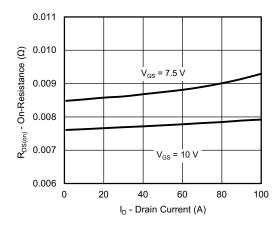
Transconductance



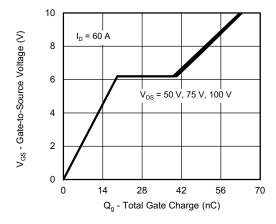
Capacitance



Transfer Characteristics



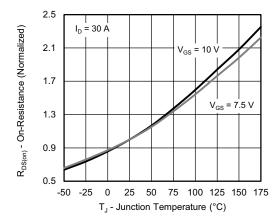
On-Resistance vs. Drain Current



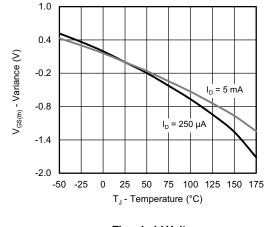
Gate Charge



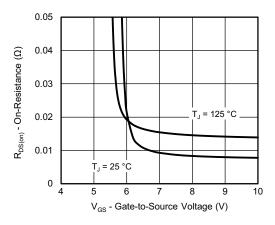
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



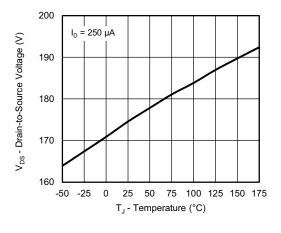
On-Resistance vs. Junction Temperature



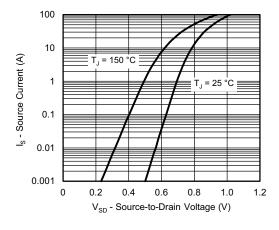
Threshold Voltage



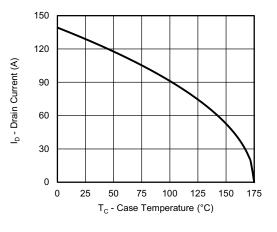
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature



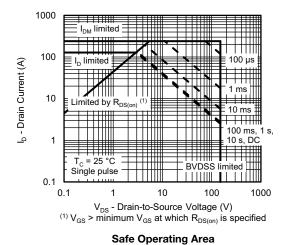
Source Drain Diode Forward Voltage

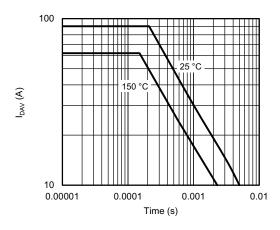


Current De-Rating

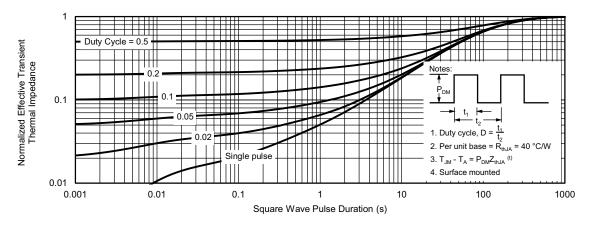


THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)





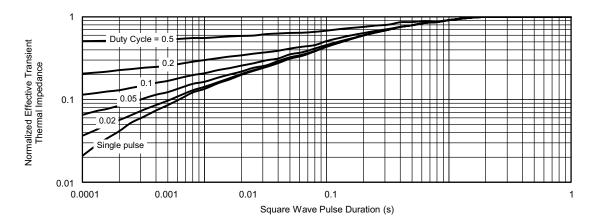
I_{DAV} vs. Time



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction to Ambient (25 °C)

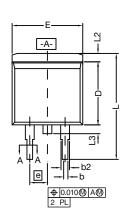
can widely vary depending on actual application parameters and operating conditions.

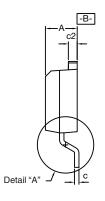
- Normalized Transient Thermal Impedance Junction to Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities

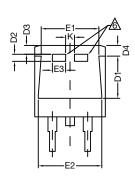
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?64434.



TO-263 (D²PAK): 3-LEAD

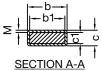








DETAIL A (ROTATED 90°)



_ - b1 , , ,	
≥ 	- -

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. *: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

6. This feature is for thick lead.

DIM.		INC	HES	MILLIMETERS		
		MIN.	MAX.	MIN.	MAX.	
Α		0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457	
C	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
D2		0.038	0.042	0.965	1.067	
D3		0.045	0.055	1.143	1.397	
	D4	0.044	0.052	1.118	1.321	
E		0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	=	
	E2	0.355	0.375	9.017	9.525	
	E3	0.072	0.078	1.829	1.981	
е		0.100) BSC	BSC 2.54 BSC		
K		0.045	0.055	1.143	1.397	
L		0.575	0.625	14.605	15.875	
L1		0.090	0.110	2.286	2.794	
L2		0.040	0.055	1.016	1.397	
L3		0.050	0.070	1.270	1.778	
	L4	0.010) BSC	0.254	4 BSC	
	М	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13						

DWG: 5843





RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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