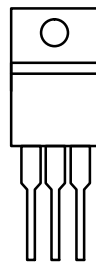


## N-Channel 100 V (D-S) MOSFET

### PRODUCT SUMMARY

V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
100	0.010 at V <sub>GS</sub> = 10 V	85 <sup>d</sup>	77

**TO-220AB**


G D S

Top View

**Ordering Information:**

SUP85N10-10P-GE3 (Lead (Pb)-free and Halogen-free)

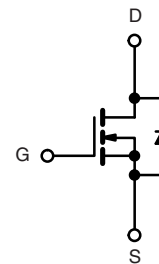
### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> and UIS Tested
- Compliant to RoHS Directive 2002/95/EC


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**

### APPLICATIONS

- Industrial



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	100	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 175 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	85 <sup>d</sup>
		T <sub>C</sub> = 70 °C	83
Pulsed Drain Current	I <sub>DM</sub>	240	A
Avalanche Current	I <sub>AS</sub>	60	
Single Avalanche Energy <sup>a</sup>	E <sub>AS</sub>	180	mJ
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>C</sub> = 25 °C	227 <sup>b</sup>
		T <sub>A</sub> = 25 °C <sup>c</sup>	3.75
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) <sup>c</sup>	R <sub>thJA</sub>	40	°C/W
Junction-to-Case (Drain)	R <sub>thJC</sub>	0.55	

Notes:

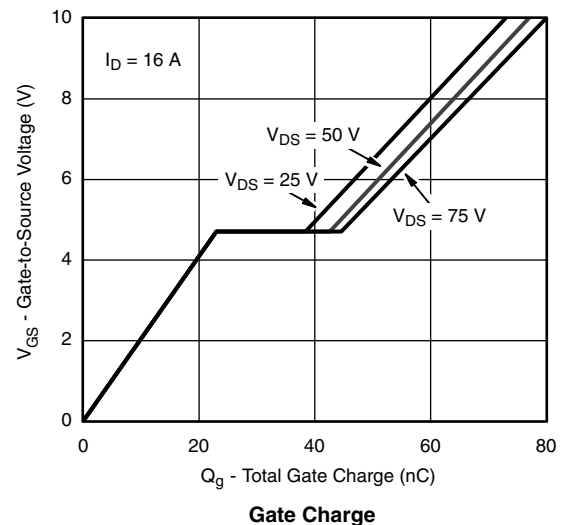
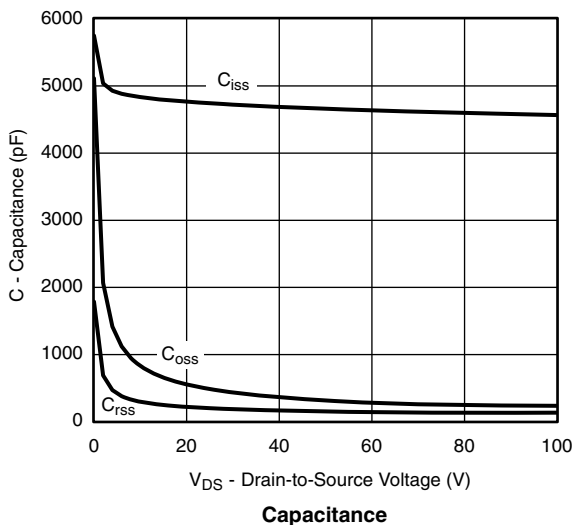
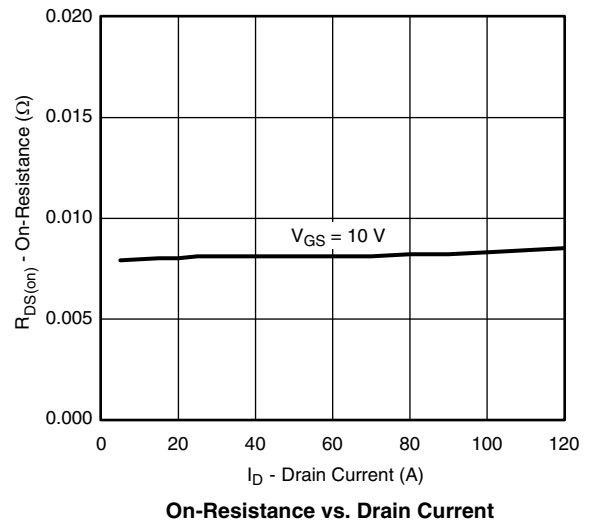
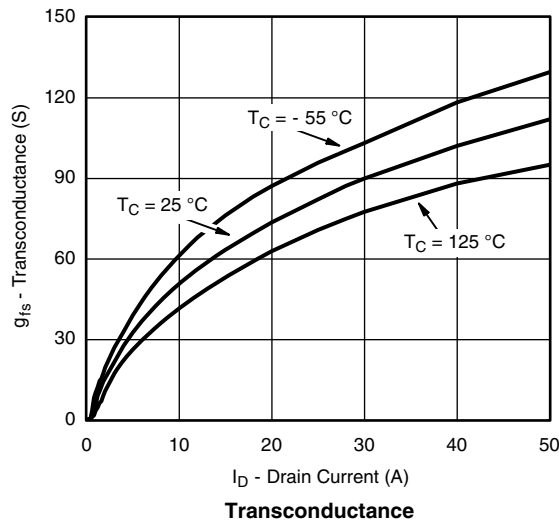
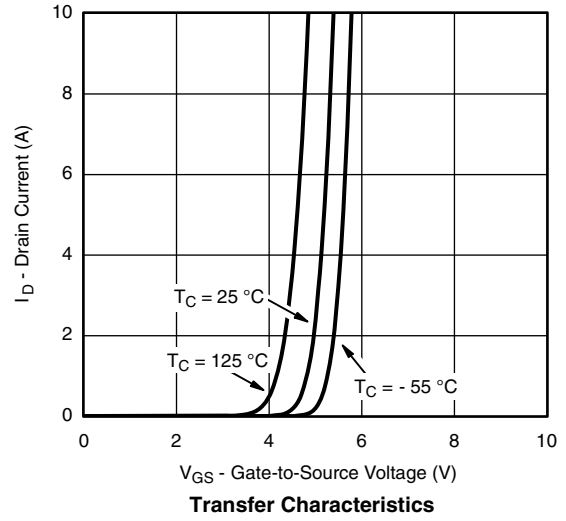
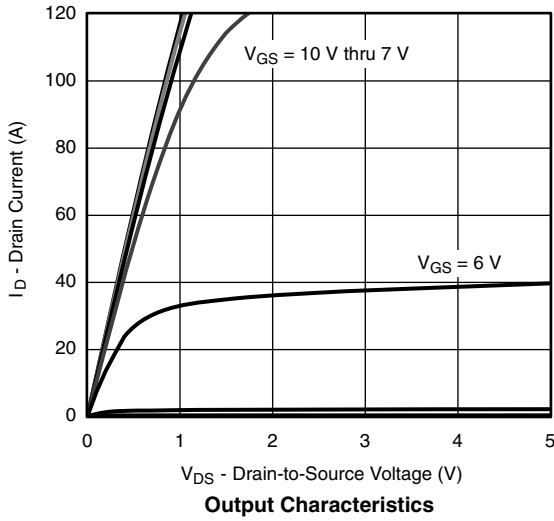
- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).
- Package limited.

<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{DS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.5		4.5	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 250$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$			250	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 10\text{ V}, V_{GS} = 10\text{ V}$	120			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0080	0.0100	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$		0.0146	0.0185	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		70		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}, f = 1\text{ MHz}$		4660		$\mu\text{F}$
Output Capacitance	$C_{oss}$			315		
Reverse Transfer Capacitance	$C_{rss}$			150		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_D = 75\text{ A}$		77	120	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			25		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			20		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	0.25	1.2	2.4	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 0.67\text{ }\Omega$ $I_D \cong 75\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		15	25	ns
Rise Time <sup>c</sup>	$t_r$			12	20	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			25	40	
Fall Time <sup>c</sup>	$t_f$			8	15	
<b>Drain-Source Body Diode Characteristics <math>T_C = 25\text{ }^\circ\text{C}</math><sup>b</sup></b>						
Continuous Current	$I_S$				85	A
Pulsed Current	$I_{SM}$				240	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = 5\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = 5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		74	115	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			6.7	10	A
Reverse Recovery Charge	$Q_{rr}$				250	400

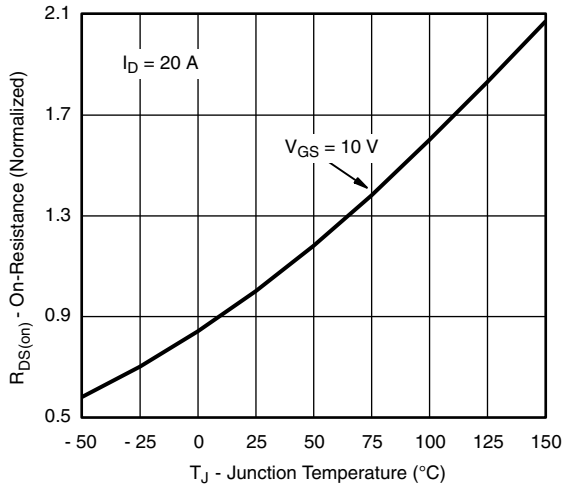
Notes:

- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

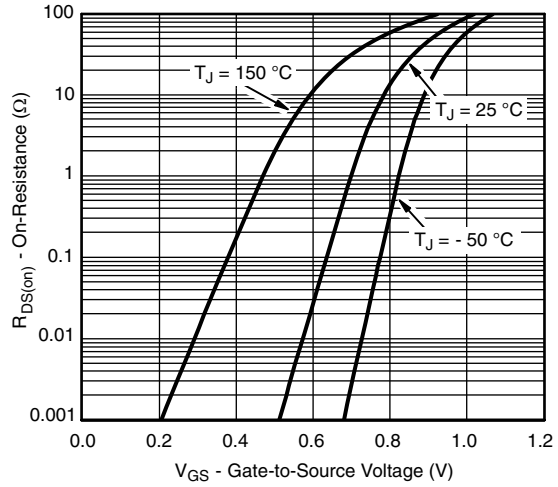
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)


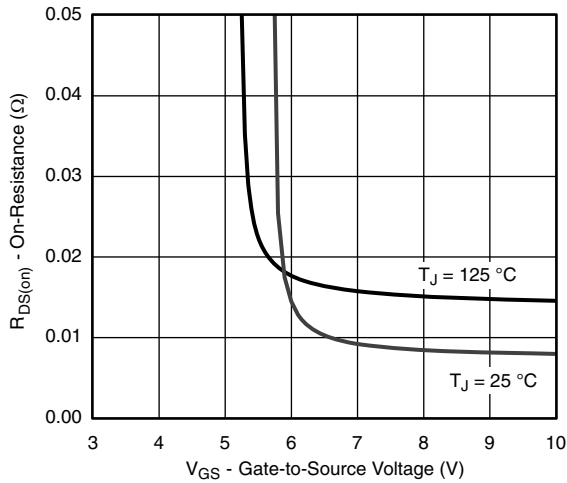
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



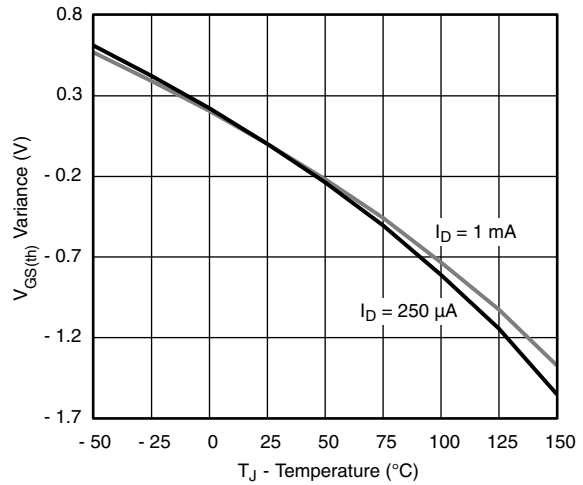
**On-Resistance vs. Junction Temperature**



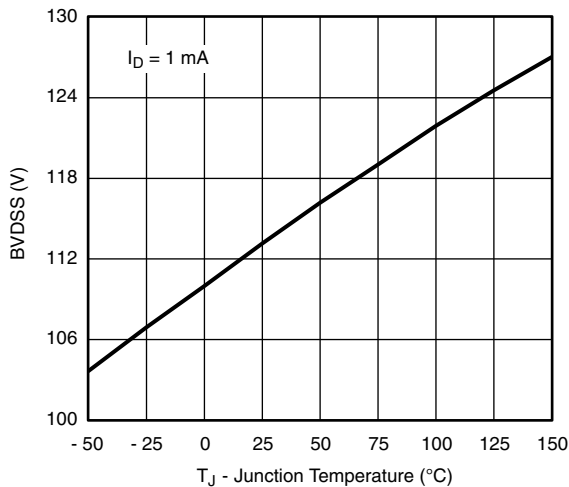
**Source-Drain Diode Forward Voltage**



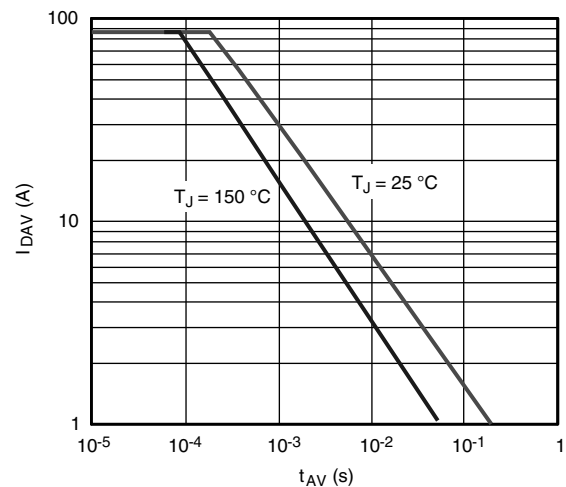
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**

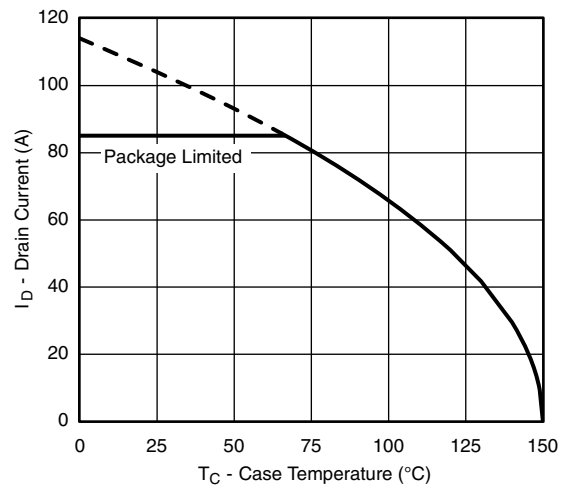
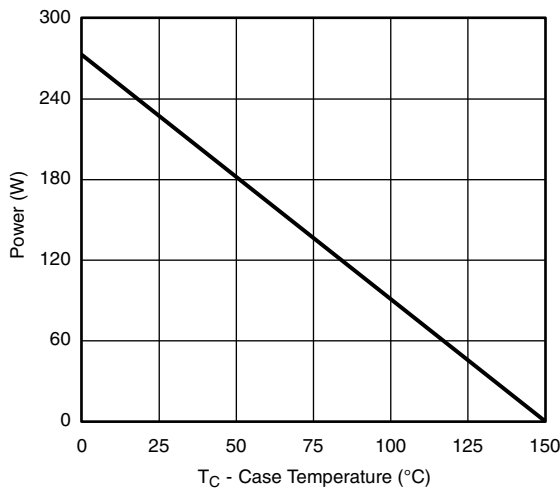
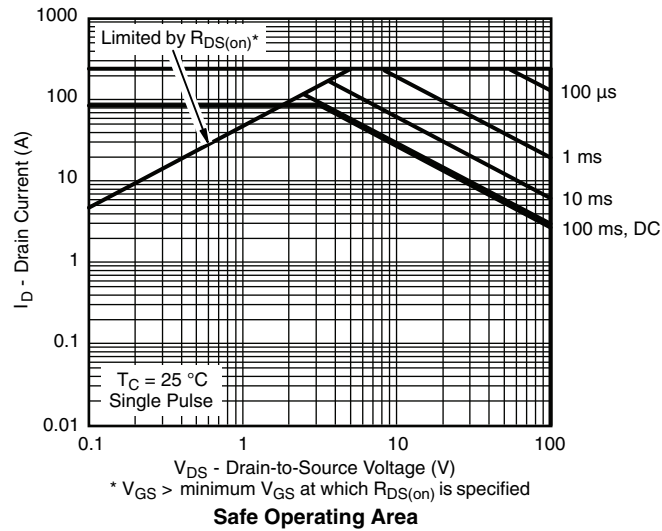


**Drain Source Breakdown Voltage vs. Junction Temperature**



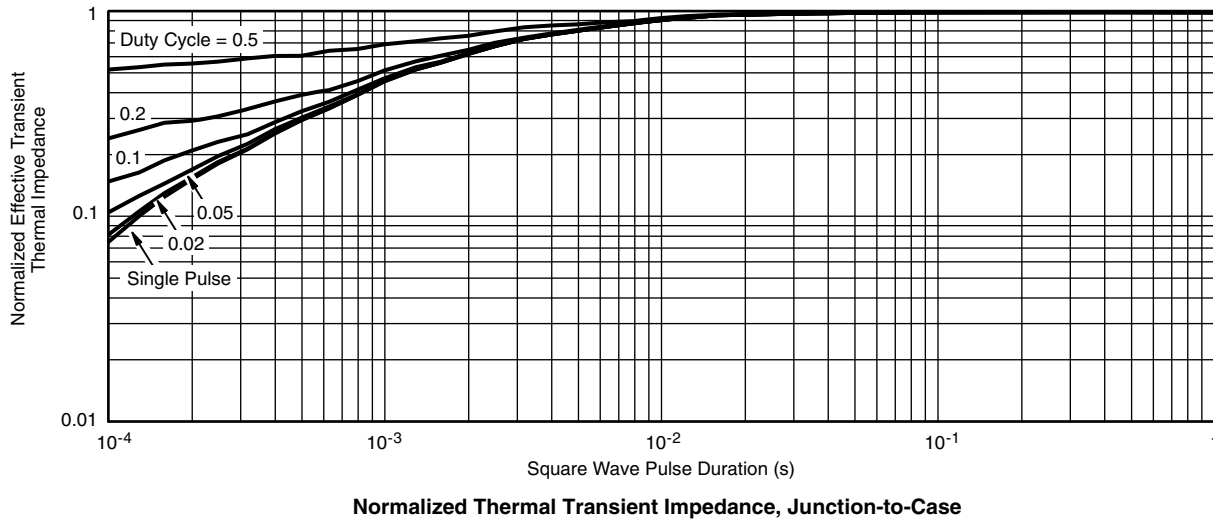
**Single Pulse Avalanche Current Capability vs. Time**

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150\text{ }^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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