100-W STEREO DIGITAL AMPLIFIER POWER STAGE CONTROLLER

FEATURES

- Stereo H-Bridge Controller
- Efficiency > 95%†
- 2x100 W (RMS) at 6 Ω (BTL)†
- THD+N < 0.15% (Typical at 100 W at 6 Ω, 1 kHz)‡
- Half-Bridge Independent Control
- Glueless Interface to TAS50XX Digital Audio PWM Processors
- 3.3-V Digital Interface
- Fault Detection
  - Overcurrent
  - Overtemperature
  - Undervoltage Protection for External MOSFETs
- Low Profile 56-Terminal TSSOP SMD Package

APPLICATIONS

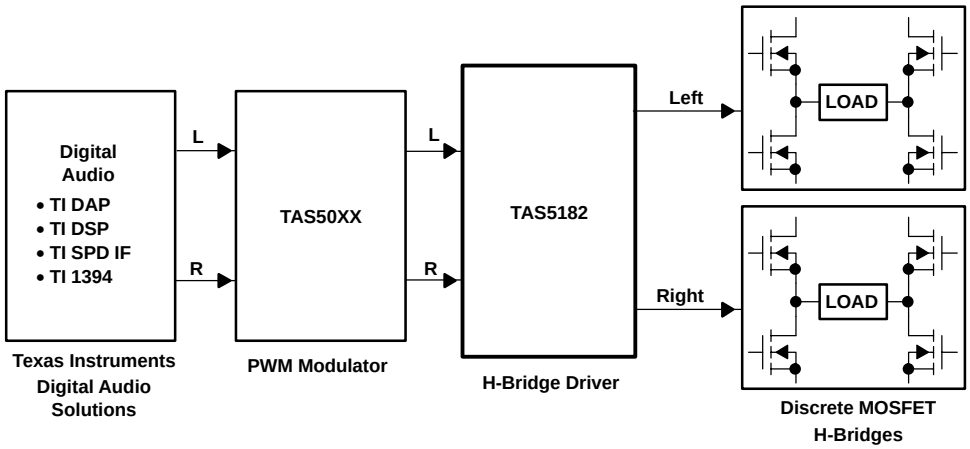
- AV Receivers
- High Power DVD Receivers
- Power Amplifiers
- Home Theater
- Subwoofer Driver

DESCRIPTION

The TAS5182 device is a high-performance, stereo digital amplifier power stage controller. It is designed to drive two discrete bridge-tied-load (BTL) MOSFET output stages at up to 100 W per channel at 6 Ω. The TAS5182 device, incorporating Texas Instrument's PurePath™ technology, is used in conjunction with a digital audio PWM processor (TAS50XX) and two discrete MOSFET H-bridges (4 MOSFETs per H-Bridge) to deliver high-power, true digital audio amplification. The efficiency of this digital amplifier can be greater than 95%, reducing the size of both the power supplies and heat sinks needed. The TAS5182 device accepts a stereo PWM 3.3-V input, and it controls the switching of the discrete H-bridges.

Overcurrent, overtemperature, and undervoltage protections are built into the TAS5182 device, safeguarding the H-bridge and speakers against output short-circuit conditions, overtemperature conditions, and other fault conditions that could damage the system.

Typical Stereo Audio System Using TAS5182 H-Bridge Driver



† When using appropriate MOSFETs.

‡ When using recommended design.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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ORDERING INFORMATION

T_A	PACKAGE
0°C to 70°C	TAS5182DCA
-40°C to 85°C	TAS5182IDCA

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (T_A) unless otherwise noted(1)

		TAS5182
Supply voltage range	GV_{DD} to GV_{SS}	-0.3 V to 15 V
	DV_{DD} to DV_{SS}	-0.3 V to 3.6 V
AP, AM, BP, BM, CP, CM, DP, DM		-0.3 V to DV_{DD} + 0.3 V
$\overline{\text{RESET}}$, $\overline{\text{SHUTDOWN}}$		-0.3 V to DV_{DD} + 0.3 V
BST_A, BST_B, BST_C, BST_D to GV_{SS} for pulse width <100 ns		63 V
Switching frequency		1500 kHz
Operating junction temperature range, T_J		150°C
Storage temperature range, T_{stg}		-65°C to 150°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage range	GV_{DD} to GV_{SS}	9	12	12.6	V
	DV_{DD} to DV_{SS}	3	3.3	3.6	V
High-side bootstrap supply voltage range	BST_A, BST_B, BST_C, BST_D		50	52.6	V
High-side drain connection voltage range	DHS_A, DHS_B, DHS_C, DHS_D		40	42	V
High-side source connection voltage range	SHS_A, SHS_B, SHS_C, SHS_D		40	42	V

ELECTRICAL CHARACTERISTICS

T_C = 25°C, DV_{DD} = 3.3 V, GV_{DD} = 12 V, Frequency = 384 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT TERMINALS: AM, AP, BM, BP, CM, CP, DM, DP						
V_{IH}	High input voltage		2			V
V_{IL}	Low input voltage				0.8	V
R_I	Input resistance			50		kΩ
R_{dtp}	Dead time resistor range		0		100	kΩ
INPUT TERMINAL: RESET_X						
$V_{IH(RESET)}$	High input voltage		2			V
$V_{IL(RESET)}$	Low input voltage				0.8	V
GATE DRIVE OUTPUT: GHS_A, GHS_B, GHS_C, GHS_D, GLS_A, GLS_B, GLS_C, GLS_D						
I_{oso}	Source current, peak	V_O = 2 V		-1.2		A
I_{osi}	Sink current, peak	V_O = 8 V		1.6		A
BST DIODE						
V_d	Forward current voltage drop	I_d = 100 mA		2		V
SUPPLY CURRENTS						
I_{DVDD}	Operating supply current	No load on gate drive output		3		mA
I_{DVDDQ}	Quiescent supply current	No switching		3		mA
I_{GVDD}	Operating supply current	No load on gate drive output		15		mA
I_{GVDDQ}	Quiescent supply current	No switching		2		mA
VOLTAGE PROTECTION						
$V_{uvp,G}$	Undervoltage protection limit, GV_{DD}				8.3	V

SWITCHING CHARACTERISTICS

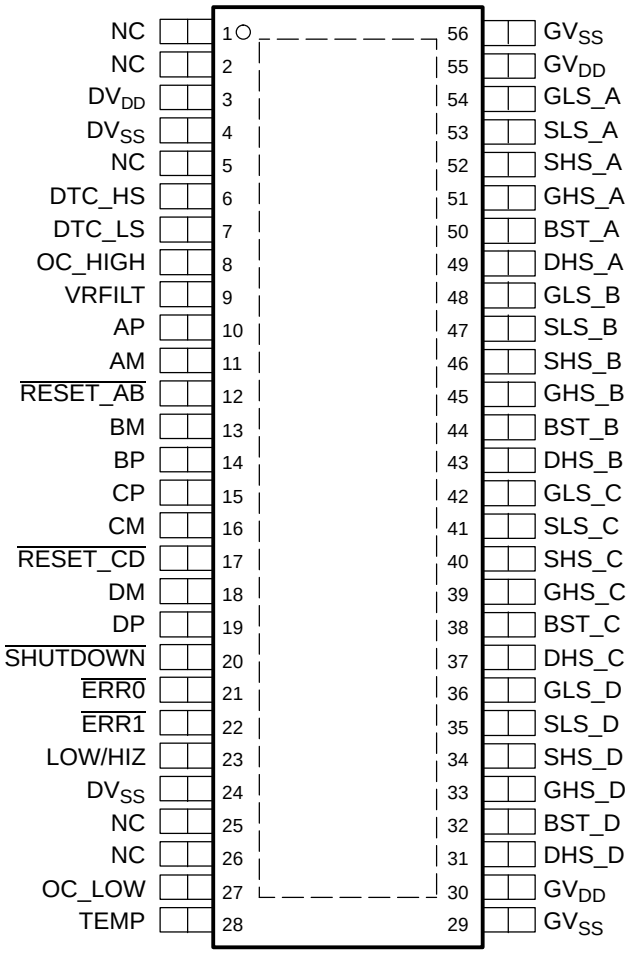
T_C = 25°C, DV_{DD} = 3.3 V, GV_{DD} = 12 V

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
TIMING, OUTPUT TERMINALS						
f_{op}	Operating frequency				1500	kHz
$t_{pd(if-O)}$	Positive input falling to GHS_x falling	C_L = 1 nF		45		ns
$t_{pd(ir-O)}$	Positive input rising to GLS_x falling	C_L = 1 nF		45		ns
t_{dtp}	Dead time programming range(1)	R_{dfp} = 100 kΩ			110	ns
$t_{r(GD)}$	Rise time, gate drive output (0.5 to 3 V)	C_L = 1 nF		4.5		ns
$t_{f(GD)}$	Fall time, gate drive output (9 to 3 V)	C_L = 1 nF		7		ns
TIMING, PROTECTION, AND CONTROL						
$t_{pd(R-SD)}$	Delay, $\overline{\text{RESET}}$ low to $\overline{\text{SHUTDOWN}}$ high			40		ns
$t_{pd(R-LH)}$	Delay, $\overline{\text{RESET}}$ low to GLS_x high			44		ns
$t_{pd(R-OP)}$	Delay, $\overline{\text{RESET}}$ high to operation state			50		ns
$t_{pd(E-L)}$	Delay, error event to all gates low			180		ns
$t_{pd(E-SD)}$	Delay, error event to $\overline{\text{SHUTDOWN}}$ low			170		ns

(1) Dead time programming definition: Adjustable delay from AP (BP, CP, or DP) rising edge to GHS_A (GHS_B, GHS_C, or GHS_D) rising edge, and AM (BM, CM, or DM) rising edge to GLS_A (GLS_B, GLS_C, or GLS_D) rising edge.

PIN ASSIGNMENTS

DCA PACKAGE
(TOP VIEW)



NC - No internal connection
Exposed pad size is 106 x 204 mils

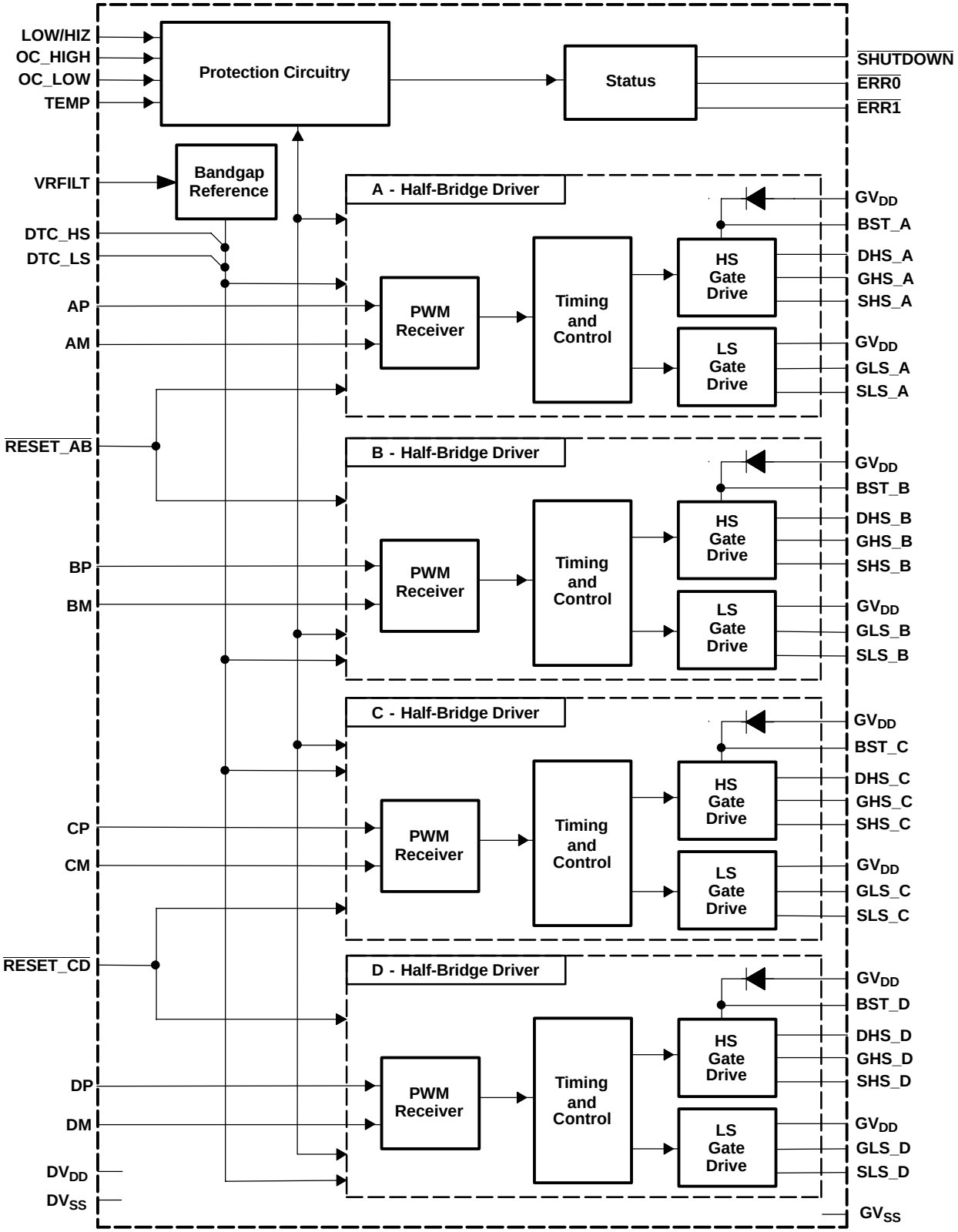
Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AM	11	I	PWM input signal (negative), half-bridge A
AP	10	I	PWM input signal (positive), half-bridge A
BM	13	I	PWM input signal (negative), half-bridge B
BP	14	I	PWM input signal (positive), half-bridge B
BST_A	50	I	High-side bootstrap supply (BST), external capacitor to SHS_A required
BST_B	44	I	High-side bootstrap supply (BST), external capacitor to SHS_B required
BST_C	38	I	High-side bootstrap supply (BST), external capacitor to SHS_C required
BST_D	32	I	High-side bootstrap supply (BST), external capacitor to SHS_D required
CM	16	I	PWM input signal (negative), half-bridge C
CP	15	I	PWM input signal (positive), half-bridge C
DM	18	I	PWM input signal (negative), half-bridge D
DP	19	I	PWM input signal (positive), half-bridge D

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DHS_A	49	I	High-side drain connection, used for high-side V_{DS} sensing
DHS_B	43	I	High-side drain connection, used for high-side V_{DS} sensing
DHS_C	37	I	High-side drain connection, used for high-side V_{DS} sensing
DHS_D	31	I	High-side drain connection, used for high-side V_{DS} sensing
DTC_HS	6	I	High-side dead-time programming, external resistor to DV_{SS} required
DTC_LS	7	I	Low-side dead-time programming, external resistor to DV_{SS} required
DV_{DD}	3	P	Logic supply voltage
DV_{SS}	4, 24	P	Digital ground, reference for input signals
$\overline{ERR0}$	21	O	Logic output, signals chip operation mode/state. This output is open drain with internal pullup resistor.
$\overline{ERR1}$	22	O	Logic output, signals chip operation mode/state. This output is open drain with internal pullup resistor.
GHS_A	51	O	Gate drive output for high-side MOSFET, half-bridge A
GHS_B	45	O	Gate drive output for high-side MOSFET, half-bridge B
GHS_C	39	O	Gate drive output for high-side MOSFET, half-bridge C
GHS_D	33	O	Gate drive output for high-side MOSFET, half-bridge D
GLS_A	54	O	Gate drive output for low-side MOSFET, half-bridge A
GLS_B	48	O	Gate drive output for low-side MOSFET, half-bridge B
GLS_C	42	O	Gate drive output for low-side MOSFET, half-bridge C
GLS_D	36	O	Gate drive output for low-side MOSFET, half-bridge D
GV_{DD}	30, 55	P	Gate drive voltage supply terminal
GV_{SS}	29, 56	P	Gate drive voltage supply ground return
LOW/HIZ	23	I	Logic signal that determines the drive output state during a reset. When $\overline{RESET\_AB}$ or $\overline{RESET\_CD}$ is low, LOW/HIZ = 1 indicates that the outputs are low impedance LOW/HIZ = 0 indicates that the outputs are high impedance
NC	1, 2, 5, 25, 26		Not connected. Terminals 1, 2, 5, 25, and 26 may be connected to DV_{SS}.
OC_HIGH	8	I	High-side overcurrent trip value programming. OC configuration circuit (see Figure 5) is required.
OC_LOW	27	I	Low-side overcurrent trip value programming. OC configuration circuit (see Figure 5) is required.
$\overline{RESET\_AB}$	12	I	Reset signal half-bridge A and B, active low
$\overline{RESET\_CD}$	17	I	Reset signal half-bridge C and D, active low
$\overline{SHUTDOWN}$	20	O	Error/warning report indicator. This output is open drain with internal pull-up resistor.
SHS_A	52	I	High-side source connection, used as BST floating ground (and high-side V_{DS} sensing)
SHS_B	46	I	High-side source connection, used as BST floating ground (and high-side V_{DS} sensing)
SHS_C	40	I	High-side source connection, used as BST floating ground (and high-side V_{DS} sensing)
SHS_D	34	I	High-side source connection, used as BST floating ground (and high-side V_{DS} sensing)
SLS_A	53	I	Source connection low-side MOSFET, ground return terminal, half-bridge A
SLS_B	47	I	Source connection low-side MOSFET, ground return terminal, half-bridge B
SLS_C	41	I	Source connection low-side MOSFET, ground return terminal, half-bridge C
SLS_D	35	I	Source connection low-side MOSFET, ground return terminal, half-bridge D
TEMP	28	I	External temperature sensing connection
VRFILT	9	I	Bandgap reference = 1.8 V. Capacitor must be connected from VRFILT to DV_{SS}.

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAMS

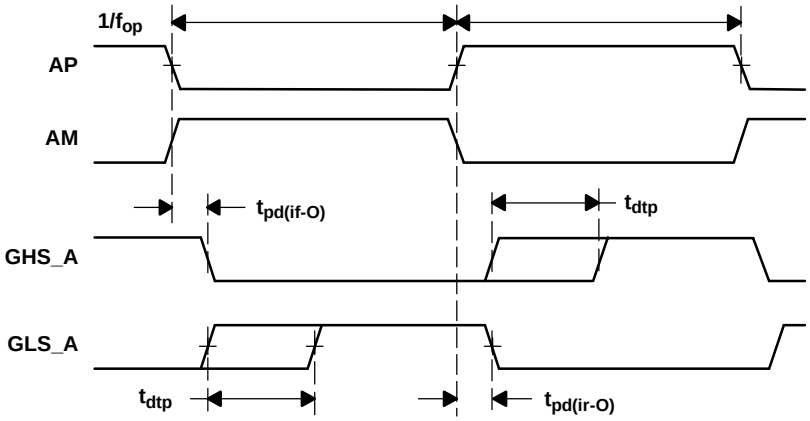


Figure 1. PWM Input to Gate Drive Output Timing (Same for A, B, C, and D Half-Bridge Drivers)

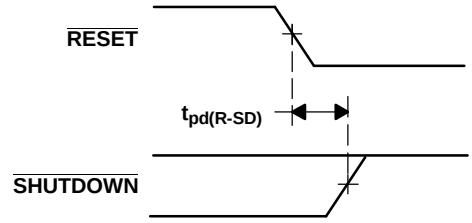


Figure 2. $\overline{\text{RESET}}$ to $\overline{\text{SHUTDOWN}}$ Propagation Delay

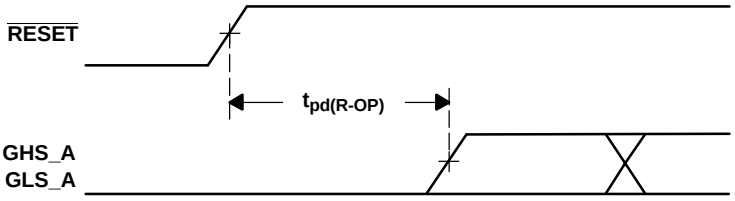
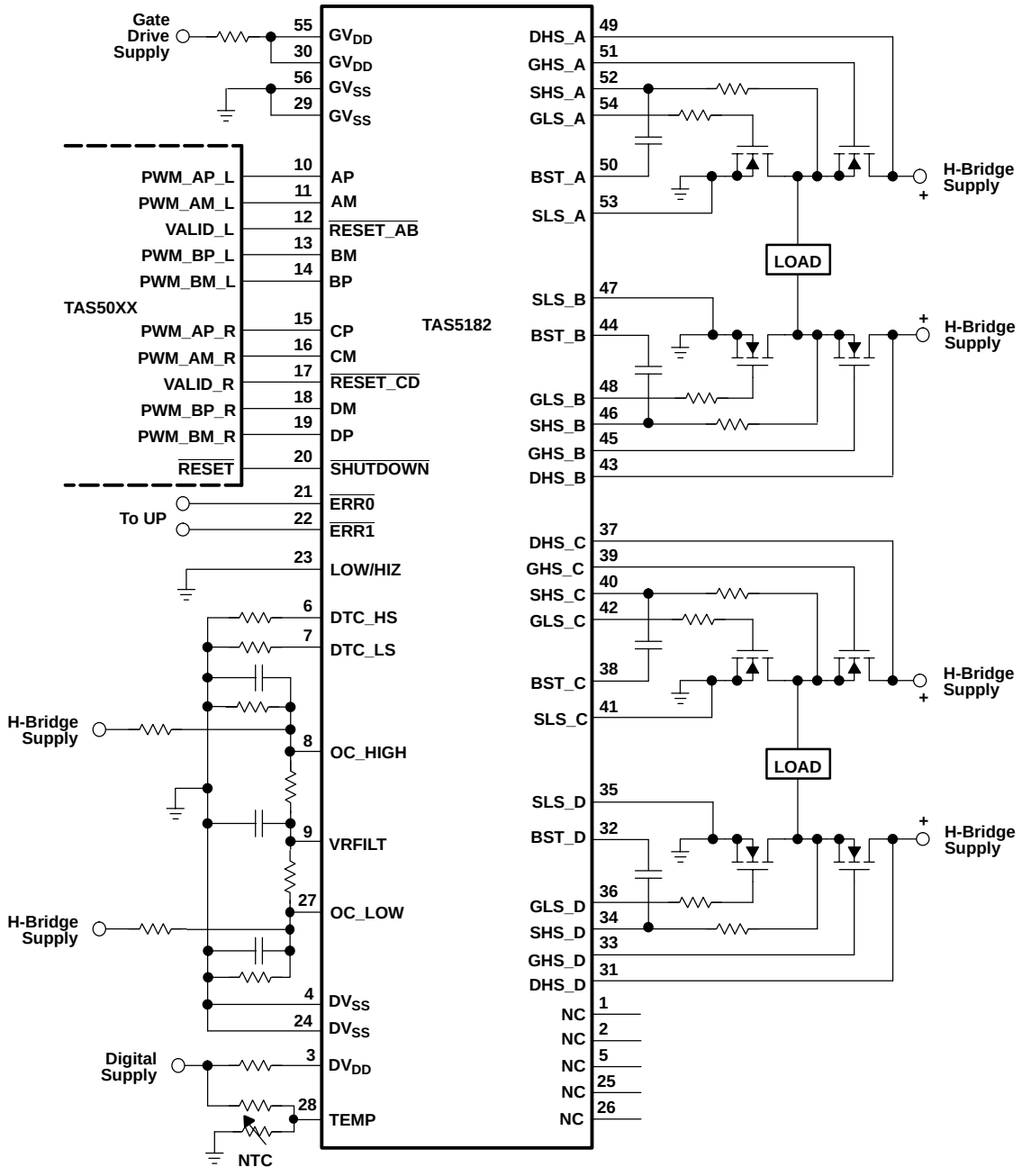


Figure 3. $\overline{\text{RESET}}$ to Gate Drive Output Propagation Delay (Same for Half-Bridge A, B, C, and D)

SIMPLIFIED APPLICATION CONNECTION DIAGRAM (BRIDGE-TIED-LOAD CONFIGURATION)



NOTE: Recommended power MOSFETs
International Rectifier IRFIZ24N (8 places)
For complete reference schematics contact Texas Instruments.

FUNCTIONAL DESCRIPTION

Power Stage Protection

The TAS5182 device provides overcurrent, overtemperature, and undervoltage protection for the MOSFET power stage.

Overcurrent Protection (OCP)

To protect the power stage from damage due to high currents, a V_{DS} sensing system is implemented in the TAS5182 device. Based on $R_{DS(on)}$ of the power MOSFETs and the maximum allowed I_{DS}, a voltage threshold can be calculated which, when exceeded, triggers the protection latch, causing the $\overline{\text{SHUTDOWN}}$ terminal to go low. This voltage threshold is resistor programmable. See the *Calculation of Overcurrent Resistor Values* section for more details.

Overtemperature Protection (OTP)

The TAS5182 device has a temperature protection system that uses an external negative temperature coefficient (NTC) resistor as a temperature sensor. See the *Overtemperature Programming Circuit* section for implementation details.

Undervoltage Protection (UVP)

To protect the power output stage during start-up, shutdown, and other possible undervoltage conditions, the TAS5182 device provides power stage undervoltage protection by driving its outputs low whenever GV_{DD} is under 7 V. With the TAS5182 outputs driven low, the MOSFETs go to a high-impedance state.

Control Terminals

The TAS5182 device provides input control terminals to reset each audio channel and also to control the electrical characteristics of the MOSFET output power stage.

Channel Reset

The reset function enables operation after power up, re-enables operation after an error event, and disables the MOSFET output stage switching during power down and mute. The falling edge of $\overline{\text{RESET\_AB}}$ (left audio channel) or $\overline{\text{RESET\_CD}}$ (right audio channel) causes the TAS5182 device to reset. The rising edge of $\overline{\text{RESET\_AB}}$ or $\overline{\text{RESET\_CD}}$ causes the TAS5182 device to clear the error latch and resume normal operation.

MOSFET Output Reset Control

The LOW/HIZ control terminal selects whether the MOSFET output stage goes into a high-impedance (HI-Z) state or LOW-LOW state when $\overline{\text{RESET\_AB}}$ or $\overline{\text{RESET\_CD}}$ is enabled. In the high-impedance state, the low-side and high-side MOSFETs are turned off causing no current flow through the MOSFETs. This effectively disconnects the load from the power supply rail. In the LOW-LOW state, the low-side MOSFETs are turned on, while the high-side MOSFETs are turned off. This causes a low or ground signal to be output to the load.

Status Terminals

The TAS5182 device provides output status terminals to report overcurrent, overtemperature, and undervoltage warnings and errors.

Shutdown Indicator

The $\overline{\text{SHUTDOWN}}$ terminal indicates an error event has occurred such as overcurrent, overtemperature, or undervoltage. The $\overline{\text{SHUTDOWN}}$ terminal is pulled high when $\overline{\text{RESET\_AB}}$ or $\overline{\text{RESET\_CD}}$ is asserted. $\overline{\text{ERR0}}$ and $\overline{\text{ERR1}}$ terminals along with the $\overline{\text{SHUTDOWN}}$ terminal indicate the type of warnings and errors. Note that $\overline{\text{SHUTDOWN}}$ is an open-drain signal. See Table 1 for a functional description of these signals.

Table 1. TAS5182 Status Signals

$\overline{\text{ERR0}}$	$\overline{\text{ERR1}}$	$\overline{\text{SHUTDOWN}}$	DESCRIPTION
0	0	0	Multiple errors (TAS5182 gate outputs low, MOSFET outputs HI-Z)
0	0	1	Not valid
0	1	0	Overtemperature error (TAS5182 gate outputs low, MOSFET outputs HI-Z)
0	1	1	Overtemperature warning (normal operation)
1	0	0	Overcurrent error (TAS5182 gate outputs low, MOSFET outputs HI-Z)
1	0	1	Not valid
1	1	0	GV_{DD} undervoltage error (TAS5182 gate outputs low, MOSFET outputs HI-Z)
1	1	1	Normal operation

TAS5182 Power Up and Reset

After power up, all gate drive outputs are held low (i.e., the error latch is set). Normal operation can be initiated by toggling $\overline{\text{RESET\_AB}}$ and/or $\overline{\text{RESET\_CD}}$ from a low state to a high state. If no errors are present, then the TAS5182 device is ready to accept audio inputs.

TAS5182 Reset and Error Timing

The TAS5182 device provides two output control configurations for reset and error situations. In a BTL system configuration, the MOSFET outputs must be grounded before resuming normal operation. This enables the bootstrap capacitors to charge.

Reset and Error Timing (BTL System)

When using this device in the BTL configuration, it is advisable to bring the MOSFET outputs to a high impedance state when reset ($\overline{\text{RESET\_AB}}$ or $\overline{\text{RESET\_CD}}$) is asserted. Figure 4 shows the timing that occurs in this configuration. This feature is enabled by connecting the LOW/HIZ terminal to DV_{SS}.

When an error event occurs (see Table 1) and following propagation delay $t_{pd(E-SD)}$, the TAS5182 device pulls the $\overline{\text{SHUTDOWN}}$ signal low. The falling edge of $\overline{\text{SHUTDOWN}}$ forces the MOSFET outputs into a high-impedance state. The $\overline{\text{SHUTDOWN}}$ signal is usually connected to the $\overline{\text{RESET}}$ terminal of the TAS50XX PWM controller. After some delay, the controller then asserts the TAS5182 $\overline{\text{RESET\_AB}}$ and $\overline{\text{RESET\_CD}}$ terminals low. The falling edge of $\overline{\text{RESET}}$ forces the MOSFET outputs to ground potential (this event also brings the $\overline{\text{SHUTDOWN}}$ signal high). This allows the bootstrap capacitors to charge through the grounded MOSFET outputs. When $\overline{\text{RESET}}$ is pulled high, the system resumes normal operation.

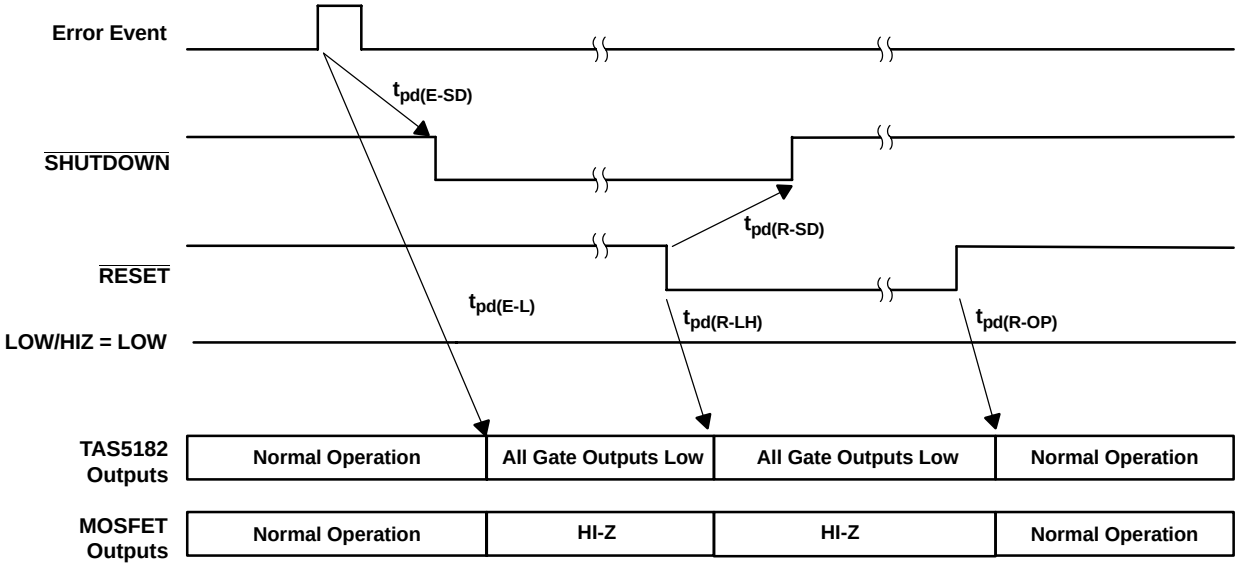


Figure 4. Reset and Error Timing (BTL System)

Overcurrent Configuration From Circuit

The output current flows through internal resistance $R_{DS(on)}$ of the external MOSFETs, which creates voltage drop V_{DS}. The overcurrent detector senses this voltage to trigger an error event. The exact current limit depends on parasitics from the PCB layout, resistance of the MOSFET at the operation temperature, and the configuration of the H-bridge output stage.

See Table 2 for the OCL and OCH reference voltages. Figure 5 shows the recommended overcurrent configuration circuit.

Table 2. OCL and OCH Reference Voltages (Overcurrent Configuration Circuit)

	VOLTAGE	OUTPUT INDUCTOR SHUTDOWN CURRENT RANGE(1)
OCL	0.7 V (terminal 27)	12-19 A
OCH	1.17 V (terminal 8)	14-24 A

(1) Measured on Texas Instruments reference board TAS5182C6REF.

Board configuration:

- 1R0 resistors on SHS and GLS connections
- GV_{DD} = 12 V, PV_{DD} = 40 V
- 10BQ060 voltage clamp on output node
- TT snubbers: L = 75 nH, C = 10 nF, R = 5.4 Ω

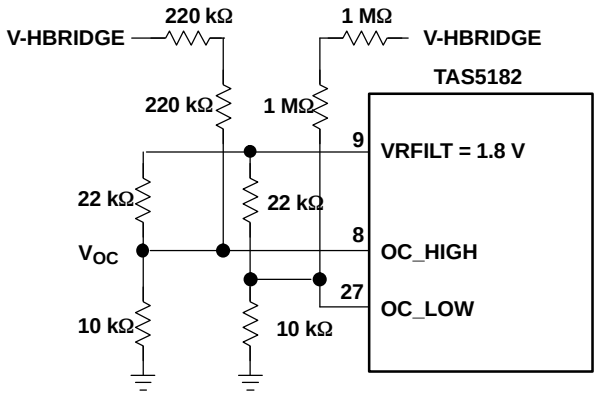


Figure 5. Overcurrent Configuration Circuit

Overtemperature Programming Circuit

The TAS5182 device features a temperature protection system that uses an external negative temperature coefficient (NTC) resistor as a temperature sensor. Figure 6 shows a typical application.

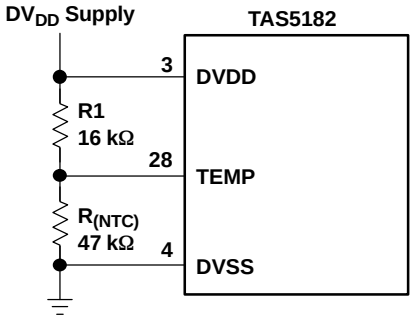


Figure 6. Temperature Sensing Circuit

The temperature protection system has two trigger limits: OT warning and OT error. OT warning occurs when the voltage at the TEMP terminal is approximately 36% of DV_{DD}. OT error occurs when the voltage at the TEMP terminal is approximately 23% of DV_{DD}. OT warning is decoded when $\overline{ERR0}$ = 0, $\overline{ERR1}$ = 1, and $\overline{SHUTDOWN}$ = 1. OT error is decoded when $\overline{ERR0}$ = 0, $\overline{ERR1}$ = 1, and $\overline{SHUTDOWN}$ = 0. The user for a particular application determines the values of R1 and R_{NTC}. Typical values are R1 = 16 kΩ and R_{NTC} = 47 kΩ.

THERMAL INFORMATION

The thermally enhanced DCA package is based on the 56-pin HTSSOP, but includes a thermal pad (see Figure 7) to provide an effective thermal contact between the IC and the PCB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220 type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have two shortcomings: they do not address the low profile requirements (< 2 mm) of many of today's advanced systems and they do not offer a terminal count high enough to accommodate increasing integration. However, traditional low-power, surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits

The PowerPAD™ package (thermally enhanced HTSSOP) combines fine-pitch, surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PCB. Because of the small size and limited mass of a HTSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered to the PCB, good power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved. See Reference 4 for recommended soldering procedure.

THERMAL DATA

PARAMETER		MIN	TYP	MAX	UNIT
Junction temperature, $T_{J(SD)}$				150	°C
Operating temperature, TC	Commercial	0	25	70	°C
	Industrial	-40	25	85	°C
Thermal resistance, θjc	Pad with solder (1)	0.27			°C/W
Thermal resistance, θja		21.17			°C/W
Thermal resistance, θjc	Pad without solder (1)	0.27			°C/W
Thermal resistance, θja		36.42			°C/W

(1) Values taken from Table 6 *Thermal Characteristics for Different Package and PCB Configurations* of the *PowerPAD Thermally Enhanced Package* application note (SLMA002). See pages 32 and 33 for a description of the printed circuit board (PCB) used for these measurements. Note that the PCB used for these measurements is not the recommended PCB for TAS5182 applications but is cited here for reference only.

Power Dissipation

The equation for TAS5182 power dissipation using N external MOSFETs is:

$P_d = V_{gd} \times Q_g \times f \times N$

where:

$V_{gd} = GV_{DD}$ (typically 12 V)

Q_g = MOSFET gate charge

f = operating frequency

N = number of external MOSFETs driven (eight for two-channel operation)

Example power dissipation calculation:

Given a TAS5182 system with eight external IRFIZ24N MOSFETs and GV_{DD} = 12 V. The power dissipation is:

$P_d = V_{gd} \times Q_g \times f \times N$ = 12V x 22.5nC x 384 kHz x 8 = 0.8 W

Note: Lab measurements yield a power dissipation of 0.8 W (PV_{DD} = 40 V).

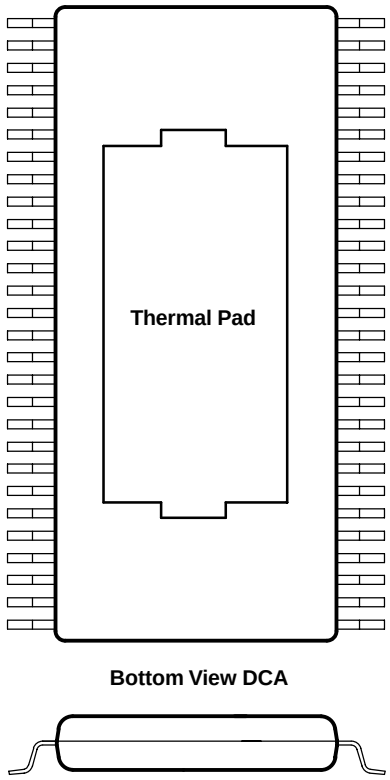


Figure 7. Views of a Thermally Enhanced DCA Package

REFERENCES

1. T*AS5000 Digital Audio PWM Process* data manual, Texas Instruments Literature Number SLAS270
2. *System Design Considerations for True Digital Audio Power Amplifiers,* Texas Instruments Literature Number SLAA117
3. *Digital Audio Measurements,* Texas Instruments Literature Number SLAA114
4. *PowerPAD Thermally Enhanced Package,* Texas Instruments Literature Number SLMA002

TAS5182 OUTPUT STAGE

To/From Texas Instruments TAS5036 PWM Modulator

TAS5182 SECTION

OC CONFIGURATION

V-HBRIDGE
R120 220k
R121 220k
R123 22k
VR-FILT
OC-HIGH
R124 10k
GND

V-HBRIDGE
R125 1M
R126 1M
R127 22k
VR-FILT
OC-LOW
R128 10k
GND

U201 — TAS5182

1	NC	56	GVSS
2	NC	55	GVDD
3	DVDD	54	GLS_A
4	DVSS	53	SLS_A
5	NC	52	SHS_A
6	DTC_HS	51	GHS_A
7	DTC_LS	50	BST_A
8	OC_HIGH	49	DHS_A
9	VRFILT	48	GLS_B
10	AP	47	SLS_B
11	AM	46	SHS_B
12	RESET_AB	45	GHS_B
13	BM	44	BST_B
14	BP	43	DHS_B
15	CP	42	GLS_C
16	CM	41	SLS_C
17	RESET_CD	40	SHS_C
18	DM	39	GHS_C
19	DP	38	BST_C
20	SHUTDOWN	37	DHS_C
21	ERR0	36	GLS_D
22	ERR1	35	SLS_D
23	LOW/HIZ	34	SHS_D
24	DVSS	33	GHS_D
25	NC	32	BST_D
26	NC	31	DHS_D
27	OC_LOW	30	GVDD
28	TEMP	29	GVSS

DVDD — R205 0R — C201 100nF
OC-HIGH — R210 0R — C214 100nF
VR-FILT — C202 100nF
PWM-AP-CH1
PWM-AM-CH1
/VALID-CH1
PWM-BM-CH1
PWM-BP-CH1
PWM-AP-CH2
PWM-AM-CH2
/VALID-CH2
PWM-BM-CH2
PWM-BP-CH2
/SHUTDOWN
/ERR0
/ERR1
OC-LOW — R211 0R — C213 100nF — C212 100nF
R207 16k — DVDD
R208 47k
GVDD — R212 1R — C205 1uF
R213 1R — C211 1uF — GVDD
C206 22nF
C207 22nF
C208 22nF
C209 22nF
GND

H-BRIDGE SECTION

PVDD-A
Q221 IRFIZ24N — C221 10nF — R223 2.70R
R221 1.00R
R222 1.00R
Q222 IRFIZ24N — R224 2.70R
D260 10BQ060 — R263 2.70R — V-HBRIDGE
C266 100nF
GND

PVDD-B
Q223 IRFIZ24N — C222 10nF — R227 2.70R
R225 1.00R
R226 1.00R
Q224 IRFIZ24N — R228 2.70R
D261 10BQ060 — R264 2.70R — V-HBRIDGE
C267 100nF
GND

PVDD-C
Q225 IRFIZ24N — C223 10nF — R231 2.70R
R229 1.00R
R230 1.00R
Q226 IRFIZ24N — R232 2.70R
D262 10BQ060 — R265 2.70R — V-HBRIDGE
C268 100nF
GND

PVDD-D
Q227 IRFIZ24N — C224 10nF — R235 2.70R
R233 1.00R
R234 1.00R
Q228 IRFIZ24N — R236 2.70R
D263 10BQ060 — R266 2.70R — V-HBRIDGE
C269 100nF
GND

DE-MODULATION FILTER CHANNEL 1

L240 7uH — CH1-OUT+
C240 470nF — R240 4.7R — C245 680pF — R242 4.70k — R244 4.70k
GND
V-HBRIDGE
C246 680pF
C241 470nF — R241 4.7R — R243 4.70k — R245 4.70k
L241 7uH — CH1-OUT-

POWER SUPPLY FILTER

PVDD-A — L260 75nH
PVDD-B — L261 75nH
C260 1000uF — C262 10nF — C264 1nF — R260 3.30R — GND — V-HBRIDGE
PVDD-C — L262 75nH
PVDD-D — L263 75nH
C261 1000uF — C263 10nF — C265 1nF — R261 3.30R — GND

DE-MODULATION FILTER CHANNEL 2

L280 7uH — CH2-OUT+
C280 470nF — R280 4.7R — C285 680pF — R282 4.70k — R284 4.70k
GND
V-HBRIDGE
C286 680pF
C281 470nF — R281 4.7R — R283 4.70k — R285 4.70k
L281 7uH — CH2-OUT-

Patents pending in circuitry design and layout (WO99/59241 & WO99/59242).

This circuitry may only be used together with the integrated circuit TAS5100/TAS5110/TAS5111/TAS5112/TAS5182 from Texas Instruments Incorporated.

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DIGITAL AUDIO & VIDEO DIVISION

Project: TAS5182C6REF	Rev: 6.00
Page Title: CHANNEL 1 & CHANNEL 2	Size:
File Name:	Engineer:
Date:	Page: of

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5182DCA	ACTIVE	HTSSOP	DCA	56	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5182	Samples
TAS5182IDCA	ACTIVE	HTSSOP	DCA	56	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TAS5182I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

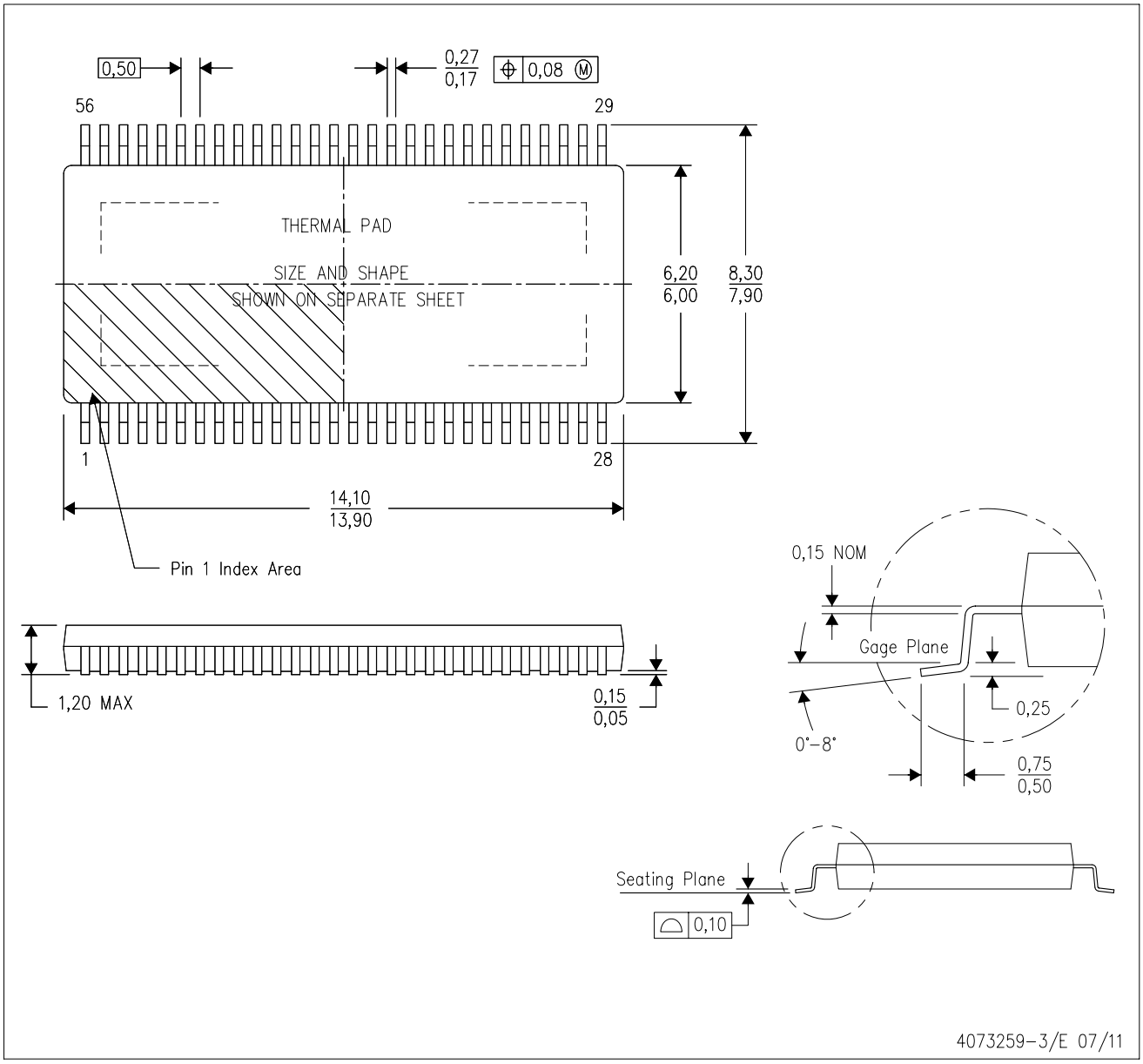
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

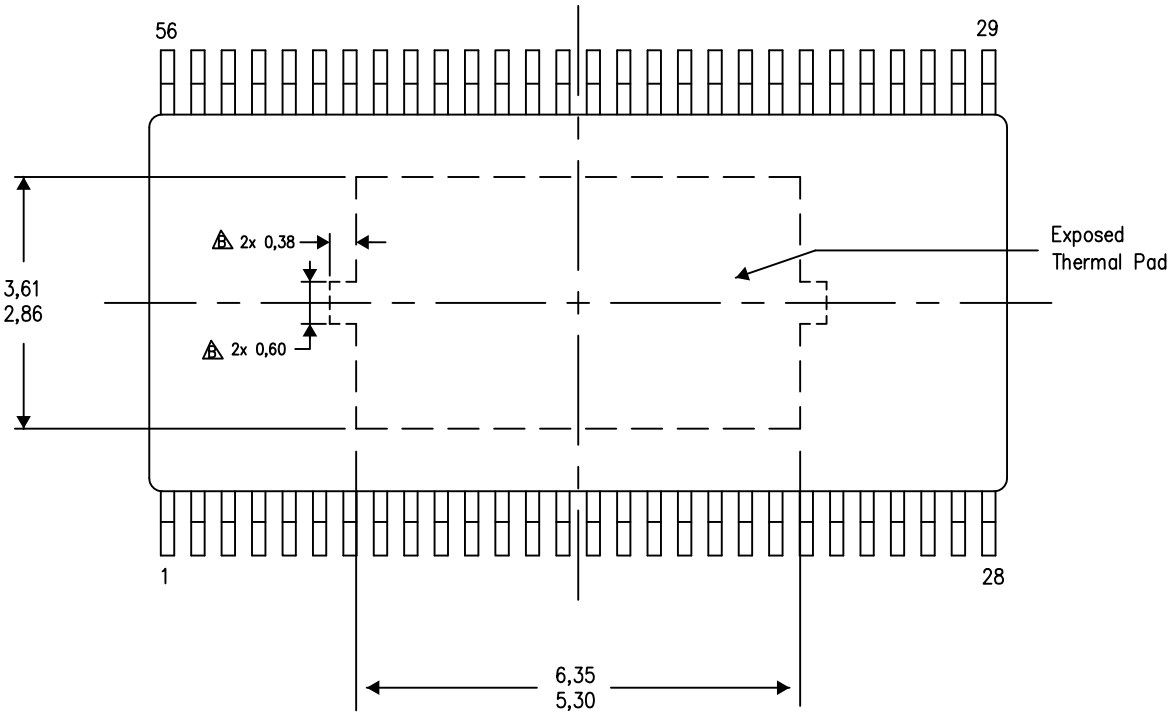
DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

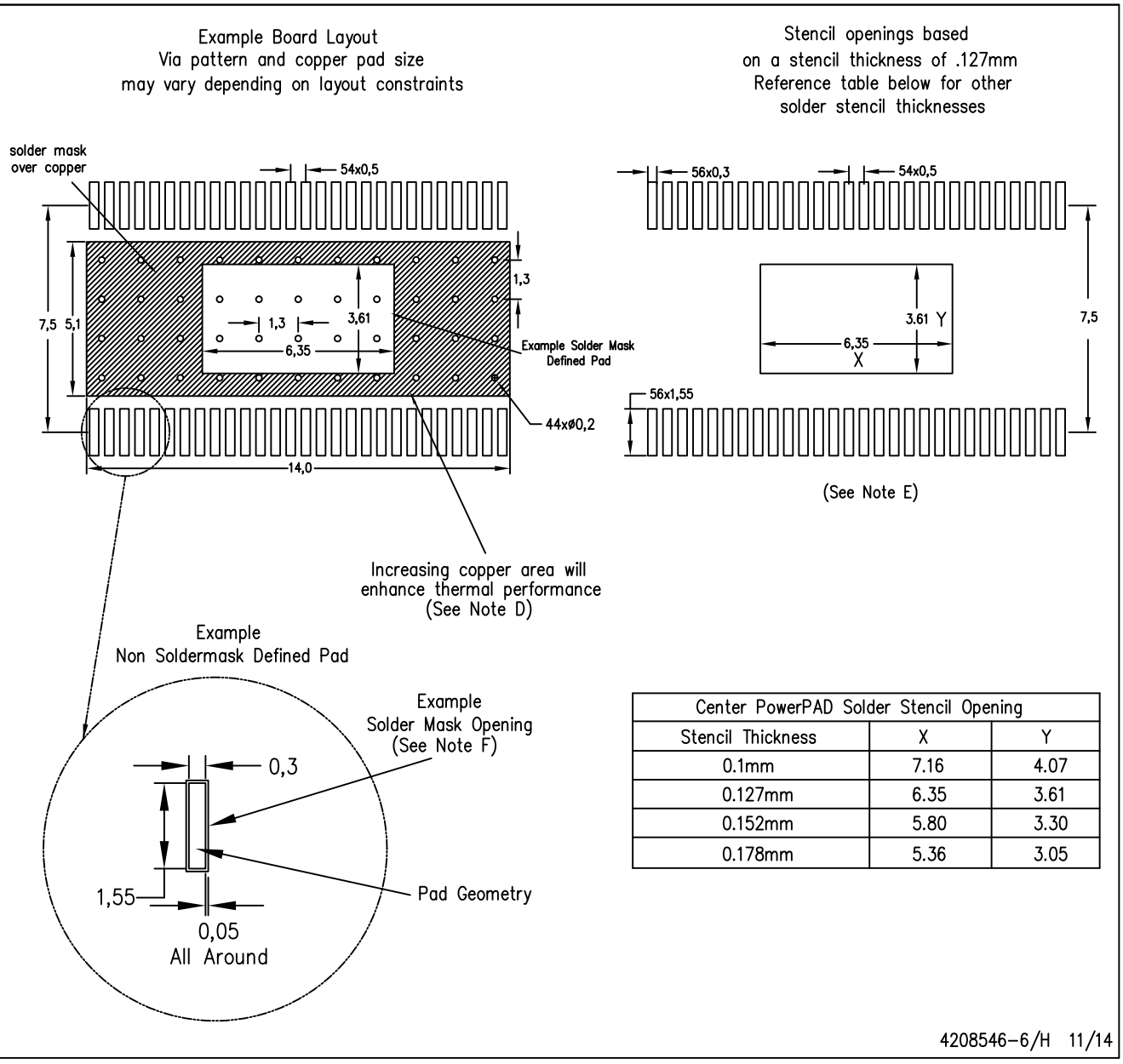
4206320–15/S 11/14

NOTES: A. All linear dimensions are in millimeters

B. Keep–out features are identified to prevent board routing interference.
These exposed metal features may vary within the identified area or completely absent on some devices.

PowerPAD is a trademark of Texas Instruments.

DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	7.16	4.07
0.127mm	6.35	3.61
0.152mm	5.80	3.30
0.178mm	5.36	3.05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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