











SCPS225C - AUGUST 2011 - REVISED DECEMBER 2017

TCA9509

TCA9509 Level-Translating I²C and SMBUS Bus Repeater

Features

- Two-Channel Bidirectional Buffer
- I²C Bus and SMBus Compatible
- Operating Supply Voltage Range of 2.7 V to 5.5 V on B side
- Operating Voltage Range of 0.9 V to 5.5 V on A-Side
- Voltage-Level Translation From 0.9 V to 5.5 V and 2.7 V to 5.5 V
- Active-High Repeater-Enable Input
- Requires No External Pullup Resistors on Lower-Voltage Port-A
- Open-Drain I²C I/O
- 5.5-V Tolerant I²C and Enable Input Support Mixed-Mode Signal Operation
- Lockup-Free Operation
- Accommodates Standard Mode and Fast Mode I²C Devices and Multiple Masters
- Supports Arbitration and Clock Stretching Across Repeater
- Powered-Off High-Impedance I²C Bus Pins
- Supports 400-kHz Fast I²C Bus Operating Speeds
- Available in
 - 1.6-mm × 1.6-mm, 0.4-mm height, 0.5-mm Pitch QFN Package
 - 3-mm × 3-mm Industry Standard MSOP Package
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Industrial Equipment
- Products with many I²C slaves and/or long PCB Traces

3 Description

This TCA9509 integrated circuit is an I²C bus/SMBus Repeater for use in I²C/SMBus systems. It can also provide bidirectional voltage-level translation (uptranslation/down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.5 V) in mixed-mode applications. This device enables I²C and similar bus systems to be extended, without degradation of performance even during level shifting.

The TCA9509 buffers both the serial data (SDA) and the serial clock (SCL) signals on the I²C bus, thus allowing 400-pF bus capacitance on the B-side. This device can also be used to isolate two halves of a bus for voltage and capacitance.

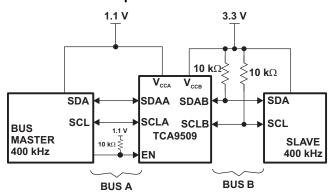
The TCA9509 has two types of drivers - A-side drivers and B-side drivers. All inputs and B-side I/Os are overvoltage tolerant to 5.5 V. The A-side I/Os are overvoltage tolerant to 5.5 V when the device is unpowered (VCCB and/or VCCA = 0 V).

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TC 4.05.00	VSSOP (8)	3.00 mm × 3.00 mm
TCA9509	X2QFN (8)	1.60 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Copyright © 2017, Texas Instruments Incorporated



Table of Contents

1	Features 1		9.2 Functional Block Diagram	8
2	Applications 1		9.3 Feature Description	9
3	Description 1		9.4 Device Functional Modes	9
4	Revision History2	10	Application and Implementation	10
5	Description (continued)3		10.1 Application Information	10
6	Pin Configuration or Functions		10.2 Typical Application	10
7	Specifications4	11	Power Supply Recommendations	13
•	7.1 Absolute Maximum Ratings 4 7.2 ESD Ratings 4 7.3 Recommended Operating Conditions 4 7.4 Thermal Information 5 7.5 Electrical Characteristics 5 7.6 Timing Requirements 5 7.7 I ² C Interface Timing Requirements 6		Layout	14 15 15 es 15 15
8	Parameter Measurement Information 7		13.4 Electrostatic Discharge Caution	15
9	Detailed Description89.1 Overview8	14	Mechanical, Packaging, and Orderable Information	

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	changes from Revision B (January 2012) to Revision C	Page
•	Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.	1
•	Added junction temperature to the Absolute Maximum Ratings	4
•	Changed thermal information for RVH and DGK packages	5
•	Changed V _{ILC} , added Test Conditions with new MIN and TYP values in the <i>Electrical Characteristics</i> table	5
•	Updated Bus A (0.9-V to 5.5-V Bus) Waveform	6
•	Updated Bus B (2.7-V to 5.5-V Bus) Waveform	6
С	Changes from Revision A (October 2011) to Revision B	Page
C	Changes from Revision A (October 2011) to Revision B Added DGK package and package information to datasheet.	
•	`	
•	Added DGK package and package information to datasheet.	1
•	Added DGK package and package information to datasheet	Page

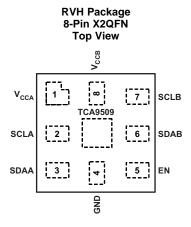


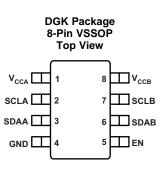
5 Description (continued)

The bus port B drivers are compliant with SMBus I/O levels, while the A-side uses a current sensing mechanism to detect the input or output LOW signal which prevents bus lock-up. The A-side uses a 1 mA current source for pull-up and a 200 Ω pull-down driver. This results in a LOW on the A-side accommodating smaller voltage swings. The output pull-down on the A-side internal buffer LOW is set for approximately 0.2 V, while the input threshold of the internal buffer is set about 50 mV lower than that of the output voltage LOW. When the A-side I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the B-side drives a hard LOW and the input level is set at 0.3 of SMBus or I²C-bus voltage level which enables B side to connect to any other I²C-bus devices or buffer.

The TCA9509 drivers are not enabled unless V_{CCA} is above 0.8 V and V_{CCB} is above 2.5 V. The enable (EN) pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the EN pin when the bus is idle.

6 Pin Configuration or Functions





Pin Functions

P	PIN		DESCRIPTION	
NAME	NO.	- I/O	DESCRIPTION	
V_{CCA}	1	Supply	A-side supply voltage (0.9 V to 5.5 V)	
SCLA	2	I/O	Serial clock bus, A side.	
SDAA	3	I/O	Serial data bus, A side.	
GND	4	Supply	Supply ground	
EN	5	Input	Active-high repeater enable input	
SDAB	6	I/O	Serial data bus, B side. Connect to V _{CCB} through a pull-up resistor.	
SCLB	7	I/O	Serial clock bus, B side. Connect to V _{CCB} through a pull-up resistor.	
V _{CCB}	8	Supply	B-side and device supply voltage (2.7 V to 5.5 V)	
Thermal Attach Pad	-	-	Thermal Attach Pad is not electrically connected and it is recommended to be attached to GND for best thermal performance. This is for the RVH package only.	



7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CCB}	Supply voltage		-0.5	6	V
V_{CCA}	Supply voltage		-0.5	6	V
V_{I}	Enable input voltage (2)		-0.5	6	V
V _{I/O}	I ² C bus voltage ⁽²⁾		-0.5	6	V
I _{IK}	Input clamp current	V ₁ < 0		-20	^
I _{OK}	Output clamp current	V _O < 0		-20	mA
P_d	Max power dissipation			100	mW
TJ	Junction temperature			125	°C
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
, Electrostatic	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	\/	
V _(ESD)	discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V _{CCA}	Supply voltage, A-side bus		0.9 ⁽¹⁾	5.5	V
V_{CCB}	Supply voltage, B-side bus		2.7	5.5	V
		SDAA, SCLA	0.7 × V _{CCA}	V_{CCA}	
V_{IH}	High-level input voltage	SDAB, SCLB	0.7 × V _{CCB}	5.5	V
		EN	$0.7 \times V_{CCA}$	5.5	
		SDAA, SCLA	-0.5	0.3	
V_{IL}	Low-level input voltage	SDAB, SCLB	-0.5	$0.3 \times V_{CCB}$	V
		EN	-0.5	0.3 × V _{CCA}	
	Lauren autaut aumant	SDAA, SCLA		10	μΑ
I _{OL}	Low-level output current	SDAB, SCLB		6	mA
T _A	Operating free-air temperature		-40	85	°C

(1) Low-level supply voltage

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



7.4 Thermal Information

		TCA		
	THERMAL METRIC ⁽¹⁾	RVH (X2QFN)	DGK (VSSOP)	UNIT
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽²⁾	160.3	222.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.4	109.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	115.9	144.5	°C/W
ΨЈТ	Junction-to-top characterization parameter	0.8	34.5	°C/W
ΨЈВ	Junction-to-board characterization parameter	116.2	142.7	°C/W
R ₀ JC(bot)	Junction-to-case (bottom) thermal resistance	80.5	n/a	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

 $V_{CCB} = 2.7 \text{ V}$ to 5.5 V, $V_{CCA} = 0.9 \text{ V}$ to $(V_{CCB}-1)$, $T_A = -40^{\circ}\text{C}$ to 85°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
V _{IK}	Input clamp voltage		I _I = -18 mA	-1.5		-0.5	V	
V	Low lovel output voltage	SDAA, SCLA	$\begin{split} I_{OL} &= 10 \; \mu A, \\ V_{ILA} &= V_{ILB} = 0 \; V, \\ V_{CCA} &= 0.9 \; to \; 1.2 \; V \end{split}$		0.18	0.25	V	
V _{OL}	Low-level output voltage	SDAA, SCLA	$\begin{split} &I_{OL} = 20 \; \mu A, \\ &V_{ILA} = V_{ILB} = 0 \; V, \\ &1.2 V < V_{CCA} \le (V_{CCB} - 1 \; V) \end{split}$		0.2	0.3	V	
V _{OL} – V _{ILc}	Low-level input voltage below low-level output voltage	SDAA, SCLA			50		mV	
\/	SDA and SCL low-level input	SDAA, SCLA	V _{CCA} ≥ 1.5 V and V _{CCB} ≥ 3.15 V	110	150		m1/	
V _{ILc}	voltage contention	SDAA, SCLA	V _{CCA} < 1.5 V or V _{CCB} < 3.15 V	50	100		mV	
V _{OLB}	Low-level output voltage	SDAB, SCLB	I _{OL} = 6 mA		0.1	0.2	V	
	Quiescent supply current for V		All port A Static high	0.25	0.45	0.9	mA	
I _{CC}	Quiescent supply current for V	CCA	All port A Static low	1.25			mA	
I _{CC}	Quiescent supply current for V	Quiescent supply current for V _{CCB}		0.5	0.9	1.1	mA	
		SDAB, SCLB	$V_I = V_{CCB}$			±1		
		SDAB, SCLB	V _I = 0.2 V			10		
	Input leakage current	SDAA, SCLA	$V_I = V_{CCA}$			±1	μА	
l _l	input leakage current	SDAA, SCLA	V _I = 0.2 V			10	μА	
		EN	$V_I = V_{CCB}$			±1		
		EN	V _I = 0.2 V			-10		
ı	High-level output leakage	SDAB, SCLB	V _O = 3.6 V			10	^	
I _{OH}	current	SDAA, SCLA	v ₀ = 3.0 v			10	μΑ	
C _{IOA}	I/O capacitance of A-side	SCLA, SDAA	V _I = 0 V		6.5	7	pF	
C _{IOB}	I/O capacitance of B-side	SCLB, SDAB	V _I = 0 V	5.5		6.2	pF	

7.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		MIN MAX	UNIT
t _{su}	Setup time, EN high before Start condition ⁽¹⁾	100	ns
t _h	Hold time, EN high after Stop condition ⁽¹⁾	100	ns

(1) EN should change state only when the global bus and the repeater port are in an idle state.

⁽²⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



7.7 I²C Interface Timing Requirements

 $T_A = -40$ °C to 85°C (unless otherwise noted)

	PARAMETE	ER .	V _{CCA} (INPUT)	V _{CCB} (OUTPUT)	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
	Propagation delay	port A to port B	1.9 V	5 V	EN High	123.1	127.2	132.8	
t _{PHL}	Propagation delay	port B to port A	1.9 V	5 V	EN FIGIT	88.1	88.8	89.8	ns
	Droposotion dolay	port A to port B	1.9 V	<i>E</i> \/	TN High	122.6	125.7	131.7	
t _{PLH}	Propagation delay	port B to port A	1.9 V	5 V	EN High	123	124.1	126.9	ns
	Transition time	port A	1.9 V	5 V	TN High	40.1	40.9	41.9	
t _{rise}	Transition time	port B	1.9 V	5 V	EN High	57.3	57.5	58.4	ns
	Transition time	port A	101/	E V	TN High	14.5	16.4	17.9	
t _{fall}	Transition time	port B	1.9 V	5 V	EN High	18.7	19.4	20.2	ns
t _{PLH2}	Propagation delay 50% of initial low on Port A to 1.5 V on Port B	port A to port B	1.9 V	5 V		176	177.3	178	ns
f _{MAX}	Maximum switching frequency					400			KHz

(1) Typical values were measured with $V_{CCA} = V_{CCB} = 2.7 \text{ V}$ at $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

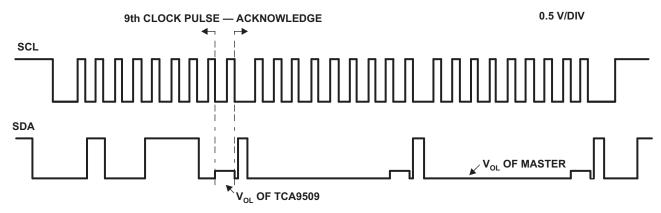


Figure 1. Bus A (0.9-V to 5.5-V Bus) Waveform

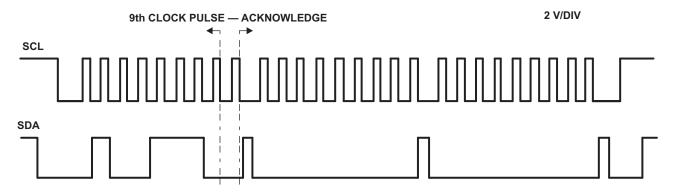
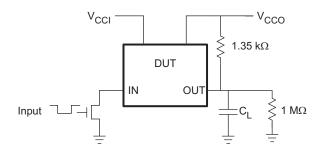


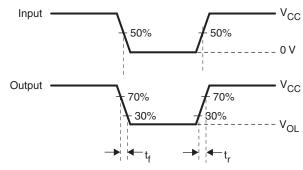
Figure 2. Bus B (2.7-V to 5.5-V Bus) Waveform



8 Parameter Measurement Information



PIN	CL
SCLA, SDAA (A-side)	50 pF
SDAB, SCLB (B-side)	50 pF



- A. R_T termination resistance should be equal to Z_{OUT} of pulse generators.
- B. C_L includes probe and jig capacitance.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, slew rate \geq 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Test Circuit and Voltage Waveforms



9 Detailed Description

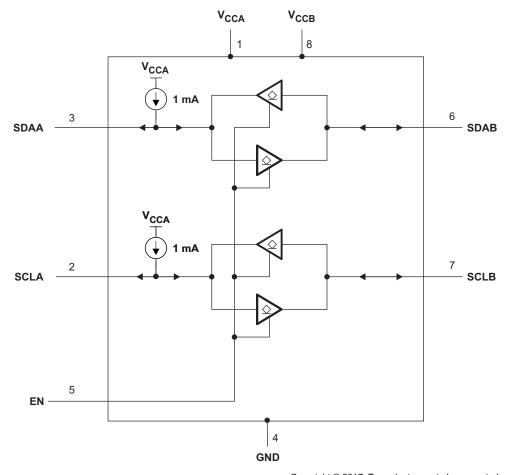
9.1 Overview

This TCA9509 integrated circuit is an I²C bus/SMBus Repeater for use in I²C/SMBus systems. It can also provide bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.5 V) in mixed-mode applications. This device enables I²C and similar bus systems to be extended, without degradation of performance even during level shifting.

The TCA9509 buffers both the serial data (SDA) and the serial clock (SCL) signals on the I²C bus, thus allowing 400-pF bus capacitance on the B-side. This device can also be used to isolate two halves of a bus for voltage and capacitance.

The TCA9509 has two types of drivers – A-side drivers and B-side drivers. All inputs and B-side I/O's are overvoltage tolerant to 5.5 V. The A-side I/O's are overvoltage tolerant to 5.5 V when the device is unpowered (V_{CCB} and/or $V_{\text{CCA}} = 0\text{V}$).

9.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated



9.3 Feature Description

9.3.1 Two-Channel Bidirectional Buffer

The TCA9509 is a two-channel bidirectional buffer with level-shifting capabilities, featuring an integrated current source on the A-side.

9.3.2 Integrated A-Side Current Source

The A-side ports of the TCA9509 feature an integrated 1 mA current source, eliminating the need for external pull-up resistors on SDAA and SCLA.

9.3.3 Standard Mode and Fast Mode Support

The TCA9509 supports standard mode as well as fast mode I²C. The maximum system operating frequency will depend on system design and delays added by the repeater.

9.4 Device Functional Modes

Table 1 lists the functional modes for the TCA9509.

Table 1. Function Table

INPUT EN	FUNCTION
L	Outputs disabled
Н	SDAA = SDAB SCLA = SCLB



10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TCA9509 is 5-V tolerant, so it does not require any additional circuitry to translate between 0.9-V to 5.5-V bus voltages and 2.7-V to 5.5-V bus voltages.

When the B-side of the TCA9509 is pulled low by a driver on the I^2C bus and the falling edge goes below 0.3 V_{CCB} , it causes the internal driver on the A-side to turn on, causing the A-side to pull down to about 0.2 V_{CCB} . When the A-side of the TCA9509 falls, a comparator detects the falling edge and causes the internal driver on the B-side to turn on and pull the B-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 1. If the bus master in Figure 4 were to write to the slave through the TCA9509, waveforms shown in Figure 2 would be observed on the B bus. This looks like a normal I^2C bus transmission, except that the high level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the A-side bus of the TCA9509, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the TCA9509. After the eighth clock pulse, the data line is pulled to the V_{OL} of the master device, which is close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the TCA9509 for a short delay, while the B-bus side rises above 0.3 V_{CCB} and then continues high. It is important to note that any arbitration or clock stretching events require that the low level on the A-bus side at the input of the TCA9509 (V_{IL}) be at or below V_{ILC} to be recognized by the TCA9509 and then transmitted to the B-bus side.

10.2 Typical Application

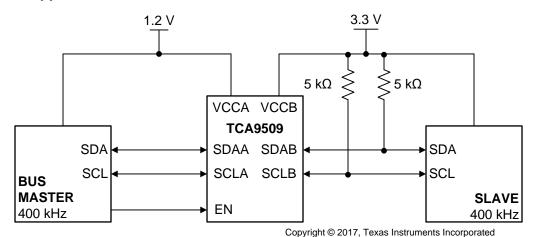


Figure 4. Typical Application, A-side Connected to Master

10.2.1 Design Requirements

A typical application is shown in Figure 4. In this example, the system master is running on a 1.2-V I^2C bus, and the slave is connected to a 3.3-V bus. Both buses run at 400 kHz. Master devices can be placed on either bus. For the level translating application, the following should be true: $V_{CCA} \le (V_{CCB} - 1 \text{ V})$

- $V_{CCA} = 0.9 \text{ V to } 5.5 \text{ V}$
- V_{CCB} = 2.7 to 5.5 V
- A-side ports must not be connected together
- Pullup resistors should not be placed on the A-side ports



Typical Application (continued)

10.2.2 Detailed Design Procedure

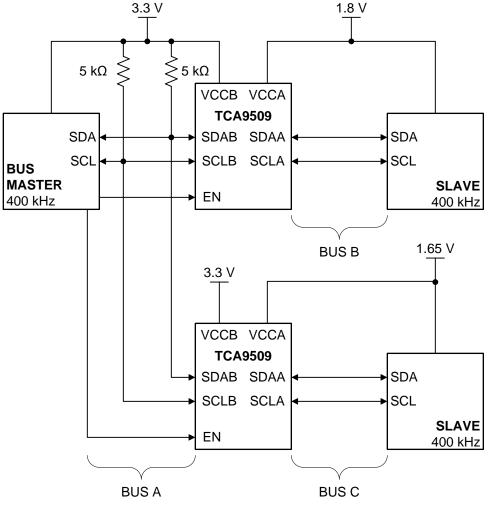
10.2.2.1 Clock Stretching Support

The TCA9509 can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the slave and master. This is best done by increasing the pull-up resistor value on B-side ports.

10.2.2.2 V_{ILC} and Pulldown Strength Requirements

For the TCA9509 to function correctly, all devices on the A-side must be able to pull the A-side below the voltage input low contention level (V_{ILC}). This means that the V_{OL} of any device on the A-side must be below V_{ILC} min.

The V_{OL} can be adjusted by changing the I_{OL} through the device which is set by the pull-up resistance value. The pull-up resistance on the A-side must be carefully selected to ensure that the logic levels will be transferred correctly to the B-side.



Copyright © 2017, Texas Instruments Incorporated

Figure 5. Typical Star Application

Multiple B-sides of TCA9509 s can be connected in a star configuration, allowing all nodes to communicate with each other. The A-sides should not be connected together when used in a star/parallel configuration.



Typical Application (continued)

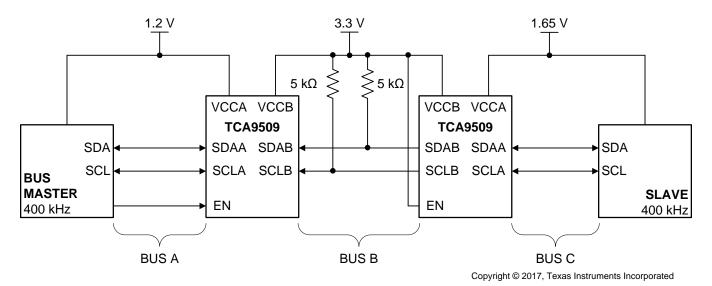


Figure 6. Typical Series Application, Two B-Sides Connected Together

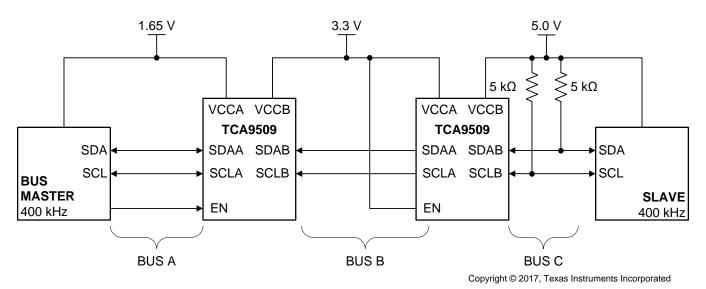


Figure 7. Typical Series Application, A-side Connected to B-Side

To further extend the I²C bus for long traces/cables, multiple TCA9509 devices can be connected in series as long as the A-side is connected to the B-side and $V_{CCA} \le (V_{CCB} - 1 \text{ V})$ must also be met. Series connections can also be made by connecting both B-sides together while following power supply rule $V_{CCA} \le (V_{CCB} - 1 \text{ V})$. I²C bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.



11 Power Supply Recommendations

 V_{CCB} and V_{CCA} can be applied in any sequence at power up. The TCA9509 includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5 V and the V_{CCA} is above 0.8 V. After power up and with the EN high, a low level on the B-side (below 0.3 × V_{CCB}) turns the corresponding A-side driver (either SDA or SCL) on and drives the A-side down to approximately 0.2 V. When the B-side rises above 0.3 × V_{CCB} , the A-side pull-down driver is turned off and the external pull-up resistor pulls the pin high. When the A-side falls first and goes below 0.3 × V_{CCA} , the B-side driver is turned on and the B-side pulls down to 0 V. The A-side pull-down is not enabled unless the A-side voltage goes below 0.4 V. If the A-side low voltage does not go below 0.5 V, the B-side driver turns off when the A-side voltage is above 0.7 × V_{CCA} . If the A-side low voltage goes below 0.4 V, the A-side pull-down driver is enabled, and the A-side is able to rise to only 0.5 V until the B-side rises above 0.3 × V_{CCB} .

A 100nF a decoupling capacitor should be placed as close to the V_{CCA} and V_{CCB} pins in order to provide proper filtering of supply noise.



12 Layout

12.1 Layout Guidelines

There are no special layout procedures required for the TCA9509. It is recommended that the decoupling capacitors be placed as close to the VCC pins as possible.

12.2 Layout Example

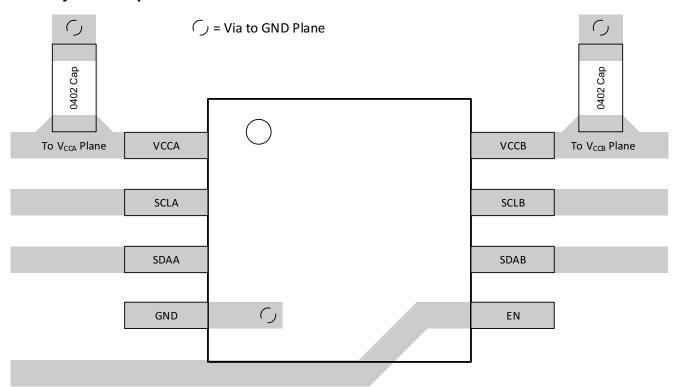


Figure 8. Example Layout

Product Folder Links: TCA9509

Copyright © 2011–2017, Texas Instruments Incorporated



13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



PACKAGE OPTION ADDENDUM

24-May-2017

PACKAGING INFORMATION

Orderable Device	Status	Package Type	_	Pins	_	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
TCA9509DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(7KO ~ 7KQ)	Samples
TCA9509RVHR	ACTIVE	X2QFN	RVH	8	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7K	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.





24-May-2017

PACKAGE MATERIALS INFORMATION

www.ti.com 3-Aug-2017

TAPE AND REEL INFORMATION





_		
		Dimension designed to accommodate the component width
	B0	Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
ı	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

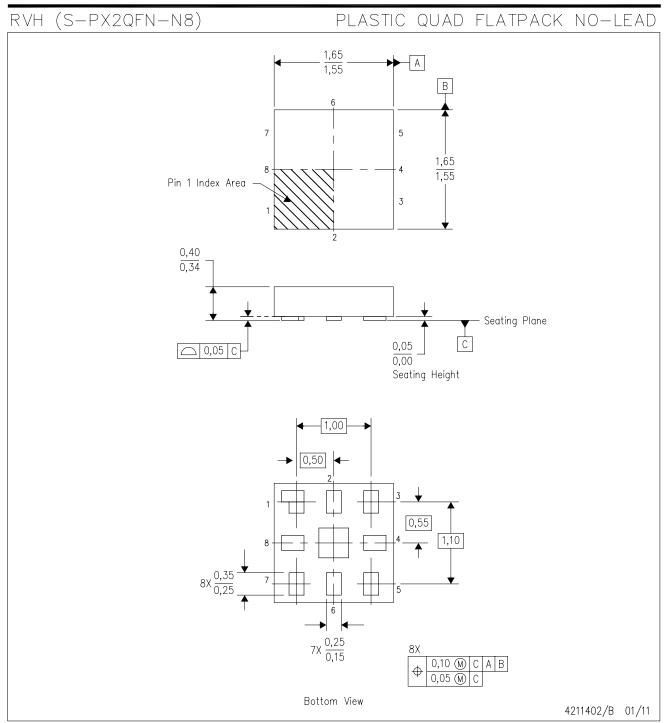
7 til dilliononono aro momina												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9509DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TCA9509RVHR	X2QFN	RVH	8	5000	180.0	8.4	1.8	1.8	0.5	4.0	8.0	Q3

www.ti.com 3-Aug-2017



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
TCA9509DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0	
TCA9509RVHR	X2QFN	RVH	8	5000	202.0	201.0	28.0	



NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- This drawing is subject to change without notice. QFN (Quad Flatpack No-Lead) package configuration.
- D. This package complies to JEDEC MO-255.



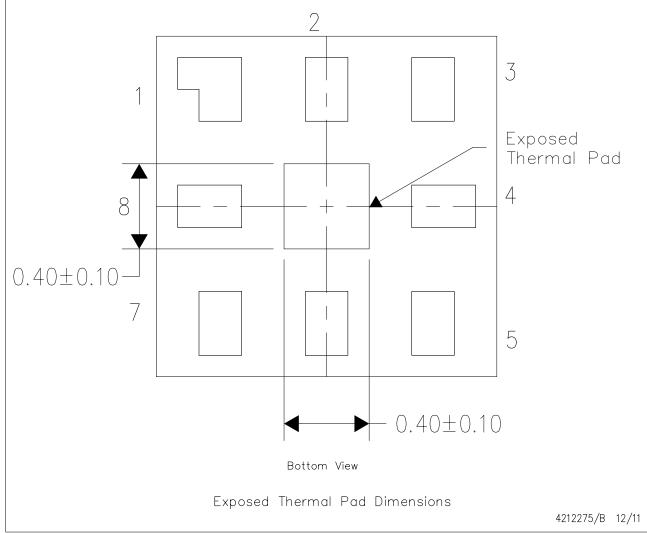
RVH (S-PX2SON-N8)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



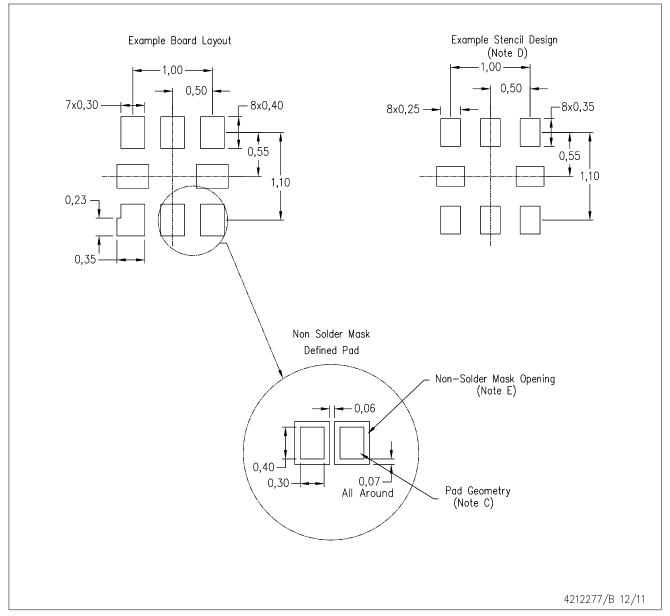
NOTES:

A. All linear dimensions are in millimeters



RVH (S-PX2QFN-N8)

PLASTIC SMALL OUTLINE NO-LEAD



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.



DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.