- Very Low Power . . . 200 μW Typ at 5 V
- Fast Response Time . . . 2.5 μs Typ With 5-mV Overdrive
- Single Supply Operation:

TLC139M . . . 4 V to 16 V TLC339M . . . 4 V to 16 V TLC339C . . . 3 V to 16 V TLC339I . . . 3 V to 16 V

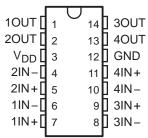
- High Input Impedance . . .  $10^{12} \Omega$  Typ
- Input Offset Voltage Change at Worst Case Input at Condition Typically 0.23 μV/Month Including the First 30 Days
- On-Chip ESD Protection

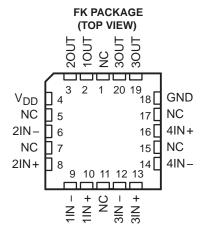
#### description

The TLC139/TLC339 consists of four independent differential-voltage comparators designed to operate from a single supply. It is functionally similar to the LM139/LM339 family but uses 1/20th the power for similar response times. The open-drain MOS output stage interfaces to a variety of leads and supplies, as well as wired logic functions. For a similar device with a push-pull output configuration, see the TLC3704 data sheet.

The Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

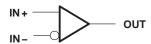
# D, J, N, OR PW PACKAGE (TOP VIEW)





NC - No internal connection

#### symbol (each comparator)



#### **AVAILABLE OPTIONS**

	V			PACKAGE		
TA	V <sub>IO</sub> max AT 25°C	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (P)	TSSOP (PW)
0°C to 70°C	5 mV	TLC339CD	_	_	TLC339CN	TLC339CPW
-40°C to 85°C	5 mV	TLC339ID	_		TLC339IN	TLC339IPW
-40°C to 125°C	5 mV	TLC339QD	_	_	TLC339QN	_
-55°C to 125°C	5 mV	TLC339MD	TLC139MFK	TLC139MJ	TLC339MN	_

The D and PW packages are available taped and reeled. Add the suffix R to the device type (e.g., TLC339CDR or TLC339CPWR).

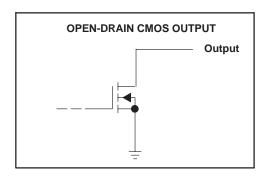
LinCMOS is a trademark of Texas Instruments Incorporated



#### description (continued)

The TLC139M and TLC339M are characterized for operation over the full military temperature range of -55°C to 125°C. The TLC339C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TLC339I is characterized for operation over the industrial temperature range of -40°C to 85°C. The TLC339Q is characterized for operation over the extended industrial temperature range of -40°C to 125°C.

#### output schematic



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>DD</sub> (see Note 1)	
Input voltage range, V <sub>I</sub>	
Output voltage range, VO	
Input current, I <sub>1</sub>	±5 mĀ
Output current, I <sub>O</sub> (each output)	20 mA
Total supply current into V <sub>DD</sub>	40 mA
Total current out of GND	60 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T <sub>A</sub> : TLC139M	–55°C to 125°C
TLC339C	0°C to 70°C
TLC339I	–40°C to 85°C
TLC339M	–55°C to 125°C
TLC339Q	–40°C to 125°C
Storage temperature range	–65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	26000
	je∠60 C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.

2. Differential voltages are at IN+ with respect to IN -.

#### **DISSIPATION RATING TABLE**

PACKAGE	$T_{\mbox{A}} \le 25^{\circ}\mbox{C}$ POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
PW	700 mW	5.6 mW/°C	448 mW	364 mW	140 mW



#### recommended operating conditions

	TLC	139M, TI	_C339M	UNIT
	MIN	NOM	MAX	UNII
Supply voltage, V <sub>DD</sub>	4	5	16	V
Common-mode input voltage, V <sub>IC</sub>	0		V <sub>DD</sub> -1.5	V
Low-level output current, IOL			20	mA
Operating free-air temperature, T <sub>A</sub>	-55		125	°C

# electrical characteristics at specified operating free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

PARAMETER		TEOT 0.0	NDITIONS <sup>†</sup>	т.	TLC139N	I, TLC33	39M	UNIT
	PARAMETER	TEST CC	ONDITIONS†	TA	MIN	TYP	MAX	UNII
		., ., .	51// 401/	25°C		1.4	5	
V <sub>IO</sub>	Input offset voltage	V <sub>IC</sub> = V <sub>ICR</sub> min, See Note 3	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	-55°C to 125°C			10	mV
	land offer terms of	V 0.5.V		25°C		1		рΑ
lio	Input offset current	V <sub>IC</sub> = 2.5 V		125°C			15	nA
	land blackman	V 0.5.V		25°C		5		рΑ
Ι <sub>ΙΒ</sub>	Input bias current	V <sub>IC</sub> = 2.5 V		125°C			30	nA
VICR	Common-mode input			25°C	0 to V <sub>DD</sub> -1			٧
	voltage range			−55°C to 125°C	0 to V <sub>DD</sub> –1.5			V
				25°C		84		
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICR</sub> min		125°C		84		dB
			−55°C		84			
				25°C		85		
kSVR	Supply-voltage rejection ratio	$V_{DD} = 5 \text{ V to } 10 \text{ V}$		125°C		84		dB
						84		
V	Laurence autout voltana	V 4.V		25°C		300	400	>/
VOL	Low-level output voltage	$V_{ID} = -1 V$ ,	$I_{OL} = 6 \text{ mA}$	125°C			800	mV
	I Pale I and a day of a consent	V 4.V		25°C		0.8	40	nA
Іон	High-level output current	$V_{ID} = -1 V$ ,	$V_O = 5 V$	125°C			1	μΑ
	Cumply ourrent /four			25°C		44	80	
IDD	Supply current (four comparators)	Outputs low,	No load	−55°C to 125°C			175	μА

<sup>&</sup>lt;sup>†</sup> All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-k $\Omega$  load to VDD.



# TLC139, TLC339, TLC339Q LinCMOS™ MICROPOWER QUAD COMPARATORS

#### recommended operating conditions

		TLC33	9C	UNIT
	MIN	NOM	MAX	UNII
Supply voltage, V <sub>DD</sub>	3	5	16	V
Common-mode input voltage, V <sub>IC</sub>	-0.2		V <sub>DD</sub> -1.5	V
Low-level output current, I <sub>OL</sub>		8	20	mA
Operating free-air temperature,T <sub>A</sub>	0		70	°C

# electrical characteristics at specified operating free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

	PARAMETER	TEST CO.	NDITIONS†	TA	TLO	C339C		UNIT		
	FARAWETER	TEST CO	NDITIONS	'A	MIN	TYP	MAX	UNII		
\/	Innut offeet voltege	V <sub>IC</sub> = V <sub>ICR</sub> min,	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	25°C		1.4	5	mV		
VIO	Input offset voltage	See Note 3		0°C to 70°C			6.5	IIIV		
	lanut effect coment	\/ 0.5\/		25°C		1		pА		
lio	Input offset current	V <sub>IC</sub> = 2.5 V		70°C			0.3	nA		
	lanut bias sumant	V 0.5.V		25°C		5		рА		
IВ	Input bias current	V <sub>IC</sub> = 2.5 V		70°C			0.6	nA		
V <sub>ICR</sub>	Common-mode input			25°C	0 to V <sub>DD</sub> -1			V		
	voltage range			0°C to 70°C	0 to V <sub>DD</sub> -1.5			V		
		V <sub>IC</sub> = V <sub>ICR</sub> min		25°C		84				
CMRR	Common-mode rejection ratio			70°C		84		dB		
	Tallo			0°C		84				
	0 1 1 1 1			25°C		85				
ksvr	Supply-voltage rejection ratio	$V_{DD} = 5 \text{ V to } 10 \text{ V}$		70°C		85		dB		
	Tallo			0°C		85				
V	Low lovel output voltage	V 4 V	la. CmA	25°C		300	400	mV		
VOL	Low-level output voltage	$V_{ID} = -1 V$ ,	$I_{OL} = 6 \text{ mA}$	70°C			650	IIIV		
	High lovel output ourse	V:- 4 V	V- 5.V	25°C		0.8	40	nA		
Іон	High-level output current	$V_{ID} = -1 V$ ,	V <sub>O</sub> = 5 V	70°C			1	μΑ		
Inn	Supply current (four	pply current (four	No load	25°C		44	80	μА		
IDD	comparators)	Outputs low,	INU IUAU	0°C to 70°C			100	μΑ		

<sup>&</sup>lt;sup>†</sup> All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to VDD.



#### recommended operating conditions

		TLC33	91	UNIT
	MIN         NOM         MAX           3         5         16           -0.2         V <sub>DD</sub> -1.5	UNII		
Supply voltage, V <sub>DD</sub>	3	5	16	V
Common-mode input voltage, V <sub>IC</sub>	-0.2		V <sub>DD</sub> -1.5	V
Low-level output current, IOL		8	20	mA
Operating free-air temperature,TA	0		70	°C

# electrical characteristics at specified operating free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

	DADAMETED	TEOT O	ONDITIONS <sup>†</sup>	т.	TL	TLC339I		
	PARAMETER	IESI C	ONDITIONST	TA	MIN	TYP	MAX	UNIT
.,	land effect cellans	V <sub>IC</sub> = V <sub>ICR</sub> min,	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	25°C		1.4	5	
VIO	Input offset voltage	See Note 3		-40°C to 85°C			7	mV
		.,		25°C		1		pA
IIO	Input offset current	V <sub>IC</sub> = 2.5 V		85°C			1	nA
	Lancet Is to a summer of	V 0.5.V		25°C		5		pA
IВ	Input bias current	V <sub>IC</sub> = 2.5 V		85°C			2	nA
V <sub>ICR</sub>	Common-mode input			25°C	0 to V <sub>DD</sub> –1			.,
	voltage range			-40°C to 85°C	0 to V <sub>DD</sub> – 1.5			V
		VIC = VICRmin		25°C		84		
CMRR	Common-mode rejection ratio			85°C		84		dB
	ratio			-40°C		84		
				25°C		85		
ksvr	Supply-voltage rejection ratio	V <sub>DD</sub> = 5 V to 10 V		85°C		85		dB
	ratio			-40°C		84		
.,	Lave laved a vita et valta na	V 4.V	L C A	25°C		300	400	\/
VOL	Low-level output voltage	$V_{ID} = -1 V$ ,	$I_{OL} = 6 \text{ mA}$	85°C			700	mV
la	High loved output oursest	\/ 4\/	V- 5.V	25°C		0.8	40	nA
ЮН	High-level output current	$V_{ID} = -1 V$ ,	V <sub>O</sub> = 5 V	85°C			1	μΑ
Inn	Supply current (four	Outputs low,	No load	25°C		44	80	^
lDD	comparators)	Outputs low,	INU IUdu	-40°C to 85°C			125	μA

<sup>&</sup>lt;sup>†</sup> All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-k $\Omega$  load to VDD.



# TLC139, TLC339, TLC339Q LinCMOS™ MICROPOWER QUAD COMPARATORS

#### recommended operating conditions

		TLC339	Q Q	UNIT
	MIN	NOM	MAX	UNII
Supply voltage, V <sub>DD</sub>	4	5	16	V
Common-mode input voltage, V <sub>IC</sub>	0		V <sub>DD</sub> -1.5	V
Low-level output current, I <sub>OL</sub>			20	mA
Operating free-air temperature,T <sub>A</sub>	- 40		125	°C

# electrical characteristics at specified operating free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

	PARAMETER	TEAT 001	unitions†	т.	TLO	C339Q		UNIT	
	PARAMETER	IESI COI	NDITIONS†	TA	MIN	TYP	MAX	UNII	
.,	land offert college	V <sub>IC</sub> = V <sub>ICR</sub> min,	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	25°C		1.4	5		
VIO	Input offset voltage	See Note 3		-40°C to 125°C			10	mV	
1	land offert compart	V 25V		25°C		1		pA	
lio	Input offset current	V <sub>IC</sub> = 2.5 V		125°C			15	nA	
	Lancet Island comment	V 05V		25°C		5 30	pA		
I <sub>IB</sub>	Input bias current	V <sub>IC</sub> = 2.5 V		125°C			30	nA	
VICR	Common-mode input			25°C	0 to V <sub>DD</sub> -1				
	voltage range			-40°C to 125°C	0 to V <sub>DD</sub> –1.5				
		v <sub>IC</sub> = v <sub>ICR</sub> min		25°C		84			
CMRR	Common-mode rejection ratio			125°C		84		dB	
	ratio			-40°C		84			
				25°C		85			
ksvr	Supply-voltage rejection ratio	$V_{DD} = 5 \text{ V to } 10 \text{ V}$		125°C		84		dB	
	Tallo			−40°C		84			
V	Lave lavel autout valtage	V 4.V	1 C A	25°C		300	400	\/	
VOL	Low-level output voltage	$V_{ID} = -1 V$ ,	$I_{OL} = 6 \text{ mA}$	125°C			800	mV	
	Ulab laval autout august	- 4 V	V- 5.V	25°C		0.8	40	nA	
ІОН	High-level output current	$V_{ID} = -1 V$ ,	V <sub>O</sub> = 5 V	125°C			1	μΑ	
loo	Supply current (four	ply current (four	No load	25°C		44	80	μА	
IDD	comparators)	Outputs low,	INO IOAU	-40°C to 125°C			125	μΑ	

<sup>&</sup>lt;sup>†</sup> All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-k $\Omega$  load to VDD.



## switching characteristics, $V_{DD} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$ (see Figure 3)

	PARAMETER	TEST CO	TLC139M, TLC339C TLC339I, TLC339M TLC339Q			UNIT	
				MIN	TYP	MAX	
			Overdrive = 2 mV		4.5		
			Overdrive = 5 mV		2.5		
	Propagation delay time, low-to-high output	f = 10 kHz, C <sub>L</sub> = 15 pF	Overdrive = 10 mV		1.7		
<sup>t</sup> PLH			Overdrive = 20 mV		1.2		μs
			Overdrive = 40 mV		1.0		
		V <sub>I</sub> = 1.4 V step at I	1.1				
			Overdrive = 2 mV		3.6		
			Overdrive = 5 mV	2.1			
1.	Description delegation block to leave beautiful	f = 10 kHz, C <sub>I</sub> = 15 pF	Overdrive = 10 mV		1.3		
tPHL	Propagation delay time, high-to-low level output	OL = 13 pi	Overdrive = 20 mV		0.85		μs
			Overdrive = 40 mV	0.55			
		V <sub>I</sub> = 1.4 V step at I	0.10				
tTHL	Transition time, high-to-low level output	f = 10 kHz, C <sub>L</sub> = 15pF	Overdrive = 50 mV		20		ns

#### PARAMETER MEASUREMENT INFORMATION

The TLC139 and TLC339 contain a digital output stage that, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for testing parameters such as input offset voltage, common-mode rejection, etc., are suggested.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V<sub>ICR</sub> test, rather than changing the input voltages, to provide greater accuracy.

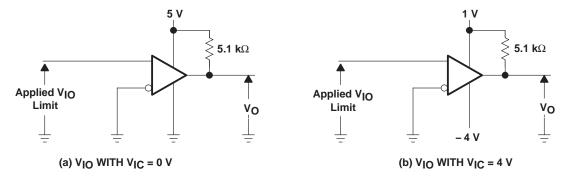


Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits



#### PARAMETER MEASUREMENT INFORMATION

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes state.

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which U1A generates a triangular waveform of approximately 20-mV amplitude. U1B acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1C through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

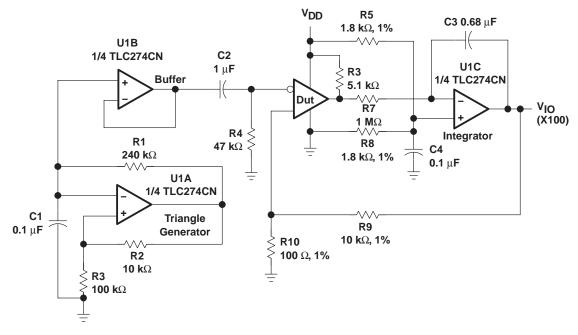


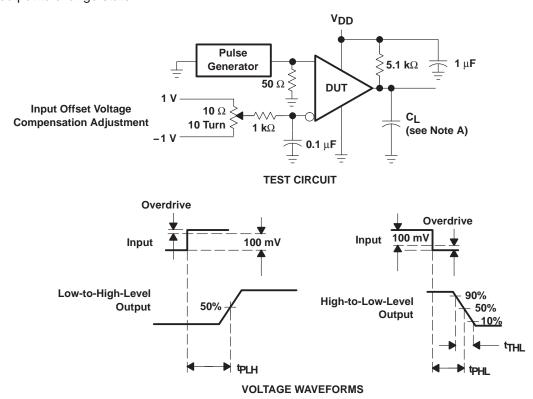
Figure 2. Circuit for Input Offset Voltage Measurement

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained, with a device in the socket to obtain the actual input current of the device.



#### PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input as shown in Figure 3, so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.



NOTE A: C<sub>L</sub> includes probe and jig capacitance.

Figure 3. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms



# TLC139, TLC339, TLC339Q LinCMOS™ MICROPOWER QUAD COMPARATORS

## **TYPICAL CHARACTERISTICS**

#### **Table of Graphs**

			FIGURE
VIO	Input offset voltage	Distribution	4
I <sub>IB</sub>	Input bias current	vs Free-air temperature	5
CMRR	Common-mode rejection ratio	vs Free-air temperature	6
ksvr	Supply-voltage rejection ratio	vs Free-air temperature	7
ЮН	High-level output current	vs High-level output voltage vs Free-air temperature	8 9
V <sub>OL</sub>	Low-level output voltage	vs Low-level output current vs Free-air temperature	10 11
I <sub>DD</sub>	Supply current	vs Supply voltage vs Free-air temperature	12 13
<sup>t</sup> PLH	Low-to-high level output propagation delay time	vs Supply voltage	14
<sup>t</sup> PHL	Low-to-high level output propagation delay time	vs Supply voltage	15
	Overdrive voltage	vs Low-to-high-level output propagation delay time	16
tf	Output fall time	vs Supply voltage	17
	Overdrive voltage	vs High-to-low-level output propagation delay time	18



#### TYPICAL CHARACTERISTICS<sup>†</sup>

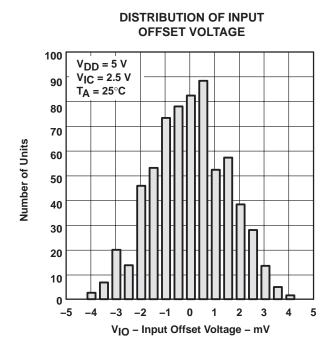
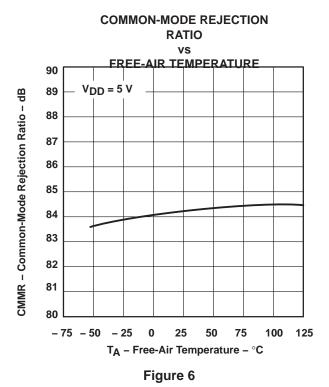


Figure 4



INPUT BIAS CURRENT vs
FREE-AIR TEMPERATURE

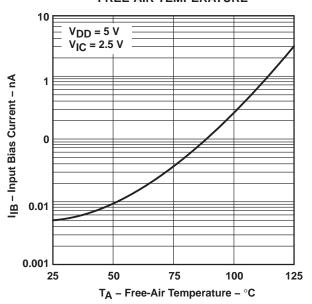


Figure 5

# SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

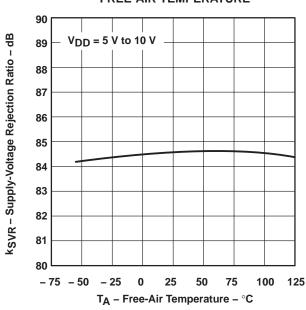
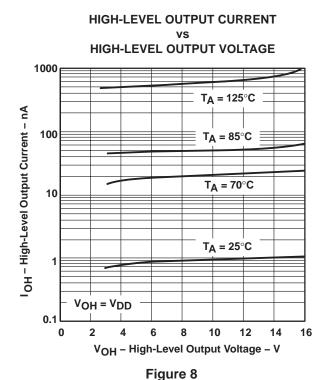


Figure 7

<sup>†</sup>Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



#### TYPICAL CHARACTERISTICS<sup>†</sup>



HIGH-LEVEL OUTPUT CURRENT vs FREE-AIR TEMPERATURE

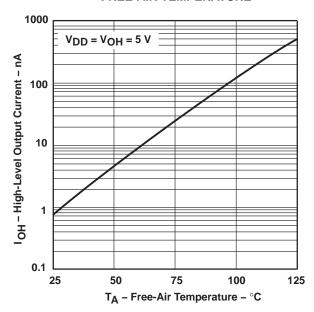
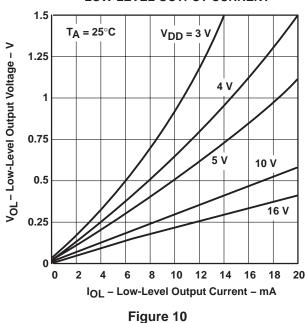


Figure 9





# LOW-LEVEL OUTPUT VOLTAGE vs

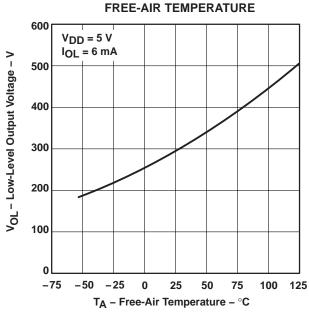


Figure 11

<sup>†</sup> Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



#### TYPICAL CHARACTERISTICS<sup>†</sup>

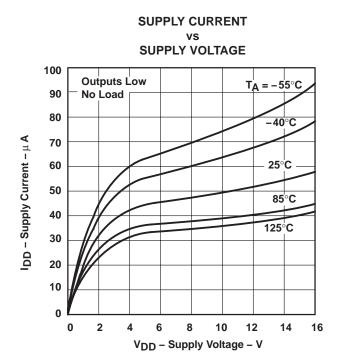
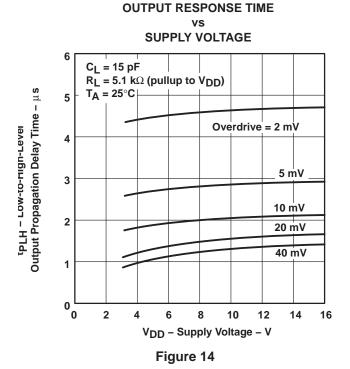


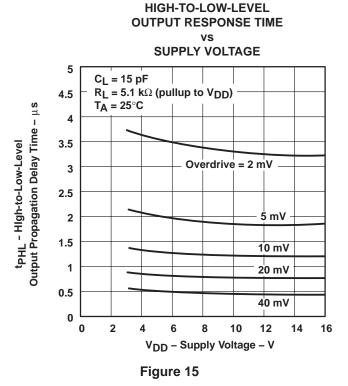
Figure 12

LOW-TO-HIGH-LEVEL



**SUPPLY CURRENT** FREE-AIR TEMPERATURE 80  $V_{DD} = 5 V$ No Load 70 60 IDD - Supply Current - μ A 50 **Outputs Low** 40 30 **Outputs High** 20 10 -75 -50 -25 50 100 125 25 75 T<sub>A</sub> - Free-Air Temperature - °C

Figure 13



<sup>†</sup>Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



#### TYPICAL CHARACTERISTICS

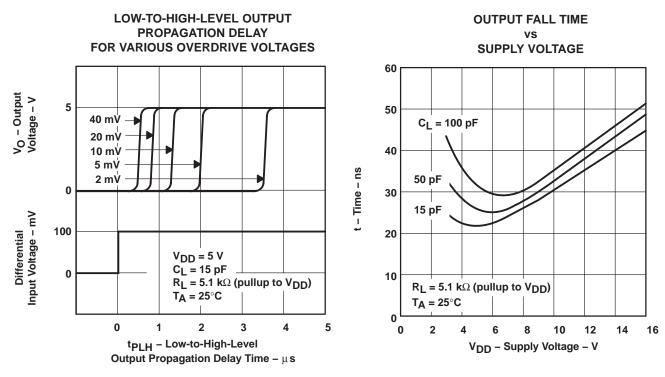


Figure 16 Figure 17

#### HIGH-TO-LOW-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS OVERDRIVE VOLTAGES

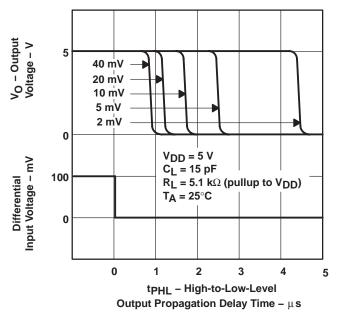


Figure 18



#### APPLICATION INFORMATION

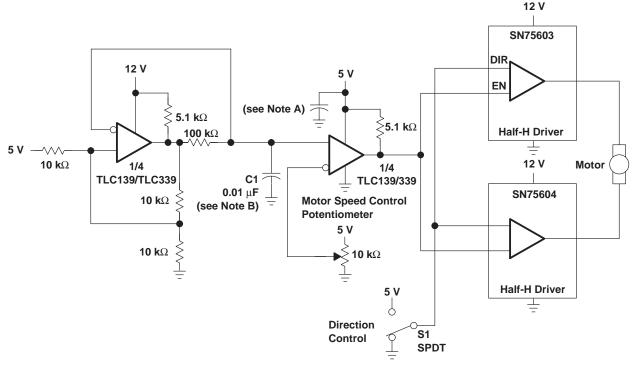
The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device is not damaged as long as the input current is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at  $25^{\circ}$ C with  $V_{DD} = 5$  V, both inputs must remain between -0.2 V and 4 V to assure proper device operation. To assure reliable operation, the supply should be decoupled with a capacitor (0.1  $\mu$ F) positioned as close to the device as possible.

The output and supply currents require close observation since the TLC139/TLC339 does not provide current protection. For example, each output can source or sink a maximum of 20 mA; however, the total current to ground has an absolute maximum of 60 mA. This prohibits sinking 20 mA from each of the four outputs simultaneously since the total current to ground would be 80 mA.

The TLC139 and TLC339 have internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, exercise care when handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

**Table of Applications** 

	FIGURE
Pulse-width-modulated motor speed controller	19
Enhanced supply supervisor	20
Two-phase nonoverlapping clock generator	21



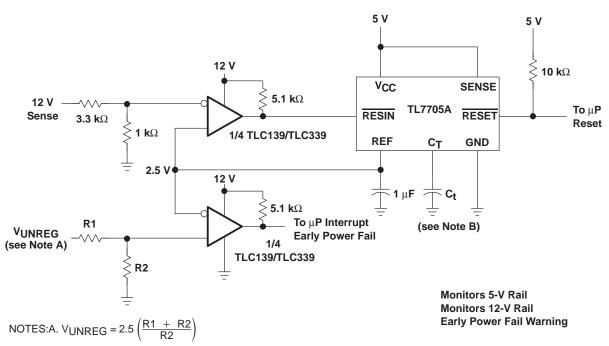
NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.

B. Select C1 for change in oscillator frequency.

Figure 19. Pulse-Width-Modulated Motor Speed Controller



#### TYPICAL APPLICATION DATA



B. The value of C<sub>t</sub> determines the time delay of reset.

Figure 20. Enhanced Supply Supervisor

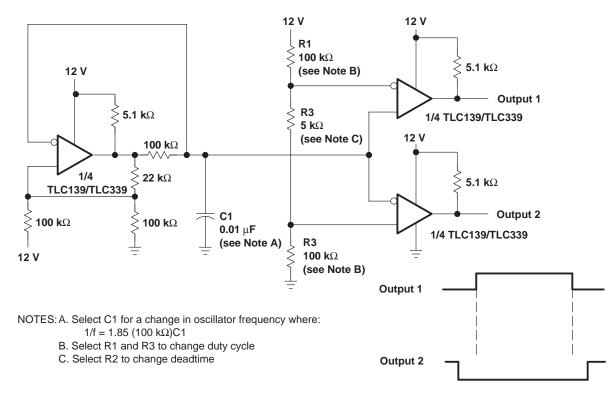


Figure 21. Two-Phase Nonoverlapping Clock Generator







17-Mar-2017

#### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87659022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87659022A TLC139MFKB	Samples
5962-8765902CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8765902CA TLC139MJB	Samples
5962-9555001NXD	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		QTLC139M	Samples
5962-9555001NXDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		QTLC139M	Samples
TLC139MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87659022A TLC139MFKB	Samples
TLC139MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8765902CA TLC139MJB	Samples
TLC339CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC339C	Samples
TLC339CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC339C	Samples
TLC339CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC339C	Samples
TLC339CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC339C	Samples
TLC339CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC339CN	Samples
TLC339CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC339CN	Samples
TLC339CNSR	ACTIVE	so	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC339	Samples
TLC339CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P339	Samples
TLC339CPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P339	Samples
TLC339CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P339	Samples





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Orderable Device	Status	Package Type	_	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
TLC339CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P339	Samples
TLC339ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC339I	Samples
TLC339IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC339I	Samples
TLC339IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC339I	Samples
TLC339IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC339I	Samples
TLC339IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC339IN	Samples
TLC339INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC339IN	Samples
TLC339IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC339I	Samples
TLC339IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC339I	Samples
TLC339IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC339I	Samples
TLC339MD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC339M	Samples
TLC339MDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM -55 to 125		TLC339M	Samples
TLC339MDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC339M	Samples
TLC339MDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM -55 to 125		TLC339M	Samples
TLC339MN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	TLC339MN	Samples

<sup>(1)</sup> The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.



#### PACKAGE OPTION ADDENDUM

17-Mar-2017

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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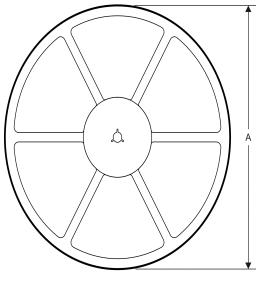
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## PACKAGE MATERIALS INFORMATION

14-Jul-2012 www.ti.com

#### TAPE AND REEL INFORMATION

#### **REEL DIMENSIONS**





#### **TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### TAPE AND REEL INFORMATION

\*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
5962-9555001NXDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC339CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC339CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TLC339CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC339IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC339IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC339MDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

www.ti.com 14-Jul-2012



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
5962-9555001NXDR	SOIC	D	14	2500	367.0	367.0	38.0
TLC339CDR	SOIC	D	14	2500	367.0	367.0	38.0
TLC339CNSR	SO	NS	14	2000	367.0	367.0	38.0
TLC339CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC339IDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC339IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC339MDR	SOIC	D	14	2500	367.0	367.0	38.0

# FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



#### **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
   Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
   Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



# D (R-PDSO-G14)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



# D (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
  - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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