16-Channel, Constant-Current LED Driver with Pre-Charge FET

Check for Samples: TLC59283

FEATURES

- **16-Channel, Constant-Current Sink Output with On and Off Control**
- **Constant-Current Sink Capability: 35 mA (V_{CC} ≤ 3.6 V), 45 mA (V_{CC} > 3.6 V)**
- **LED Power-Supply Voltage: Up to 10 V**
- **V_{CC} = 3 V to 5.5 V**
- **Constant-Current Accuracy:**
  - **Channel-to-Channel: ±1.4% (typ), ±3% (max)**
  - **Device-to-Device: ±2% (typ), ±4% (max)**
- **CMOS Logic Level I/O**
- **Data Transfer Rate: 35 MHz**
- **BLANK Pulse Width: 50 ns**
- **Pre-Charge FET for Ghosting Reduction**
- **Grouped Switching Delay for Noise Reduction**
- **Operating Temperature: –40°C to +85°C**

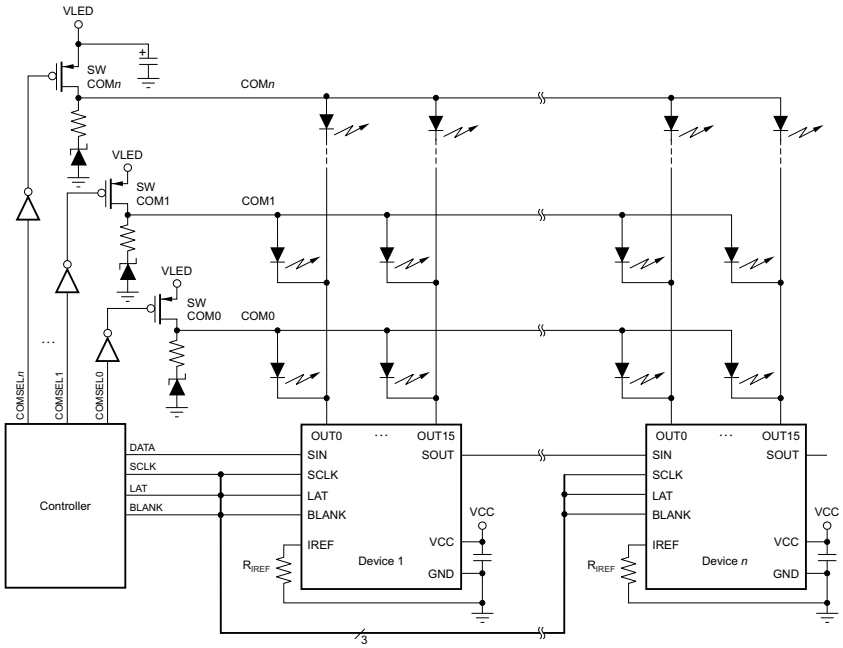
APPLICATIONS

- **Video Displays**
- **Message Boards**

DESCRIPTION

The TLC59283 is a 16-channel, constant-current sink light-emitting diode (LED) driver. Each channel can be individually controlled with a simple serial communications protocol that is compatible with 3.3-V or 5-V CMOS logic levels, depending on the operating VCC. When the serial data buffer is loaded, a LAT rising edge transfers the data to the OUT*n* outputs. The BLANK pin can be used to turn off all OUT*n* outputs during power-on and output data latching to prevent unwanted image displays during these times. The constant-current value of all 16 channels is set by a single external resistor.

Each constant-current output has a pre-charge field-effect transistor (FET) that can reduce ghosting on the multiplexing (dynamic) drive LED display. Multiple TLC59283s can be cascaded together to control additional LEDs from the same processor.



Typical Application Circuit (Multiple Daisy-Chained TLC59283s)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE AND ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLC59283	SSOP-24 and QSOP-24	TLC59283DBQR	Tape and Reel, 2500
		TLC59283DBQ	Tube, 50
TLC59283	QFN-24	TLC59283RGER	Tape and Reel, 3000
		TLC59283RGE	Tape and Reel, 250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating free-air temperature range, unless otherwise noted.

			VALUE		UNIT
			MIN	MAX	
Voltage	V_{CC}	Supply	–0.3	+6	V
	V_{IN}	Input range, SIN, SCLK, LAT, BLANK, IREF	–0.3	V_{CC} + 0.3	V
	V_{OUT}	Output range, SOUT	–0.3	V_{CC} + 0.3	V
		Output range, OUT0 to OUT15	–0.3	+11	V
Current	I_{OUT}	Output (dc), OUT0 to OUT15		+50	mA
Temperature	$T_{J(MAX)}$	Operating junction		+150	°C
	T_{stg}	Storage range	–55	+150	°C
Electrostatic discharge ratings	ESD	Human body model (HBM)		3000	V
		Charged device model (CDM)		2000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TLC59283		UNITS
		DBQ	RGE	
		24 PINS	24 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	91.5	42.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	55.2	55.3	
θ_{JB}	Junction-to-board thermal resistance	44.9	21.7	
ψ_{JT}	Junction-to-top characterization parameter	16.8	1.9	
ψ_{JB}	Junction-to-board characterization parameter	44.5	21.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	8.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

At T_A = –40°C to +85°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	TLC59283 MIN	TLC59283 MAX	UNIT
DC CHARACTERISTICS (V_{CC} = 3 V to 5.5 V)						
V_{CC}	Supply voltage			3	5.5	V
V_O	Voltage applied to output		OUT0 to OUT15		10	V
V_{IH}	Input voltage	High	SIN, SCLK, LAT, BLANK	0.7 × V_{CC}	V_{CC}	V
V_{IL}		Low	SIN, SCLK, LAT, BLANK	GND	0.3 × V_{CC}	V
I_{OH}	Output current	High	SOUT		–2	mA
I_{OL}		Low	SOUT		2	mA
I_{OLC}	Constant output sink current		OUT0 to OUT15, 3 V ≤ V_{CC} ≤ 3.6 V	2	35	mA
			OUT0 to OUT15, 3.6 V < V_{CC} ≤ 5.5 V	2	45	mA
T_A	Temperature range	Operating free-air		–40	+85	°C
T_J		Operating junction		–40	+125	°C
AC CHARACTERISTICS (V_{CC} = 3 V to 5.5 V)						
$f_{CLK\ (SCLK)}$	Data shift clock frequency		SCLK		35	MHz
t_{WH0}	Pulse duration		SCLK	10		ns
t_{WL0}			SCLK	10		ns
t_{WH1}			LAT	20		ns
t_{WH2}			BLANK	100		ns
t_{WL2}			BLANK	50		ns
t_{SU0}	Setup time		SIN↑↓ – SCLK↑	4		ns
t_{SU1}			LAT↓ – SCLK↑	10		ns
t_{H0}	Hold time		SIN↑↓ – SCLK↑	4		ns
t_{H1}			LAT↓ – SCLK↑	10		ns

ELECTRICAL CHARACTERISTICS

All minimum and maximum specifications are at T_A = –40°C to +85°C and V_{CC} = 3 V to 5.5 V, unless otherwise noted. Typical specifications are at T_A = +25°C and V_{CC} = 3.3 V.

PARAMETER			TEST CONDITIONS		TLC59283 MIN	TLC59283 TYP	TLC59283 MAX	UNIT
V_{OH}	Output voltage	High	I_{OH} = –2 mA at SOUT		V_{CC} – 0.4		V_{CC}	V
V_{OL}		Low	I_{OL} = 2 mA at SOUT				0.4	V
V_{PCHG}	Pre-charged voltage		I_O = –10 µA		V_{CC} – 2.0	V_{CC} – 1.4	V_{CC} – 0.8	V
V_{IREF}	Reference voltage output		R_{IREF} = 1.5 kΩ, T_A = +25°C			1.208		V
I_{IN}	Input current		V_{IN} = V_{CC} or GND at SIN and SCLK		–1		1	µA
I_{CC0}	Supply current (V_{CC})		SIN, SCLK, LAT = GND, BLANK = V_{OUTn} = V_{CC}, R_{IREF} = open			1	2	mA
I_{CC1}			SIN, SCLK, LAT = GND, BLANK = V_{OUTn} = V_{CC}, R_{IREF} = 3 kΩ (I_{OUT} = 17.6 mA target)			3	4	mA
I_{CC2}			All OUT*n* = ON, SIN, SCLK, LAT, BLANK = GND, V_{OUTn} = 0.8 V, R_{IREF} = 3 kΩ			7	9	mA
I_{CC3}			All OUT*n* = ON, SIN, SCLK, LAT, BLANK = GND, V_{OUTn} = 0.8 V, R_{IREF} = 1.5 kΩ (I_{OUT} = 35.3 mA target)			8	11	mA
I_{OLC}	Constant output current		All OUT*n* = ON, V_{OUTn} = V_{OUTfix} = 0.8 V, R_{IREF} = 1.5 kΩ, T_A = +25°C (see Figure 8)		32.9	35.3	37.7	mA
I_{OLKG0}	Output leakage current		All OUT*n* = OFF, V_{OUTn} = V_{OUTfix} = 10 V, BLANK = V_{CC}, R_{IREF} = 1.5 kΩ (see Figure 8)	T_J = +25°C			0.1	µA
				T_J = +85°C			0.2	µA
				T_J = +125°C		0.07	0.5	µA
ΔI_{OLC0}	Constant-current error	Channel-to-channel(1)	All OUT*n* = ON, V_{OUTn} = V_{OUTfix} = 0.8 V, R_{IREF} = 1.5 kΩ, T_A = +25°C (see Figure 8)			±1.4	±3	%
ΔI_{OLC1}		Device-to-device(2)	All OUT*n* = ON, V_{OUTn} = V_{OUTfix} = 0.8 V, R_{IREF} = 1.5 kΩ, T_A = +25°C (see Figure 8)			±2	±4	%
ΔI_{OLC2}	Line regulation(3)		All OUT*n* = ON, V_{OUTn} = V_{OUTfix} = 0.8 V, R_{IREF} = 1.5 kΩ, V_{CC} = 3 V to 5.5 V			±0.05	±1	%/V
ΔI_{OLC3}	Load regulation(4)		All OUT*n* = ON, V_{OUTn} = 0.8 V to 3 V, V_{OUTfix} = 0.8 V, R_{IREF} = 1.5 kΩ			±0.5	±1	%/V
R_{PUP}	Resistor	Pull-up	BLANK		250	500	750	kΩ
R_{PDWN}		Pull-down	LAT		250	500	750	kΩ
R_{PCHG}	Pre-charge FET on-resistance		VCC = 5.0 V, V_{OUTn} = 0 V, OUT0 to OUT15, BLANK = V_{CC}, T_A = +25°C			3	6	kΩ

(1) The deviation of each output from the average of OUT0 to OUT15 constant-current. Deviation is calculated by the formula:

$$\Delta\ (\%) = \left(\frac{I_{OUTn}}{\frac{(I_{OUT0} + I_{OUT1} + \ldots + I_{OUT14} + I_{OUT15})}{16}} - 1 \right) \times 100$$

(2) The deviation of the OUT0 to OUT15 constant-current average from the ideal constant-current value. Deviation is calculated by the following formula:

$$\Delta\ (\%) = \left(\frac{\frac{(I_{OUT0} + I_{OUT1} + \ldots I_{OUT14} + I_{OUT15})}{16} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

Ideal current is calculated by the formula:

$$I_{OUT(IDEAL)} = 43.8 \times \left(\frac{1.208\ V}{R_{IREF}} \right)$$

(3) Line regulation is calculated by this equation:

$$\Delta\ (\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{CC} = 5.5\ V) - (I_{OUTn} \text{ at } V_{CC} = 3\ V)}{(I_{OUTn} \text{ at } V_{CC} = 3\ V)} \right) \times \frac{100}{5.5\ V - 3\ V}$$

(4) Load regulation is calculated by the equation:

$$\Delta\ (\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{OUTn} = 3\ V) - (I_{OUTn} \text{ at } V_{OUTn} = 1\ V)}{(I_{OUTn} \text{ at } V_{OUTn} = 1\ V)} \right) \times \frac{100}{3\ V - 1\ V}$$

SWITCHING CHARACTERISTICS

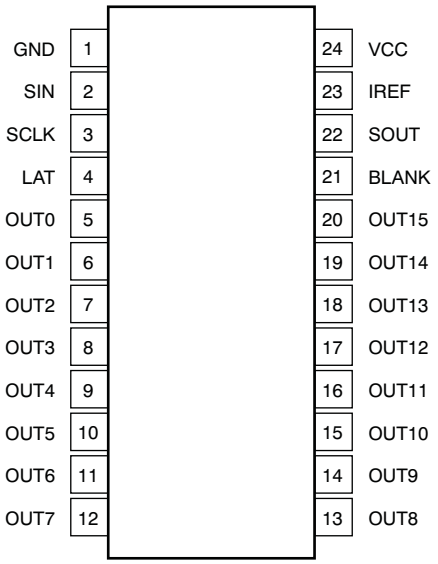
All minimum and maximum specifications are at T_A = –40°C to +85°C, V_{CC} = 3 V to 5.5 V, C_L = 15 pF, R_L = 110 Ω, R_{IREF} = 1.5 kΩ, and V_{LED} = 5.0 V, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	TLC59283			UNIT
			MIN	TYP	MAX	
t_{R0}	Rise time	SOUT (see Figure 7)		3	10	ns
t_{R1}		OUT*n* (see Figure 6)		44		ns
t_{F0}	Fall time	SOUT (see Figure 7)		3	10	ns
t_{F1}		OUT*n* (see Figure 6)		44		ns
t_{D0}	Propagation delay time	SCLK↑ to SOUT↑↓		11	20	ns
t_{D1}		LAT↑ or BLANK↑↓ to OUT0 on or off, T_A = +25°C		60	100	ns
t_{D2}		Grouped OUT*n* on or off to next group on or off, T_A = +25°C		2		ns
t_{ON_ERR}	Output on-time error(1)	Output on or off latch data = all '1', 50-ns BLANK GND level pulse, V_{CC} = 3.3 V, T_A = +25°C	–45		45	ns

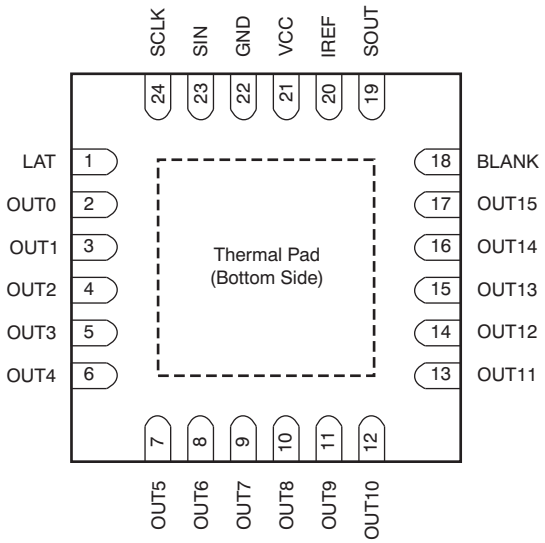
(1) Output on-time error (t_{ON_ERR}) is calculated by the formula: t_{ON_ERR} (ns) = t_{OUT_ON} – BLANK low level one-shot pulse width (t_{WL2}). t_{OUT_ON} indicates the actual on-time of the constant-current output.

PIN CONFIGURATIONS

DBQ PACKAGE
SSOP-24 AND QSOP-24
(TOP VIEW)



RGE PACKAGE
QFN-24
(TOP VIEW)

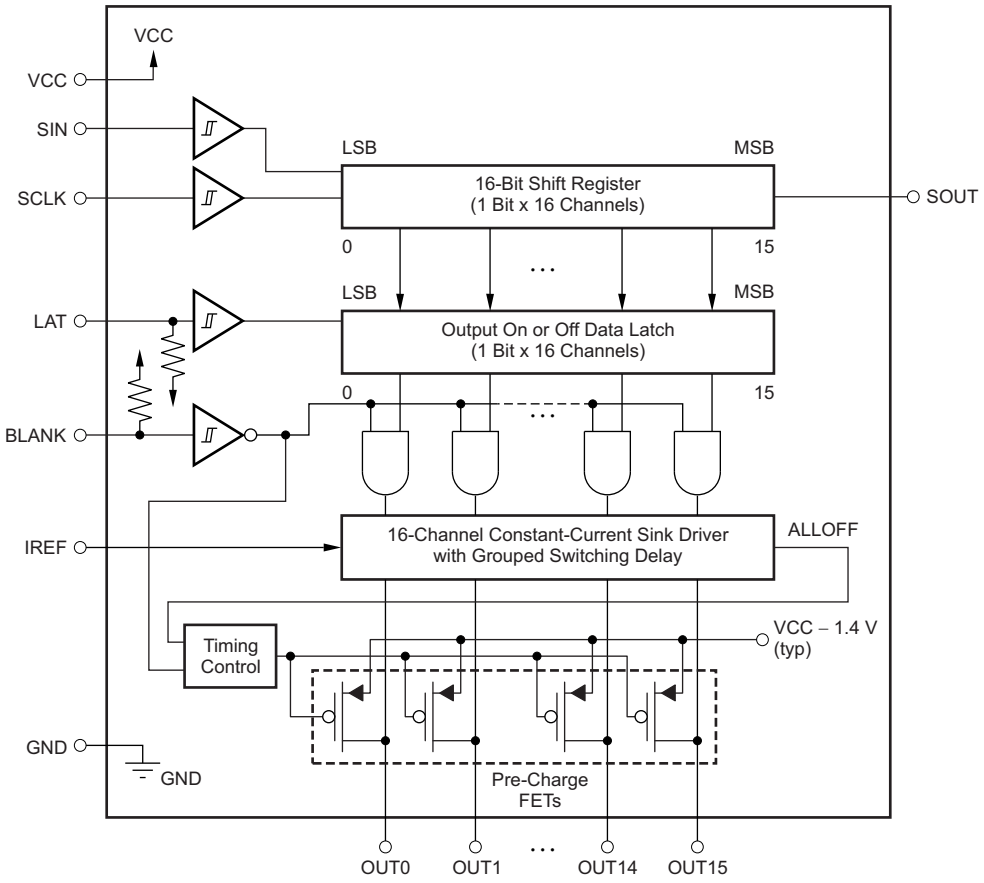


NOTE: Thermal pad is not connected to GND internally. The thermal pad must be connected to GND via the printed circuit board (PCB) pattern.

PIN DESCRIPTIONS

PIN			I/O	DESCRIPTION
NAME	NUMBER			
	DBQ	RGE		
BLANK	21	18	I	All outputs empty (blank); Schmitt buffer input. When BLANK is high, all constant-current outputs (OUT0 to OUT15) are forced off and all pre-charge FETs are turned on. When BLANK is low, all constant-current outputs are controlled by the data in the output on or off data latch and all pre-charge FETs are turned off. This pin is internally pulled up to V_{CC} with a 500-kΩ (typ) resistor.
GND	1	22	—	Power ground
IREF	23	20	I/O	Constant-current value setting, the OUT0 to OUT15 sink constant-current outputs are set to the desired values by connecting an external resistor between IREF and GND.
LAT	4	1	I	Level-triggered latch; Schmitt buffer input. The data in the 16-bit shift register continue to transfer to the output on or off data latch while LAT is high. Therefore, if the data in the 16-bit shift register are changed when LAT is high, the data in the data latch are also changed. The data in the data latch are held when LAT is low. This pin is internally pulled down to GND with a 500-kΩ (typ) resistor.
OUT0	5	2	O	Constant-current output. Each output can be tied together with others to increase the constant-current. Different voltages can be applied to each output.
OUT1	6	3	O	Constant-current output
OUT2	7	4	O	Constant-current output
OUT3	8	5	O	Constant-current output
OUT4	9	6	O	Constant-current output
OUT5	10	7	O	Constant-current output
OUT6	11	8	O	Constant-current output
OUT7	12	9	O	Constant-current output
OUT8	13	10	O	Constant-current output
OUT9	14	11	O	Constant-current output
OUT10	15	12	O	Constant-current output
OUT11	16	13	O	Constant-current output
OUT12	17	14	O	Constant-current output
OUT13	18	15	O	Constant-current output
OUT14	19	16	O	Constant-current output
OUT15	20	17	O	Constant-current output
SCLK	3	24	I	Serial data shift clock; Schmitt buffer input. All data in the 16-bit shift register are shifted toward the MSB by a 1-bit SCLK synchronization.
SIN	2	23	I	Serial data input for driver on or off control; Schmitt buffer input. When SIN is high, the LSB is set to '1' for only one SCLK input rising edge. If two SCLK rising edges are input while SIN is high, then the 16-bit shift register LSB and LSB+1 are set to '1'. When SIN is low, the LSB is set to '0' at the SCLK input rising edge.
SOUT	22	19	O	Serial data output. This output is connected to the 16-bit shift register MSB. SOUT data changes at the SCLK rising edge.
VCC	24	21	—	Power-supply voltage

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION

PIN-EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

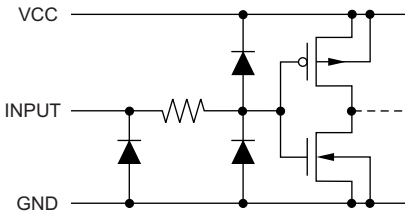


Figure 1. SIN and SCLK

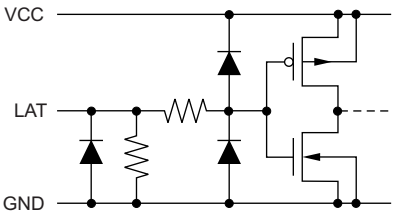


Figure 2. LAT

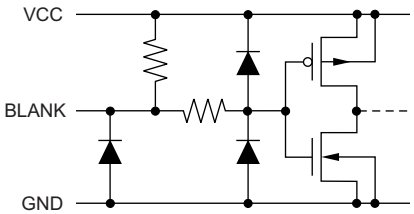


Figure 3. BLANK

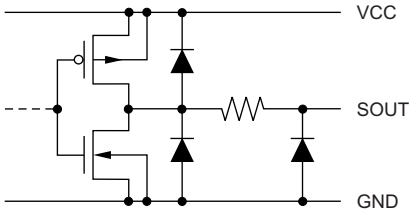
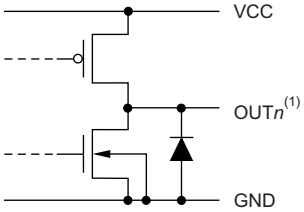


Figure 4. SOUT



(1) n = 0 to 15.

Figure 5. OUT0 Through OUT15

TEST CIRCUITS

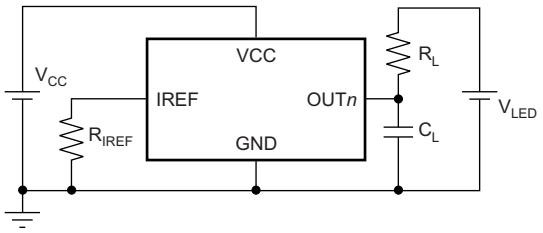


Figure 6. OUT*n* Rise and Fall Time Test Circuit

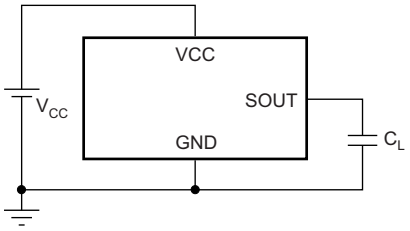


Figure 7. SOUT Rise and Fall Time Test Circuit

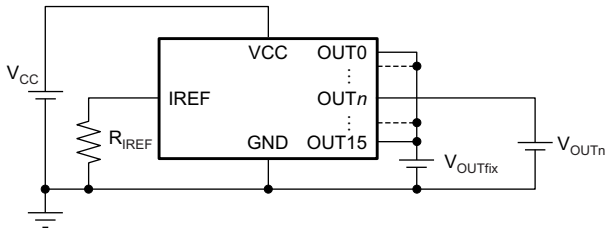
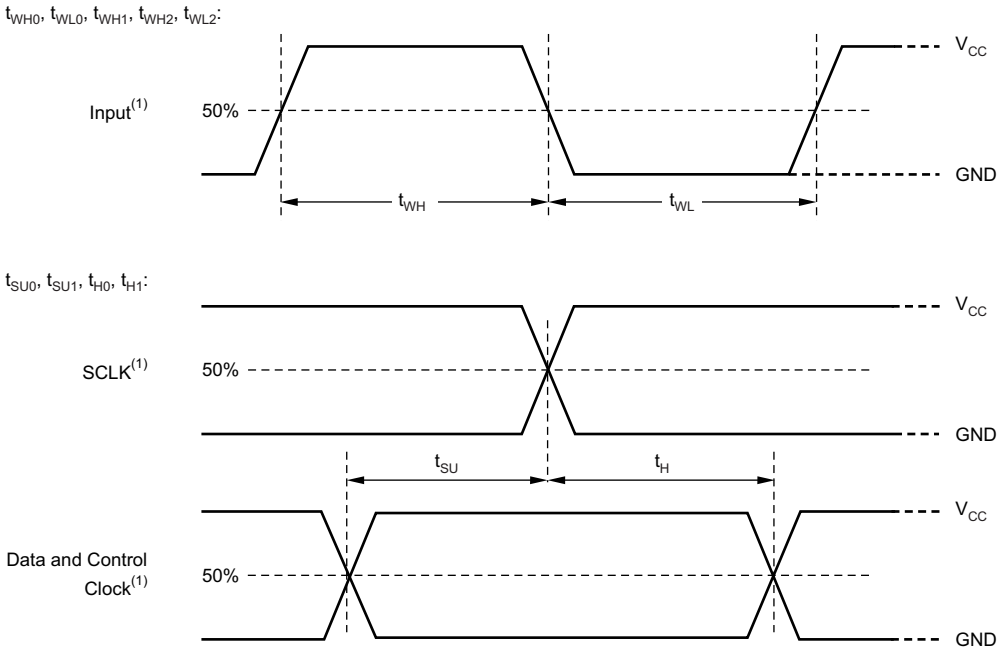


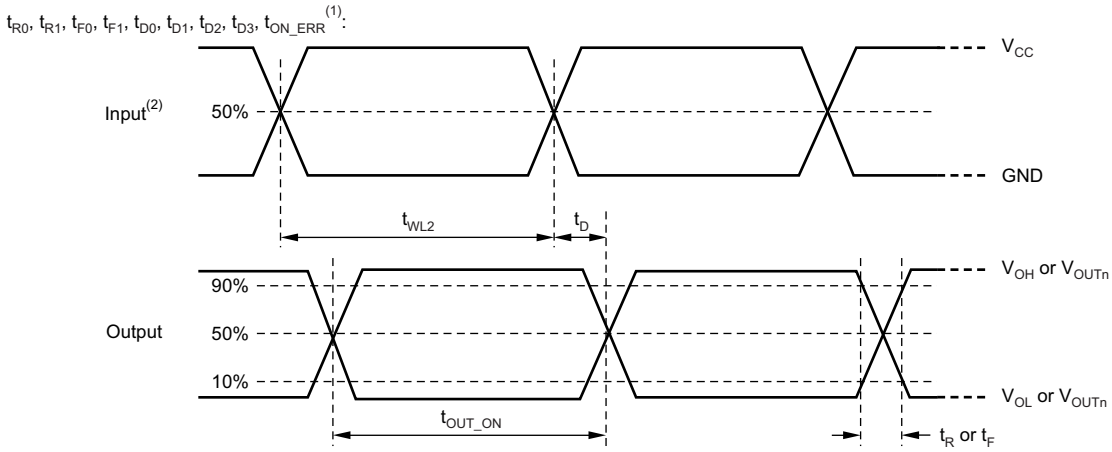
Figure 8. OUT*n* Constant-Current Test Circuit

TIMING DIAGRAMS



(1) Input pulse rise and fall time is 1 ns to 3 ns.

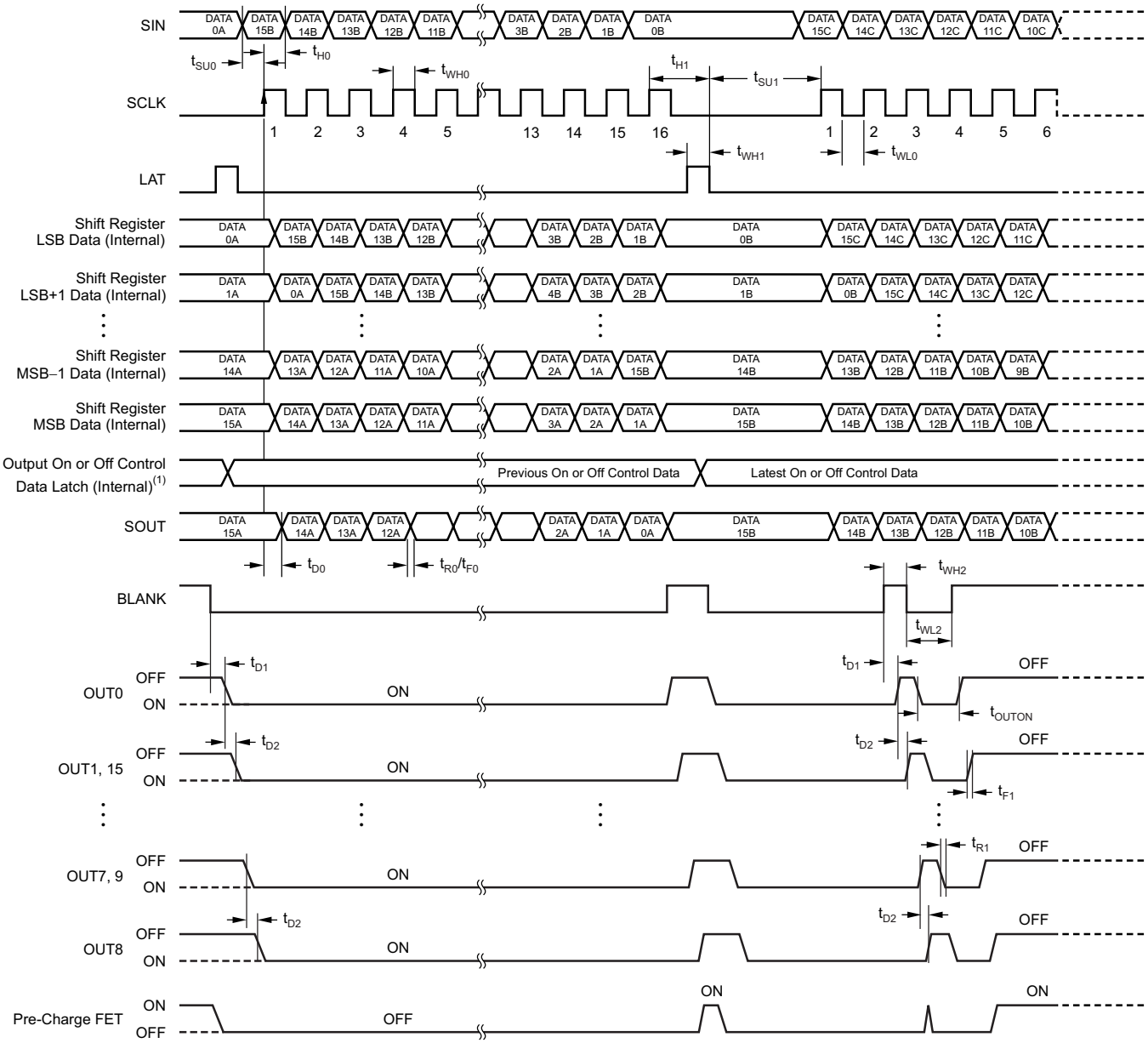
Figure 9. Input Timing Diagram



(1) t_{ON_ERR} is calculated by $t_{OUTON} - t_{WL2}$.

(2) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 10. Output Timing Diagram



(1) Output on or off data = FFFFh.

(2) $t_{ON\_ERR} = t_{OUTON} - t_{WL2}$.

Figure 11. Data Write and Output On or Off Timing Diagram

TYPICAL CHARACTERISTICS

At T_A = +25°C and V_{CC} = 3.3 V, unless otherwise noted.

REFERENCE RESISTOR vs OUTPUT CURRENT

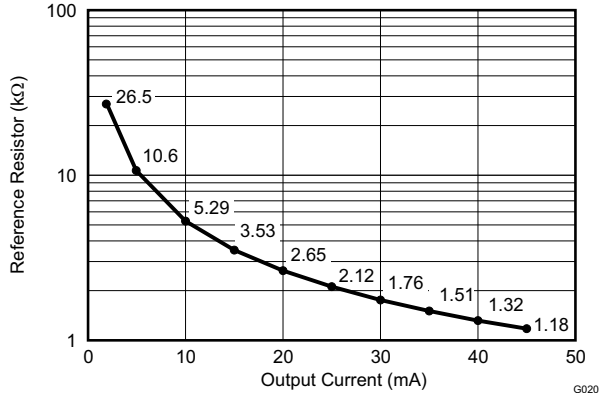


Figure 12.

OUTPUT CURRENT vs OUTPUT VOLTAGE (VCC = 3.3 V)

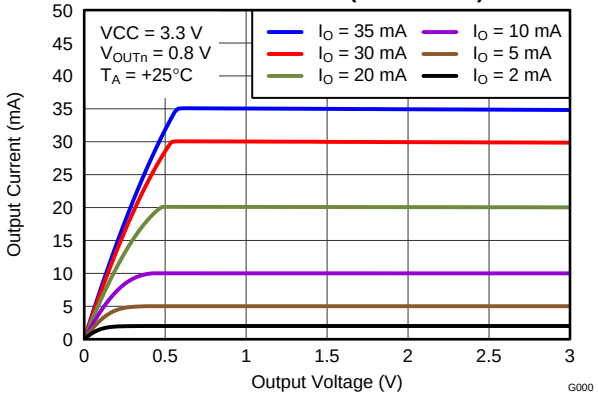


Figure 13.

OUTPUT CURRENT vs OUTPUT VOLTAGE (VCC = 5.0 V)

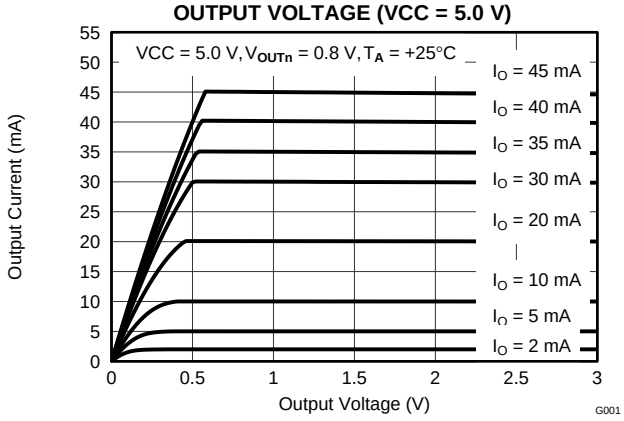


Figure 14.

OUTPUT CURRENT vs OUTPUT VOLTAGE (VCC = 3.3 V, Magnified)

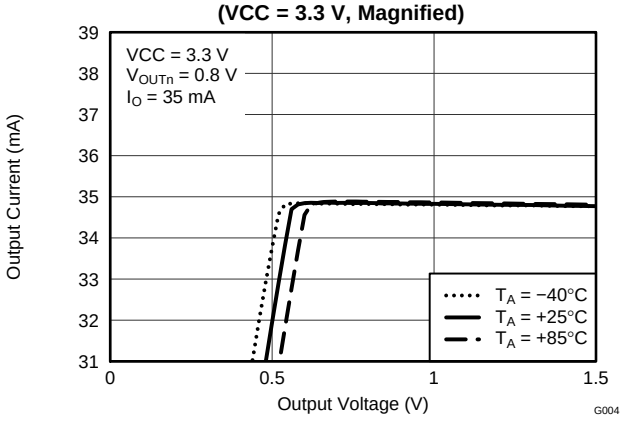


Figure 15.

OUTPUT CURRENT vs OUTPUT VOLTAGE (VCC = 5.0 V, Magnified)

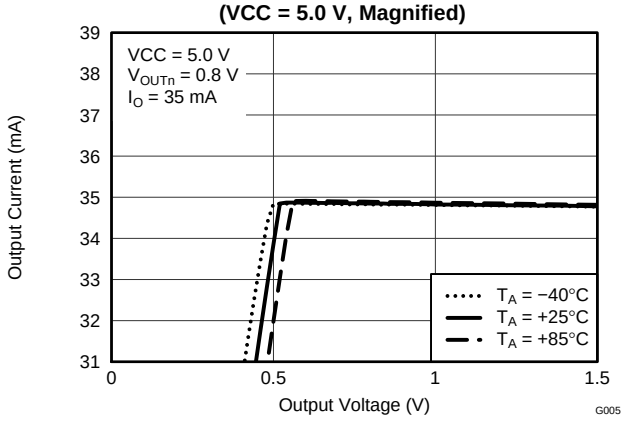


Figure 16.

ΔI_{OLC} vs AMBIENT TEMPERATURE

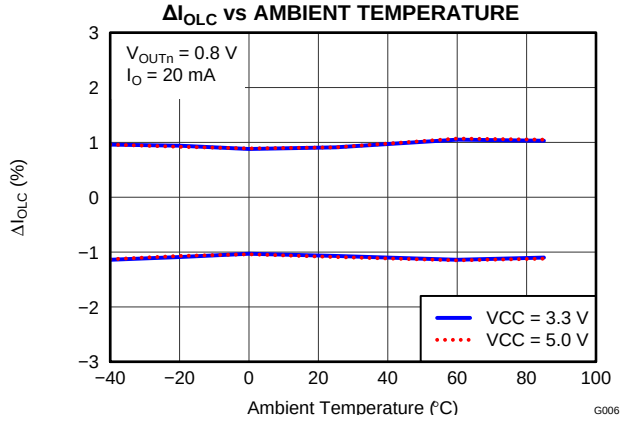


Figure 17.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{CC} = 3.3 V, unless otherwise noted.

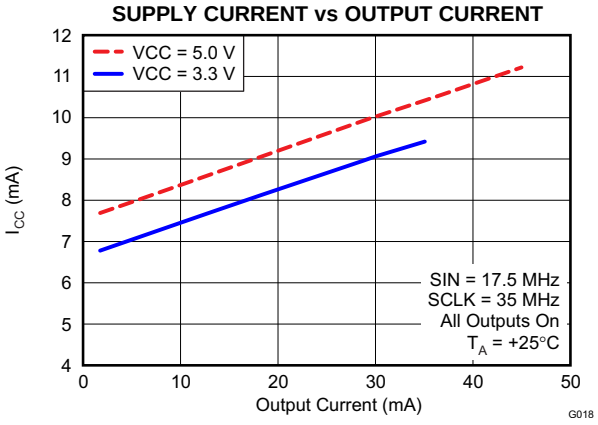


Figure 18.

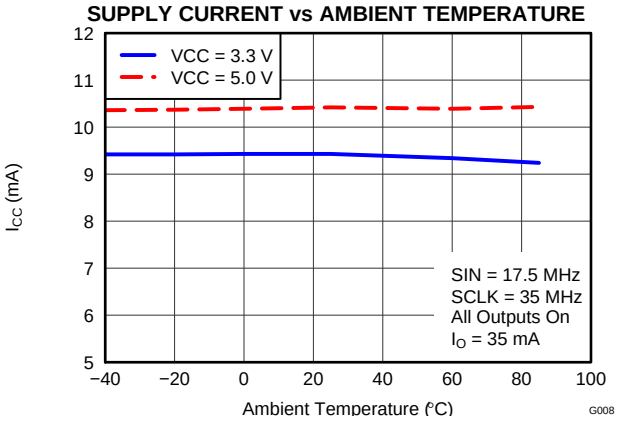


Figure 19.

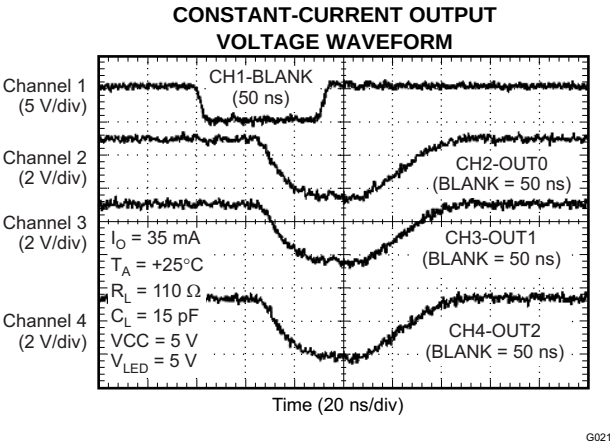


Figure 20.

DETAILED DESCRIPTION

CONSTANT SINK CURRENT VALUE SETTING

The constant-current values are determined by an external resistor (R_{IREF}) placed between IREF and GND. The resistor (R_{IREF}) value is calculated by Equation 1.

$$R_{IREF}\ (k\Omega) = \frac{V_{IREF}\ (V)}{I_{OLC}\ (mA)} \times 43.8 \quad (1)$$

Where:

V_{IREF} = the internal reference voltage on the IREF pin (typically 1.208 V)

I_{OLC} must be set in the range of 2 mA to 35 mA when V_{CC} is less than 3.6 V. Also, when V_{CC} is equal to 3.6 V or greater, I_{OLC} must be set in the range of 2 mA to 45 mA. The constant sink current characteristic for the external resistor value is illustrated in Figure 12. Table 1 describes the constant-current output versus external resistor value.

Table 1. Constant-Current Output versus External Resistor Value

I_{OLC} (mA)	R_{IREF} (kΩ, Typical)
45 (V_{CC} > 3.6 V only)	1.18
40 (V_{CC} > 3.6 V only)	1.32
35	1.51
30	1.76
25	2.12
20	2.65
15	3.53
10	5.29
5	10.6
2	26.5

CONSTANT-CURRENT DRIVER ON OR OFF CONTROL

When BLANK is low, the corresponding output is turned on if the data in the on or off control data latch are '1' and remains off if the data are '0'. When BLANK is high, all outputs are forced off. This control is shown in Table 2.

Table 2. Output On or Off Control Data Truth Table

OUTPUT ON OR OFF DATA	CONSTANT-CURRENT OUTPUT STATUS
0	Off
1	On

When the device is initially powered on, the data in the 16-bit shift register and output on or off data latch are not set to default values. Therefore, the output on or off data must be written to the data latch before turning the constant-current output on. **BLANK should be high when powered on because the constant-current may be turned on as a result of random data in the output on or off data latch.**

REGISTER CONFIGURATION

The TLC59283 has a 16-bit shift register and an output on or off data latch. Both the shift register and data latch are 16 bits long and are used to turn the constant-current outputs on and off. Figure 21 shows the shift register and data latch configuration. The data at the SIN pin are shifted into the 16-bit shift register LSB at the rising edge of the SCLK pin; SOUT data change at the SCLK rising edge.

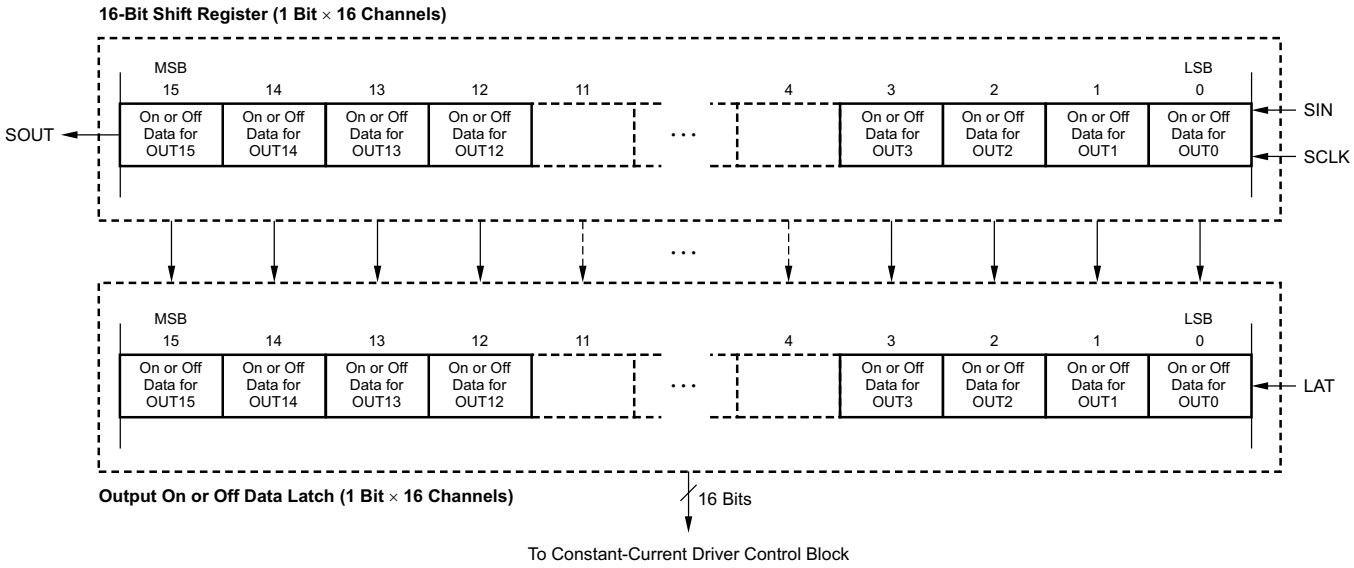


Figure 21. 16-Bit Shift Register and Output On or Off Data Latch Configuration

The output on or off data in the 16-bit shift register continue to transfer to the output on or off data latch while LAT is high. Therefore, if the data in the 16-bit shift register are changed when LAT is high, the data in the data latch are also changed. The data in the data latch are held when LAT is low. When the device initially powers on, the data in the output on or off shift register and latch are not set to default values; on or off control data must be written to the on or off control data latch before turning the constant-current output on. All constant-current outputs are forced off when BLANK is high. The OUT*n* on or off outputs are controlled by the data in the output on or off data latch. The writing data truth table and timing diagram are shown in Table 3 and Figure 22, respectively.

Table 3. Truth Table in Operation

SCLK	LAT	BLANK	SIN	OUT0…OUT7…OUT15	SOUT
↑	High	Low	Dn	Dn…Dn – 7…Dn – 15	Dn – 15
↑	Low	Low	Dn + 1	No change	Dn – 14
↑	High	Low	Dn + 2	Dn + 2…Dn – 5…Dn – 13	Dn – 13
↓	—	Low	Dn + 3	Dn + 2…Dn – 5…Dn – 13	Dn – 13
↓	—	High	Dn + 3	Off	Dn – 13

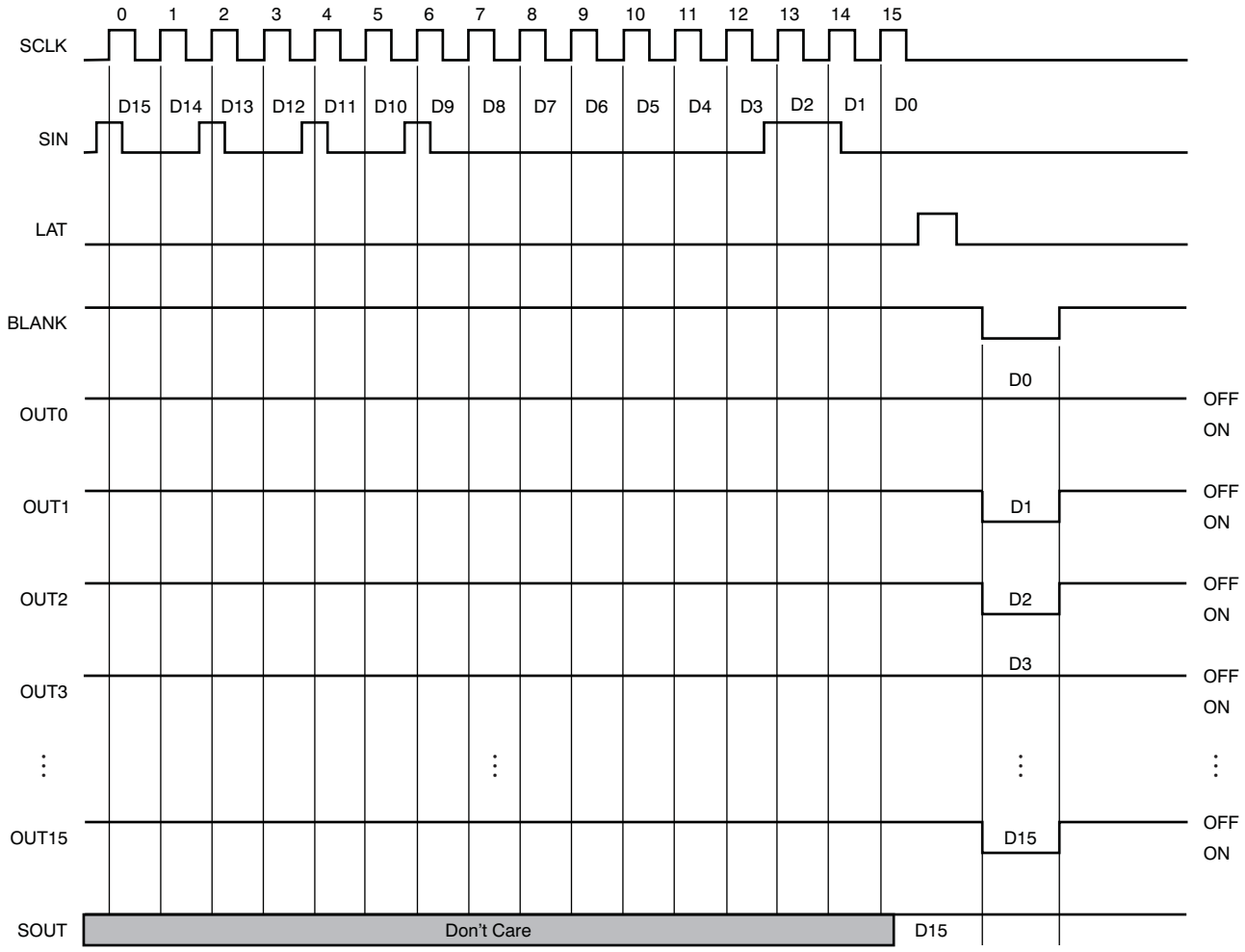


Figure 22. Operation Timing Diagram

NOISE REDUCTION

Large surge currents may flow through the device and board if all 16 outputs turn on or off simultaneously. These large current surges can induce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC59283 independently turns on or off the outputs for each group with a 1-ns (typ) delay time; see Figure 11. The 16 outputs are grouped into nine groups of either one or two outputs: group 1 (OUT0), group 2 (OUT1 and OUT15), group 3 (OUT2 and OUT14), group 4 (OUT3 and OUT13), group 5 (OUT4 and OUT12), group 6 (OUT5 and OUT11), group 7 (OUT6 and OUT10), group 8 (OUT7 and OUT9), and group 9 (OUT9). Both turn-on and turn-off times are delayed when BLANK transitions from low to high or high to low. Also when output-on and -off data are changed at the LAT rising edge while BLANK is low, both turn-on and turn-off times are delayed. However, the state of each output is controlled by the data in the output on or off data latch and the BLANK level.

Internal Pre-Charge FET

The internal pre-charge FET prevents ghosting of multiplexed LED modules. One cause of this phenomenon is the parasitic capacitance charging current of the constant-current outputs (OUT*n*) and PCB wiring connected to OUT*n* through the LED. One of the mechanisms is shown in Figure 23.

In Figure 23, the constant-current driver turns LED0-0 on at (1) and off at (2). After LED0-0 is turned off, the OUT0 voltage is pulled up to V_{CHG} by LED0-0. This OUT0 node has some parasitic capacitance (such as the constant-current driver output capacitance and the board layout capacitance shown as C0-2). After LED0-0 turns off, SWPMOS0 is turned off, SWNMOS0 is turned on for COM0, and COM0 is pulled down to GND. Because there is a parasitic capacitance between COM0 and OUT0, the OUT0 voltage is also pulled down to GND. Afterwards, SWPMOS1 is turned on for the next common line (COM1). When SWPMOS1 turns on, the OUT0 voltage is pulled up from the ground voltage to $V_{LED} - V_F$. The charge current (I_{CHRG}) flows to the parasitic capacitor (C0) through LED1-0, causing the LED to briefly turn on and creating a ghosting effect of LED1-0.

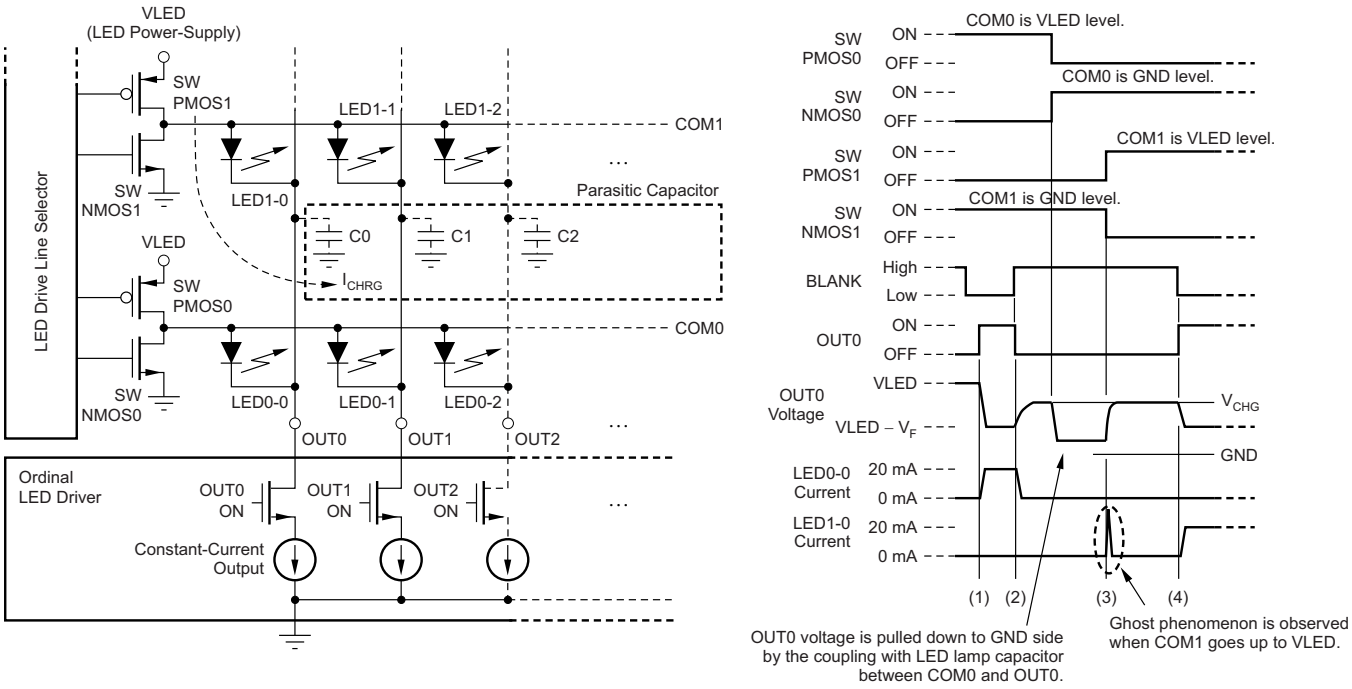


Figure 23. LED Ghost-Lighting Phenomenon Mechanism

The TLC59283 has an internal pre-charge FET to prevent ghosting, as shown in Figure 24. When a small delay after PWM control for a single common line completes, the FET pulls OUT*n* up to V_{CC}. The charge current does not flow to C0 through LED1-0 when SWMOS1 is turned on and the ghosting is eliminated at (3). However, depending on the LED anode voltage, the number of LEDs in series, the LED forward voltage, and the TLC59283 V_{CC} supply voltage, there may not be a great enough ghost-canceling effect.

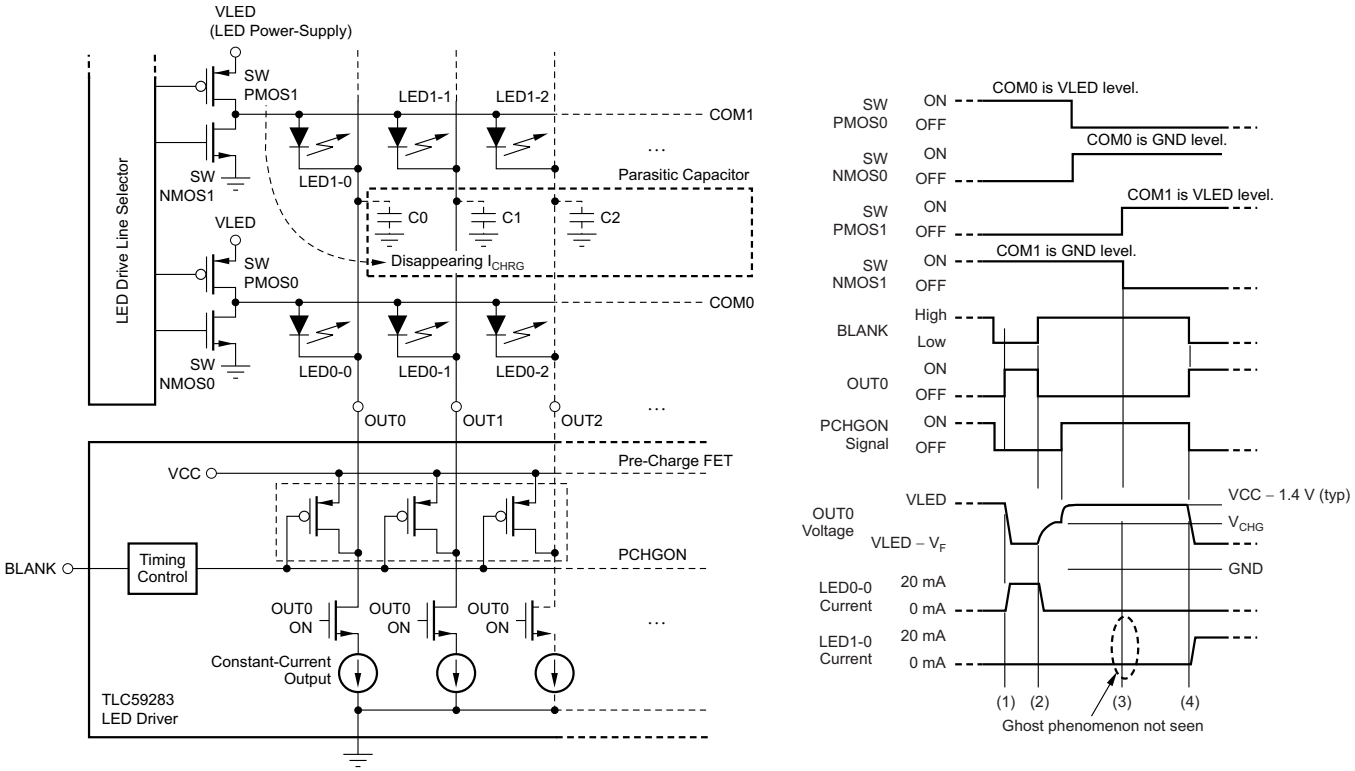


Figure 24. LED Ghost-Lighting Mechanism by Pre-Charge FET

HISTORY TABLE

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2012) to Revision B	Page
• Changed HBM ESD rating maximum specification in the Absolute Maximum Ratings table	2
• Changed I_{CC2} typical and maximum specifications in Electrical Characteristics table	4
• Changed I_{CC3} typical specification in Electrical Characteristics table	4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLC59283DBQ	ACTIVE	SSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC59283	Samples
TLC59283DBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC59283	Samples
TLC59283RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 59283	Samples
TLC59283RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 59283	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

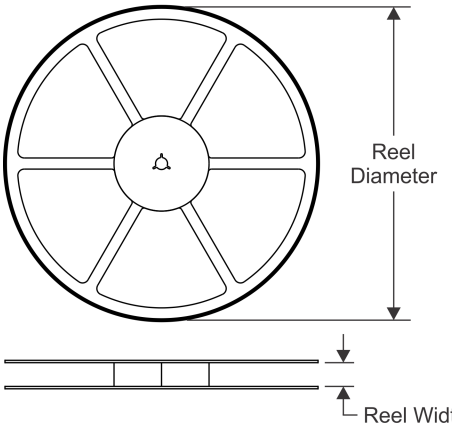
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

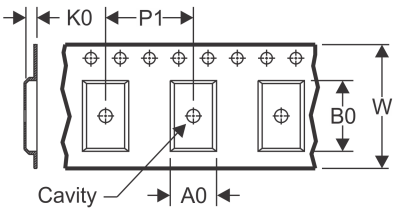
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

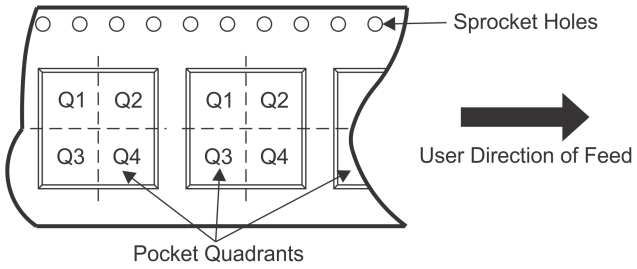


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

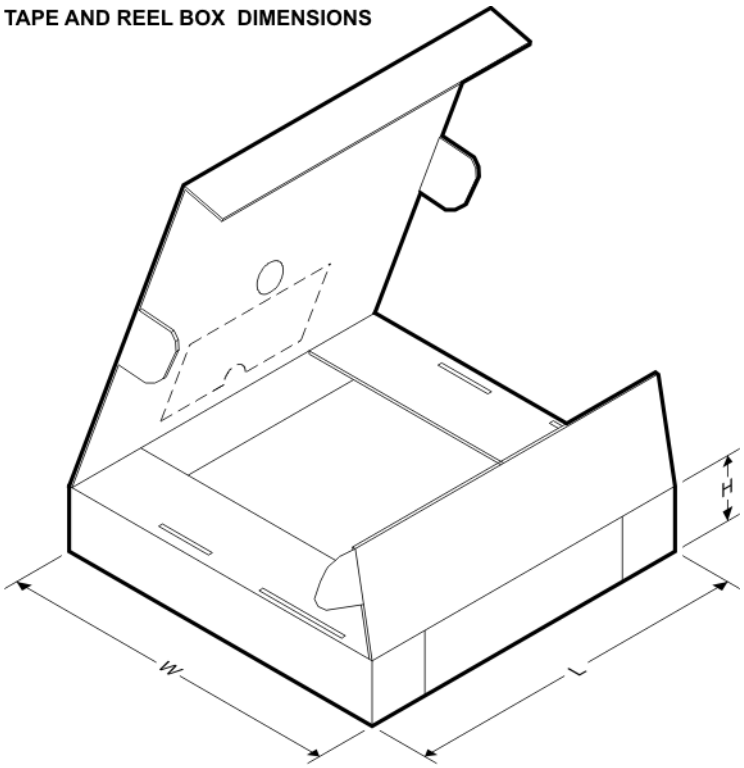
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59283DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC59283RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLC59283RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



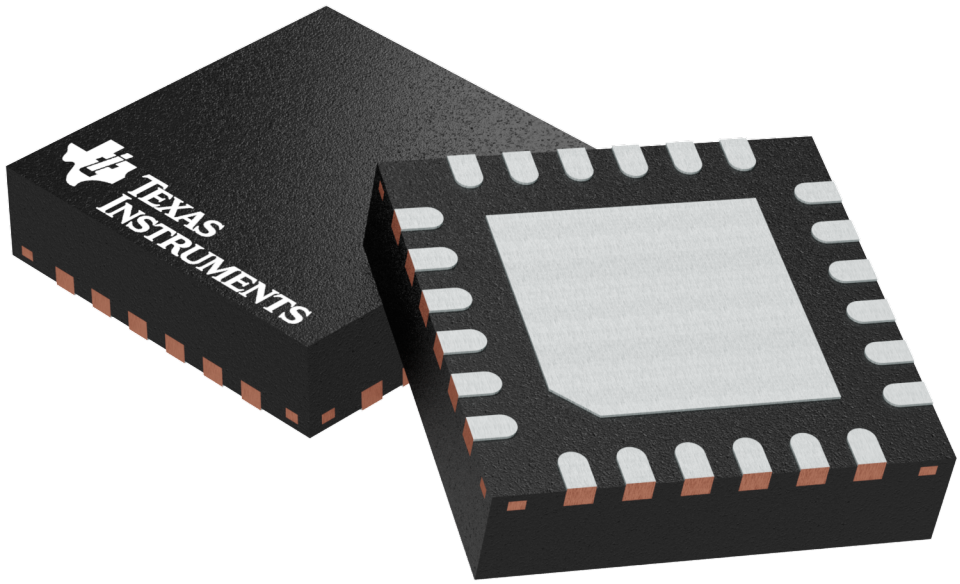
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59283DBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
TLC59283RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TLC59283RGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

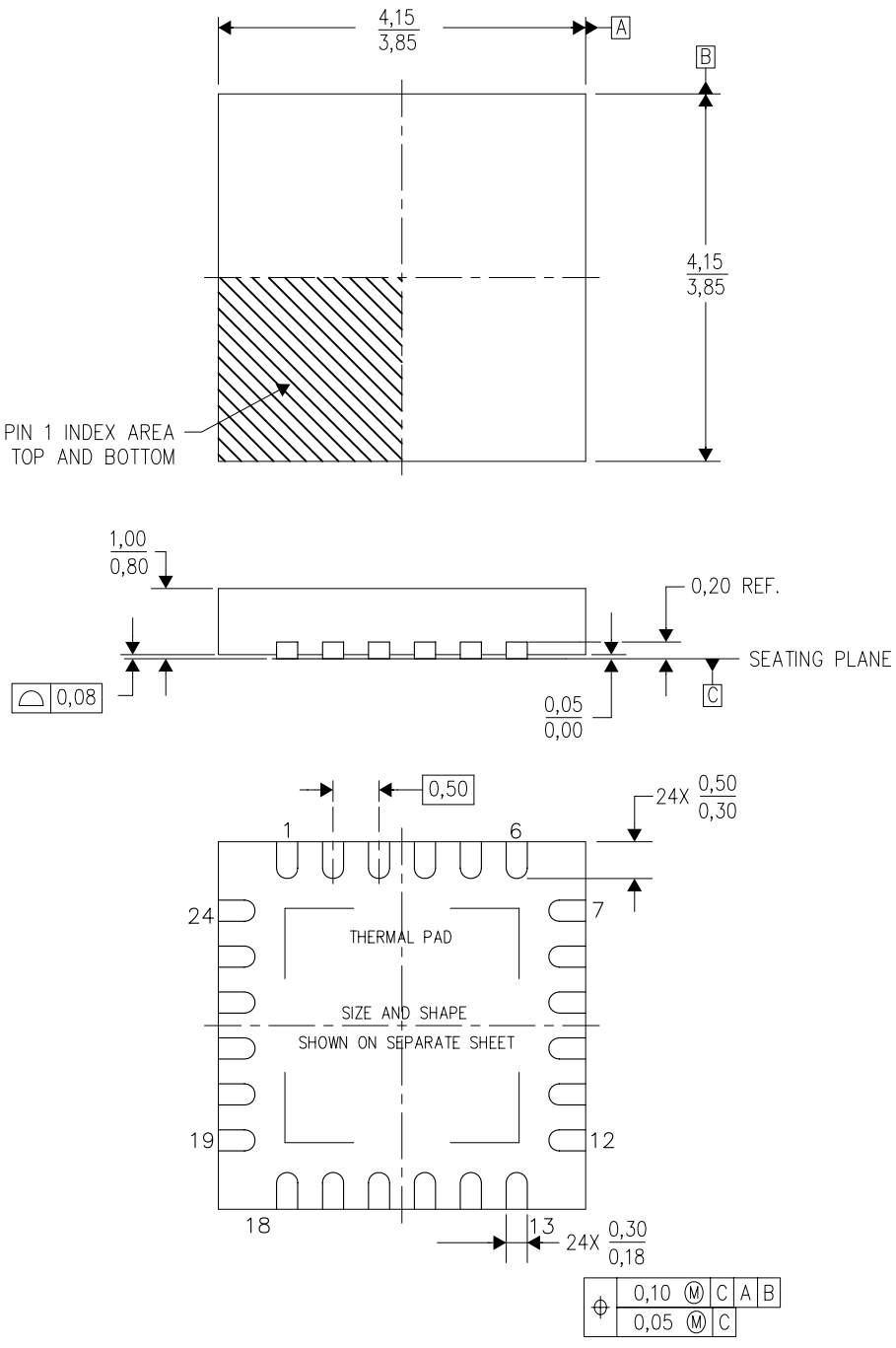
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

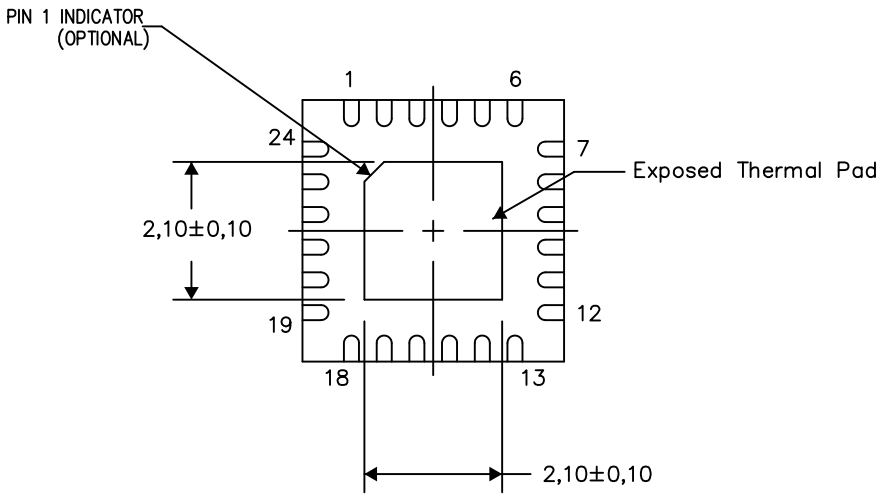
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



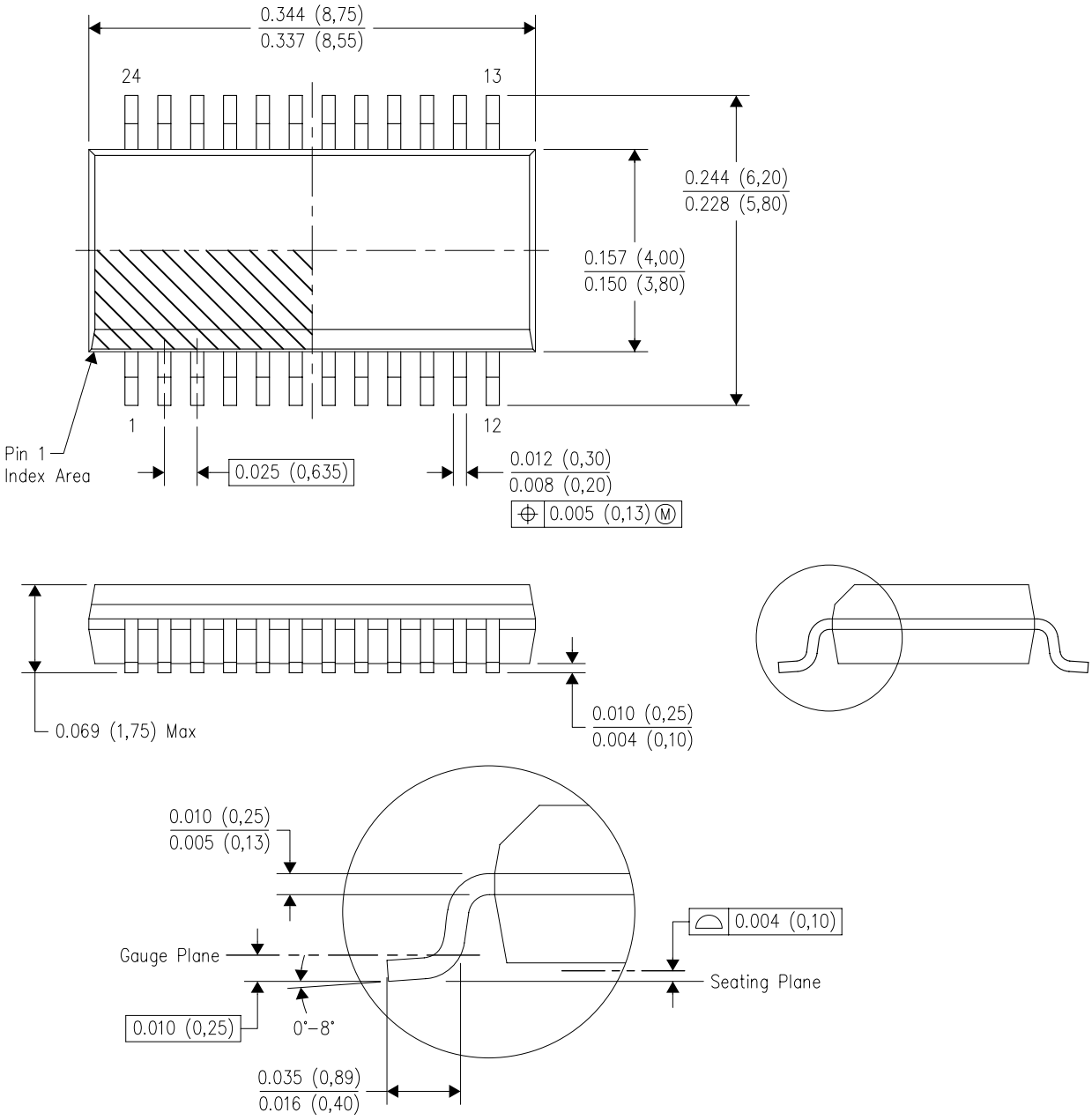
Bottom View

Exposed Thermal Pad Dimensions

4206344–7/AK 08/15

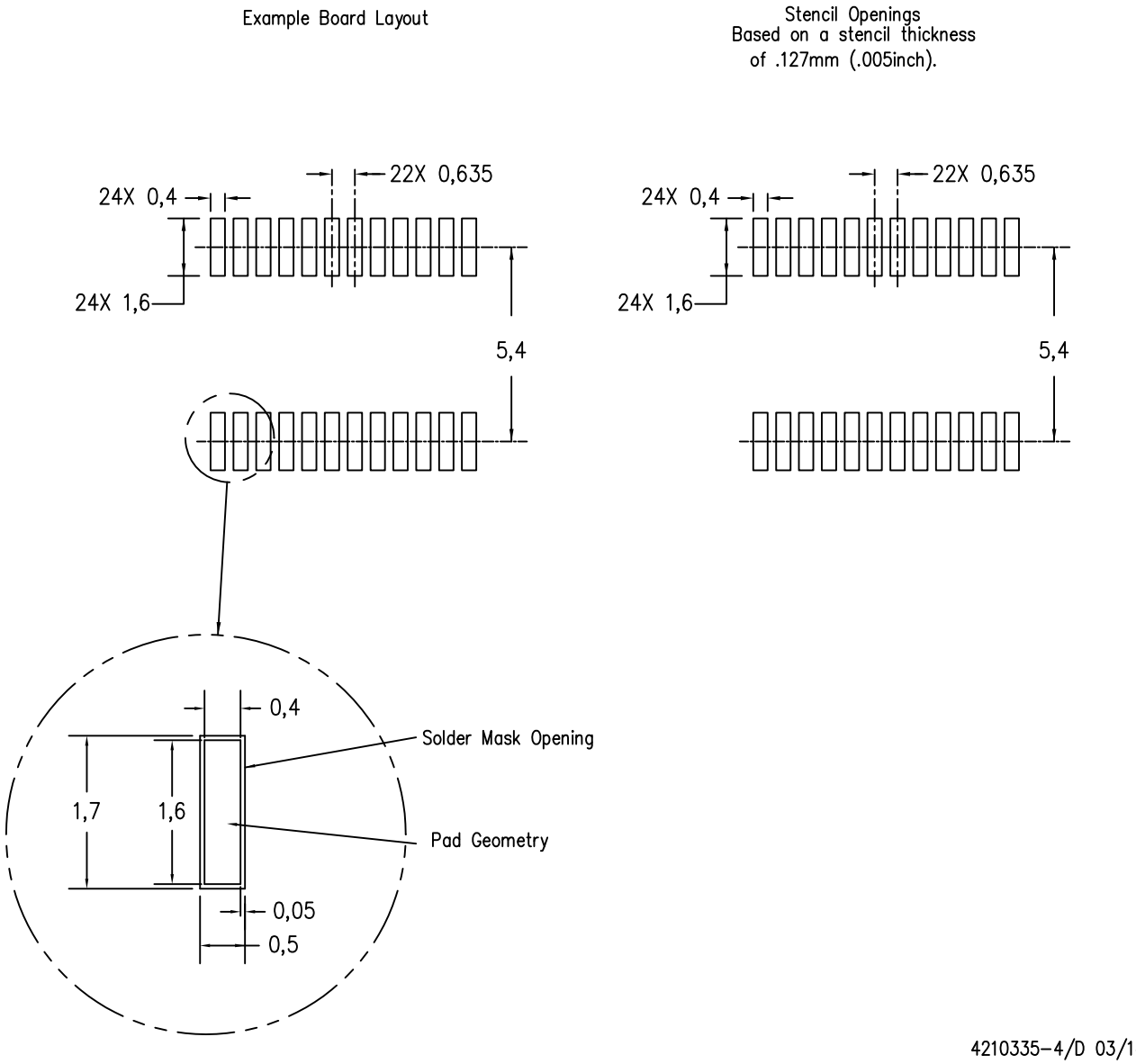
NOTES: A. All linear dimensions are in millimeters

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

DBQ (R–PDSO–G24) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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