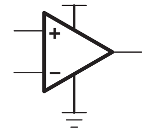
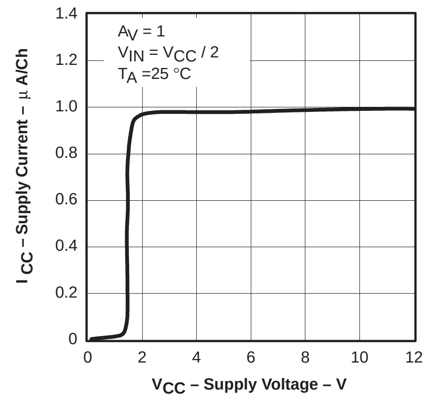
- **Micropower Operation . . . 1 μA/Channel**
- **Rail-to-Rail Input/Output**
- **Gain Bandwidth Product . . . 5.5 kHz**
- **Supply Voltage Range . . . 2.5 V to 12 V**
- **Specified Temperature Range**
  - **T_A = 0°C to 70°C . . . Commercial Grade**
  - **T_A = –40°C to 125°C . . . Industrial Grade**
- **Ultrasmall Packaging**
  - **5-Pin SOT-23 (TLV2241)**
  - **8-Pin MSOP (TLV2242)**
- **Universal OpAmp EVM**

Operational Amplifier



SUPPLY CURRENT vs SUPPLY VOLTAGE



description

The TLV224x family of single-supply operational amplifiers offers very low supply current of only 1 μA per channel.

The low supply current is coupled with extremely low input bias currents enabling them to be used with mega-Ω resistors making them ideal for portable, long active life, applications. DC accuracy is ensured with a low typical offset voltage as low as 600 μV, CMRR of 100 dB, and minimum open loop gain of 100 V/mV at 2.7 V.

The maximum recommended supply voltage is as high as 12 V and ensured operation down to 2.5 V, with electrical characteristics specified at 2.7 V, 5 V and 12 V. The 2.5-V operation makes it compatible with Li-Ion battery-powered systems and many micropower microcontrollers available today including TI's MSP430.

FAMILY PACKAGE TABLE

DEVICE	NO. OF Ch	PACKAGE TYPES					UNIVERSAL EVM
		PDIP	SOIC	SOT-23	TSSOP	MSOP	
TLV2241	1	8	8	5	—	—	Refer to the EVM Selection Guide (Lit# SLOU060)
TLV2242	2	8	8	—	—	8	
TLV2244	4	14	14	—	14	—	

SELECTION OF SINGLE SUPPLY OPERATIONAL AMPLIFIER PRODUCTS†

DEVICE	V_{DD} (V)	V_{IO} (mV)	BW (MHz)	SLEW RATE (V/μs)	I_{DD} (PER CHANNEL) (μA)	RAIL-TO-RAIL
TLV240x‡	2.5–16	0.390	0.005	0.002	0.880	I/O
TLV224x	2.5–12	0.600	0.005	0.002	1	I/O
TLV2211	2.7–10	0.450	0.065	0.025	13	O
TLV245x	2.7–6	0.020	0.22	0.110	23	I/O
TLV225x	2.7–8	0.200	0.2	0.12	35	O

† All specifications are typical values measured at 5 V.
‡ This device also offers 18-V reverse battery protection and 5-V over-the-rail operation on the inputs.

TLV2241 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE† (D)	SOT-23‡ (DBV)	SYMBOLS	PLASTIC DIP (P)
0°C to 70°C	3000 μV	TLV2241CD	—	—	—
–40°C to 125°C		TLV2241ID	TLV2241IDBV	VBEI	TLV2241IP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2241CDR).

‡ This package is available in a 250 piece mini-reel. To order this package, add a T suffix to the part number (e.g., TLV2241DBVT). This package is also available in a 3000 piece reel, add a R suffix to the part number (e.g., TLV2241DBVR).

TLV2242 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE† (D)	MSOP† (DGK)	SYMBOLS	PLASTIC DIP (P)
0°C to 70°C	3000 μV	TLV2242CD	—	—	—
–40°C to 125°C		TLV2242ID	TLV2242IDGK	xxTIALE	TLV2242IP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2242CDR).

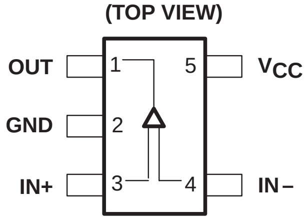
TLV2244 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE† (D)	PLASTIC DIP (N)	TSSOP (PW)
0°C to 70°C	3000 μV	TLV2244CD	—	—
–40°C to 125°C		TLV2244ID	TLV2244IN	TLV2244IPW

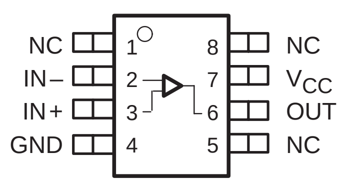
† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2244CDR).

TLV224x PACKAGE PINOUTS

TLV2241
DBV PACKAGE
(TOP VIEW)

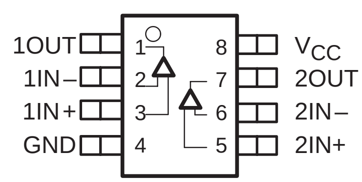


TLV2241
D OR P PACKAGE
(TOP VIEW)

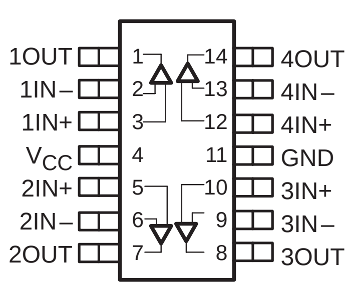


NC – No internal connection

TLV2242
D, DGK, OR P PACKAGE
(TOP VIEW)



TLV2244
D, N, OR PW PACKAGE
(TOP VIEW)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . 16.5 V
Differential input voltage, V_{ID} . . . . ± V_{CC}
Input current, I_I (any input) . . . . ±10 mA
Output current, I_O . . . . ±10 mA
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . 0°C to 70°C
I suffix . . . . –40°C to 125°C
Maximum junction temperature, T_J . . . . 150°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND

DISSIPATION RATING TABLE

PACKAGE	Θ_{JC} (°C/W)	Θ_{JA} (°C/W)	$T_A \leq 25°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8)	38.3	176	710 mW	142 mW
D (14)	26.9	122.6	1022 mW	204.4 mW
DBV (5)	55	324.1	385 mW	77.1 mW
DGK (8)	54.2	259.9	481 mW	96.2 mW
N (14)	32	78	1600 mW	320.5 mW
P (8)	41	104	1200 mW	240.4 mW
PW (14)	29.3	173.6	720 mW	144 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}	Single supply	2.5	12	V
	Split supply	±1.25	±6	
Common-mode input voltage range, V_{ICR}		0	V_{CC}	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	–40	125	

electrical characteristics at recommended operating conditions, V_{CC} = 2.7, 5 V, and 12 V (unless otherwise noted)‡

dc performance

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = V_{CC}/2$ V, $V_{IC} = V_{CC}/2$ V, R_S = 50 Ω		25°C		600	3000	μV
				Full range			4500	
α_{VIO}	Offset voltage drift			25°C		3		μV/°C
CMRR	Common-mode rejection ratio	V_{IC} = 0 to V_{CC}, R_S = 50 Ω	V_{CC} = 2.7 V	25°C	55	100		dB
				Full range	50			
			V_{CC} = 5 V	25°C	60	100		
				Full range	53			
			V_{CC} = 12 V	25°C	60	100		
				Full range	55			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 2.7 V, $V_{O(pp)}$ = 1 V, R_L = 500 kΩ		25°C	100	400		V/mV
				Full range	30			
		V_{CC} = 5 V, $V_{O(pp)}$ = 3 V, R_L = 500 kΩ		25°C	250	1000		
				Full range	100			
		V_{CC} = 12 V, $V_{O(pp)}$ = 6 V, R_L = 500 kΩ		25°C	700	1500		
				Full range	120			

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

input characteristics

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
I_{IO}	Input offset current	$V_O = V_{CC}/2$ V, $V_{IC} = V_{CC}/2$ V, R_S = 50 Ω		25°C		25	250	pA
			TLV224xC	Full range			300	
			TLV224xI				400	
I_{IB}	Input bias current			25°C		100	500	pA
			TLV224xC	Full range			550	
			TLV224xI				1000	
$r_{i(d)}$	Differential input resistance			25°C		300		MΩ
$C_{i(c)}$	Common-mode input capacitance	f = 100 kHz		25°C		3		pF

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.
‡ Specifications at 5 V are ensured by design and device testing at 2.7 V and 12 V.

electrical characteristics at recommended operating conditions, V_{CC} = 2.7, 5 V, and 12 V (unless otherwise noted)‡ (continued)

output characteristics

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$V_{IC} = V_{CC}/2$, I_{OH} = –2 μA	V_{CC} = 2.7 V	25°C	2.65	2.68		V
				Full range	2.63			
			V_{CC} = 5 V	25°C	4.95	4.98		
				Full range	4.93			
			V_{CC} = 12 V	25°C	11.95	11.98		
				Full range	11.93			
		$V_{IC} = V_{CC}/2$, I_{OH} = –50 μA	V_{CC} = 2.7 V	25°C	2.62	2.65		
				Full range	2.6			
			V_{CC} = 5 V	25°C	4.92	4.95		
				Full range	4.9			
			V_{CC} = 12 V	25°C	11.92	11.95		
				Full range	11.9			
V_{OL}	Low-level output voltage	$V_{IC} = V_{CC}/2$, I_{OL} = 2 μA		25°C		90	150	mV
				Full range			180	
		$V_{IC} = V_{CC}/2$, I_{OL} = 50 μA		25°C		180	230	
				Full range			260	
I_O	Output current	V_O = 0.5 V from rail		25°C		±200		μA

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

power supply

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
I_{CC}	Supply current (per channel)	$V_O = V_{CC}/2$	V_{CC} = 2.7 V or 5 V	25°C		980	1200	nA
				Full range			1500	
			V_{CC} = 12 V	25°C		1000	1250	
				Full range			1550	
PSRR	Power supply rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC} = 2.7 to 5 V, $V_{IC} = V_{CC}/2$ V, No load,		25°C	70	100		dB
			TLV224xC	Full range	65			
			TLV224xI		60			dB
		V_{CC} = 5 to 12 V, $V_{IC} = V_{CC}/2$ V, No load		25°C	70	100		dB
				Full range	70			

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.
‡ Specifications at 5 V are ensured by design and device testing at 2.7 V and 12 V.

electrical characteristics at recommended operating conditions, V_{CC} = 2.7, 5 V, and 12 V (unless otherwise noted)‡ (continued)

dynamic performance

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
UGBW	Unity gain bandwidth	R_L = 500 kΩ, C_L = 100 pF		25°C		5.5		kHz
SR	Slew rate at unity gain	$V_{O(pp)}$ = 0.8 V, R_L = 500 kΩ, C_L = 100 pF		25°C		2		V/ms
φM	Phase margin	R_L = 500 kΩ, C_L = 100 pF		25°C		60		
	Gain margin					15		dB
t_s	Settling time	V_{CC} = 2.7 or 5 V, $V_{(STEP)PP}$ = 1 V, C_L = 100 pF, A_V = –1, R_L = 100 kΩ	0.1%	25°C		1.84		ms
		V_{CC} = 12 V, $V_{(STEP)PP}$ = 1 V, C_L = 100 pF, A_V = –1, R_L = 100 kΩ	0.1%			6.1		
			0.01%			32		

noise/distortion performance

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		800		nV/√Hz
		f = 100 Hz			500		
I_n	Equivalent input noise current	f = 100 Hz			8		fA/√Hz

‡ Specifications at 5 V are ensured by design and device testing at 2.7 V and 12 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2, 3
I_{IB}	Input bias current	vs Free-air temperature	4, 6, 8
		vs Common-mode input voltage	5, 7, 9
I_{IO}	Input offset current	vs Free-air temperature	4, 6, 8
		vs Common-mode input voltage	5, 7, 9
CMRR	Common-mode rejection ratio	vs Frequency	10
V_{OH}	High-level output voltage	vs High-level output current	11, 13, 15
V_{OL}	Low-level output voltage	vs Low-level output current	12, 14, 16
$V_{O(PP)}$	Output voltage peak-to-peak	vs Frequency	17
z_o	Output impedance	vs Frequency	18
I_{CC}	Supply current	vs Supply voltage	19
PSRR	Power supply rejection ratio	vs Frequency	20
A_{VD}	Differential voltage gain	vs Frequency	21
	Phase	vs Frequency	21
	Gain-bandwidth product	vs Supply voltage	22
SR	Slew rate	vs Free-air temperature	23
ϕ_m	Phase margin	vs Capacitive load	24
	Gain margin	vs Capacitive load	25
	Voltage noise over a 10 Second Period		26
	Large-signal voltage follower		27, 28, 29
	Small-signal voltage follower		30
	Large-signal inverting pulse response		31, 32, 33
	Small-signal inverting pulse response		34
	Crosstalk	vs Frequency	35

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

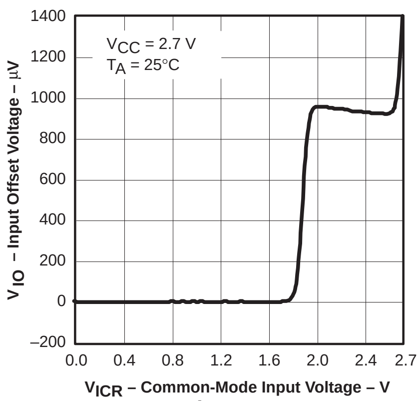


Figure 1

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

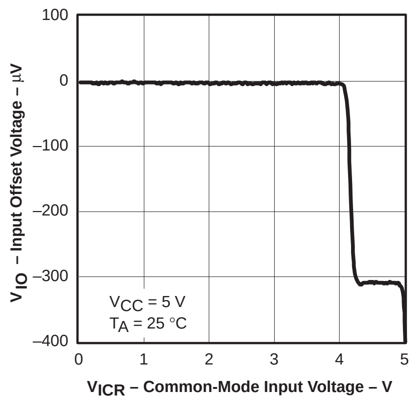


Figure 2

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

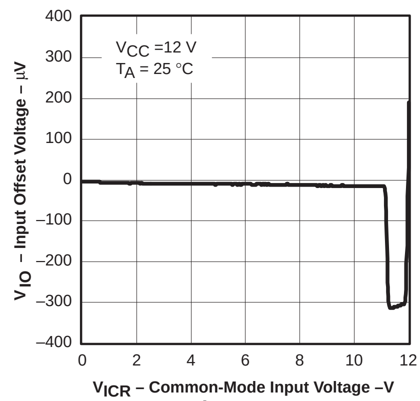


Figure 3

INPUT BIAS / OFFSET CURRENT vs FREE-AIR TEMPERATURE

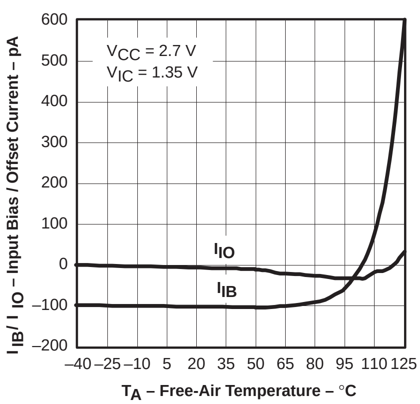


Figure 4

INPUT BIAS / OFFSET CURRENT vs COMMON MODE INPUT VOLTAGE

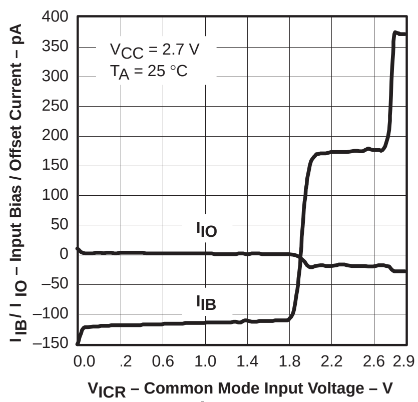


Figure 5

INPUT BIAS / OFFSET CURRENT vs FREE-AIR TEMPERATURE

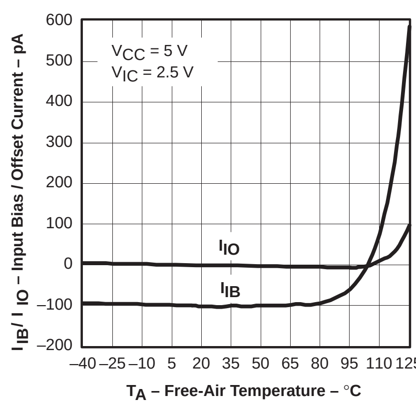


Figure 6

INPUT BIAS / OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

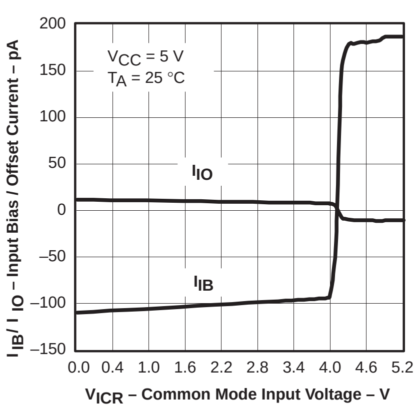


Figure 7

INPUT BIAS / OFFSET CURRENT vs FREE-AIR TEMPERATURE

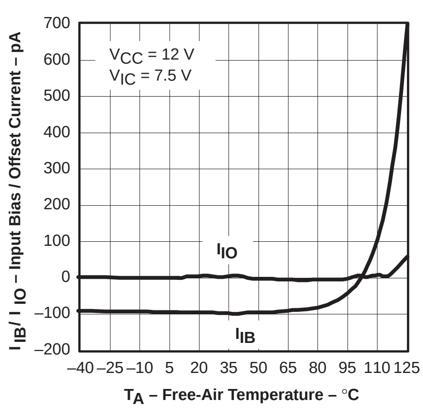


Figure 8

INPUT BIAS / OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

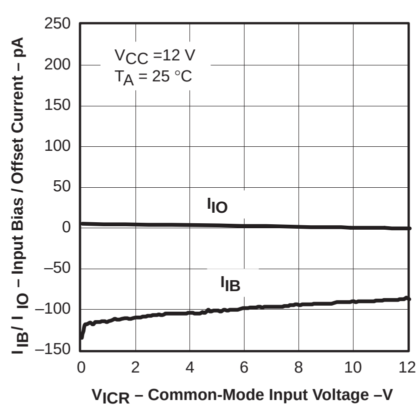


Figure 9

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREQUENCY

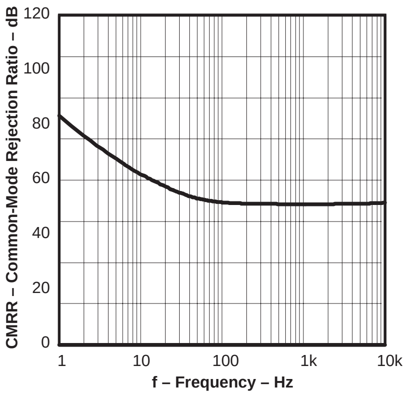


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

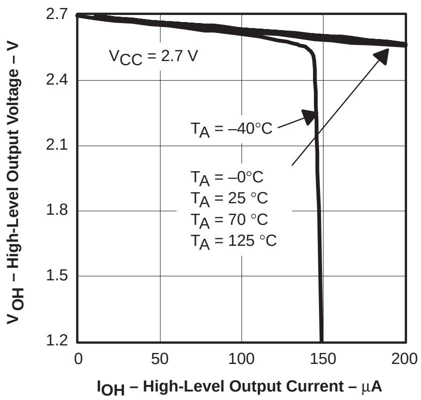


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

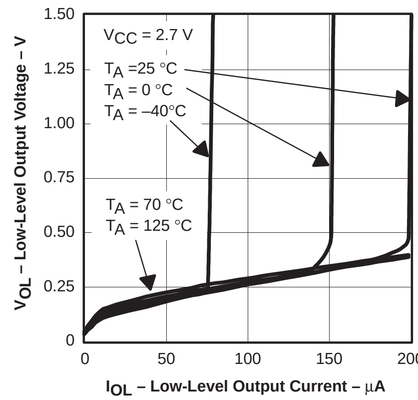


Figure 12

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

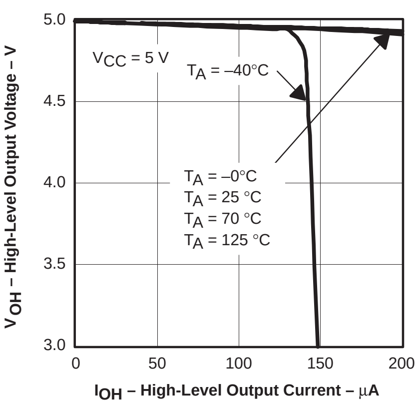


Figure 13

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

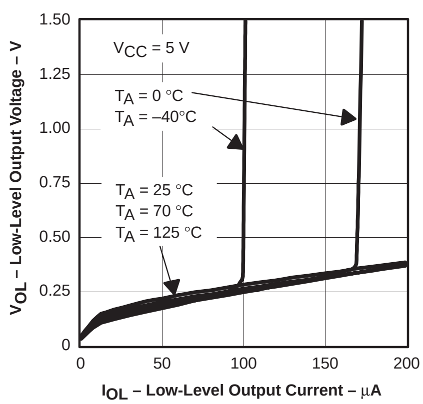


Figure 14

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

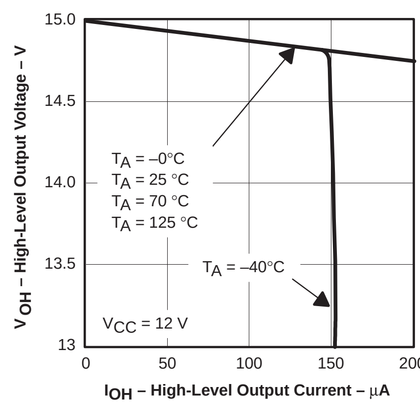


Figure 15

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

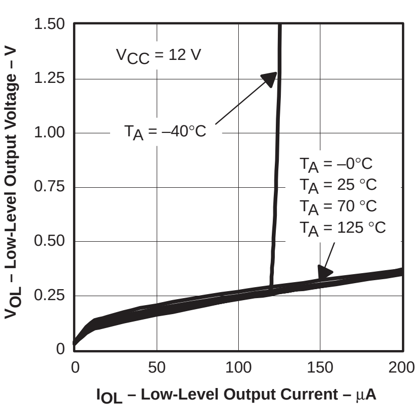


Figure 16

OUTPUT VOLTAGE PEAK-TO-PEAK vs FREQUENCY

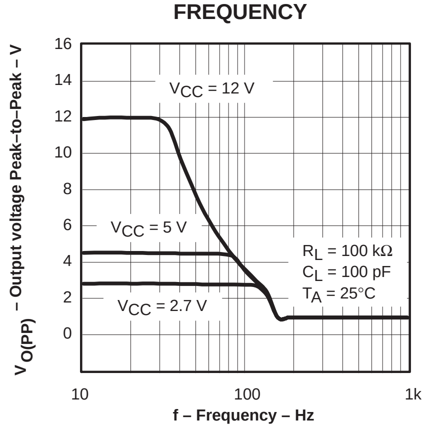


Figure 17

OUTPUT IMPEDANCE vs FREQUENCY

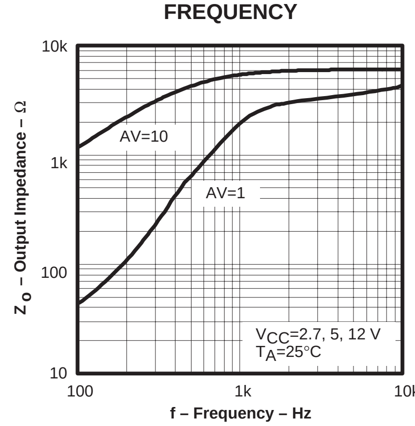


Figure 18

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

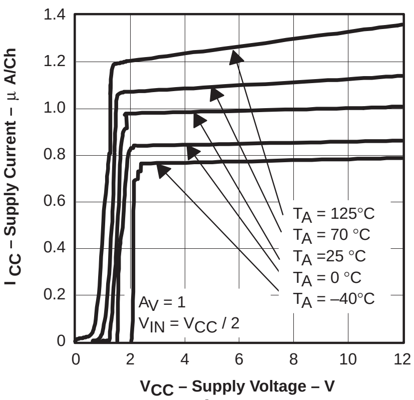


Figure 19

POWER SUPPLY REJECTION RATIO vs FREQUENCY

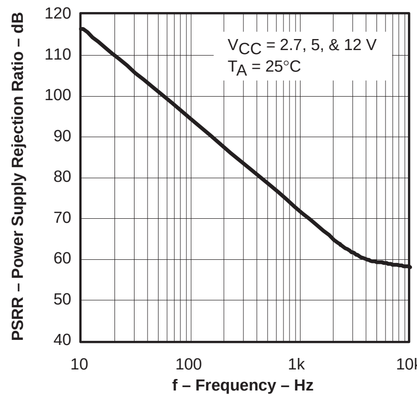


Figure 20

DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY

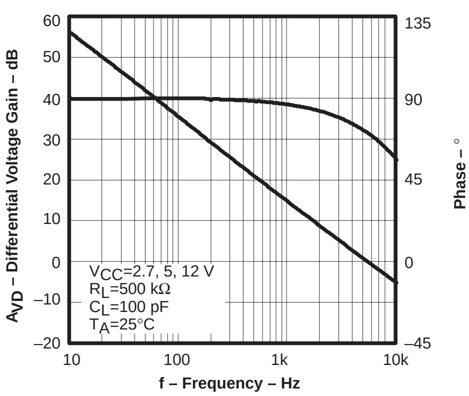


Figure 21

GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

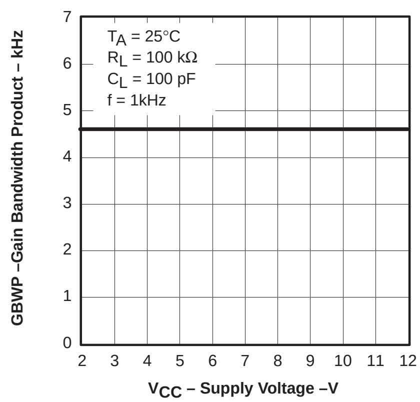


Figure 22

SLEW RATE vs FREE-AIR TEMPERATURE

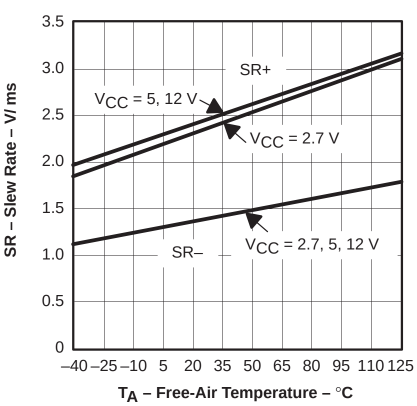


Figure 23

PHASE MARGIN vs CAPACITIVE LOAD

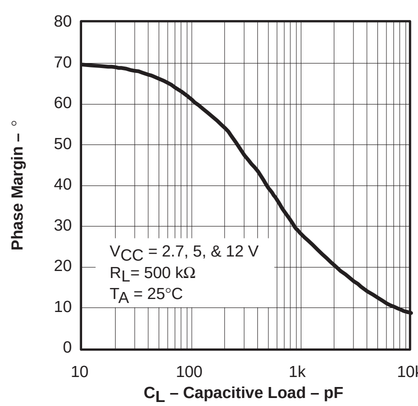


Figure 24

TYPICAL CHARACTERISTICS

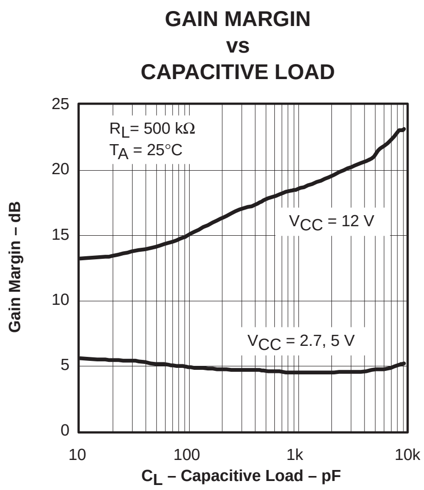


Figure 25

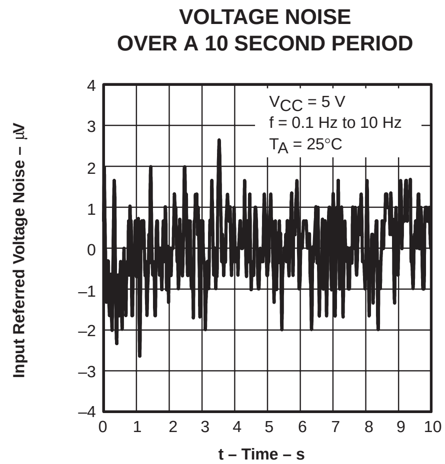


Figure 26

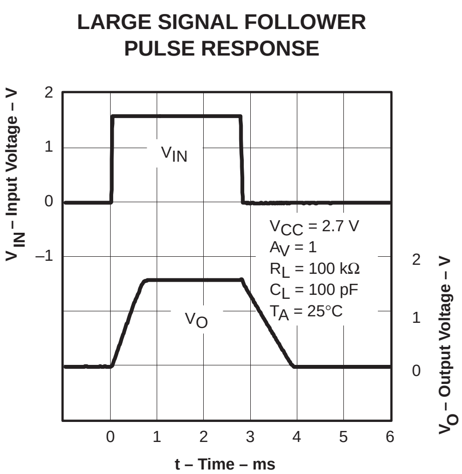


Figure 27

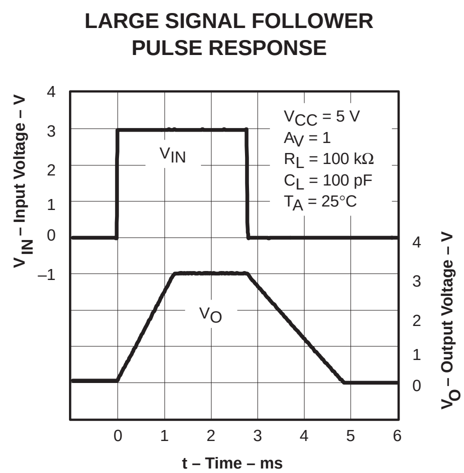


Figure 28

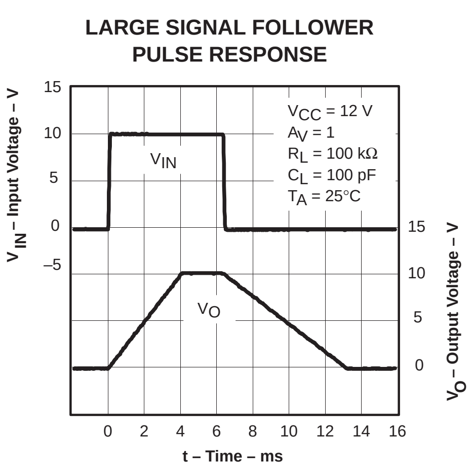


Figure 29

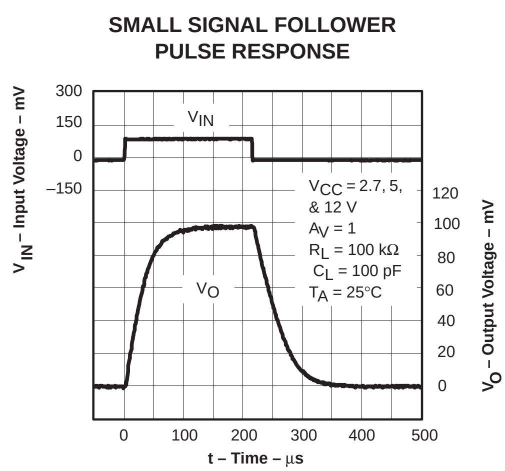


Figure 30

TYPICAL CHARACTERISTICS

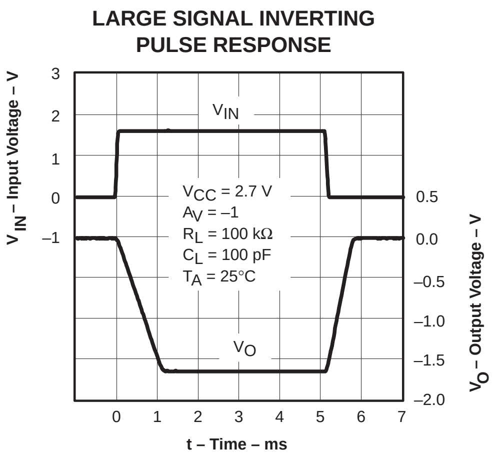


Figure 31

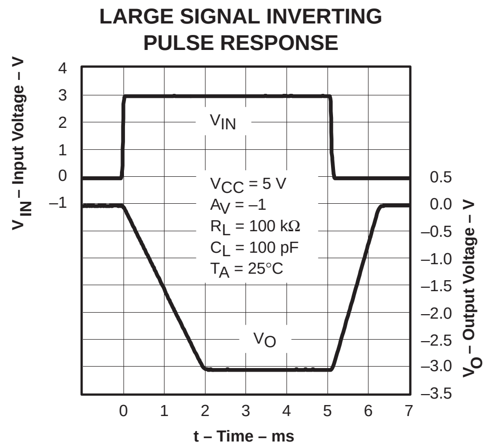


Figure 32

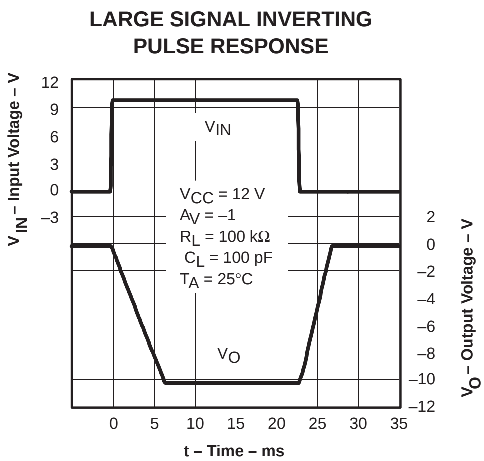


Figure 33

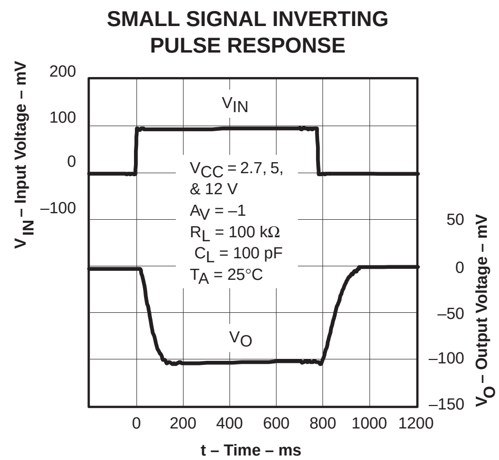


Figure 34

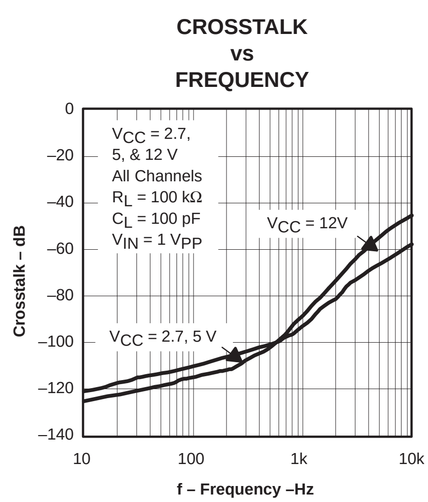
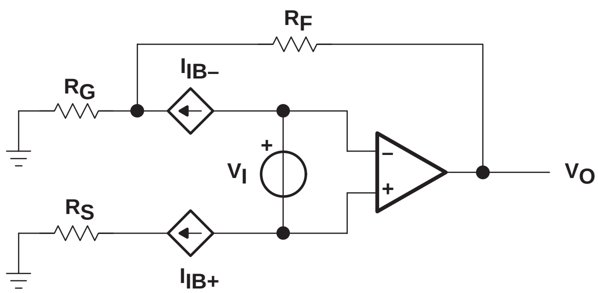


Figure 35

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

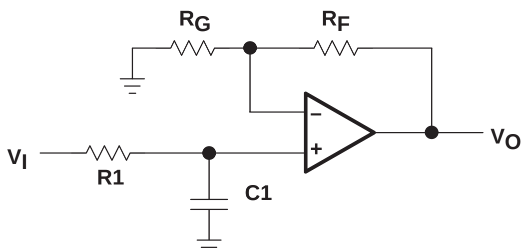


$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 36. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 37).

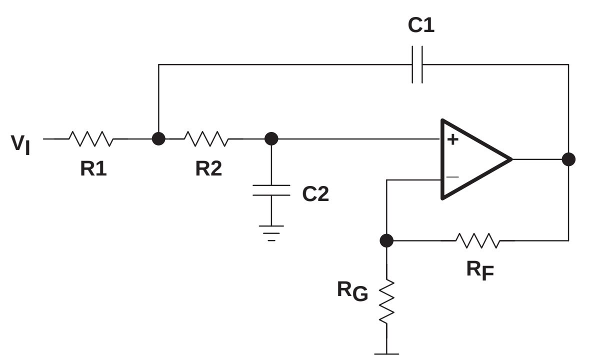


$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 37. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 38. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV224x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

general power dissipation considerations

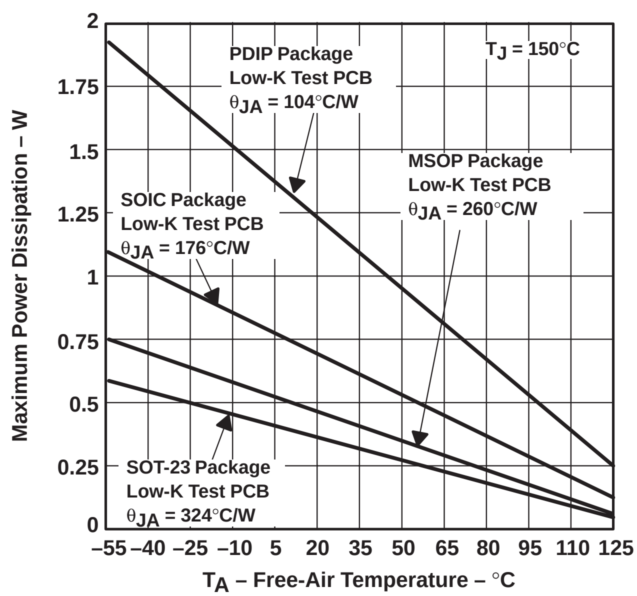
For a given θ_{JA}, the maximum power dissipation is shown in Figure 39 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of THS224x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

MAXIMUM POWER DISSIPATION
vs
FREE-AIR TEMPERATURE



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 39. Maximum Power Dissipation vs Free-Air Temperature

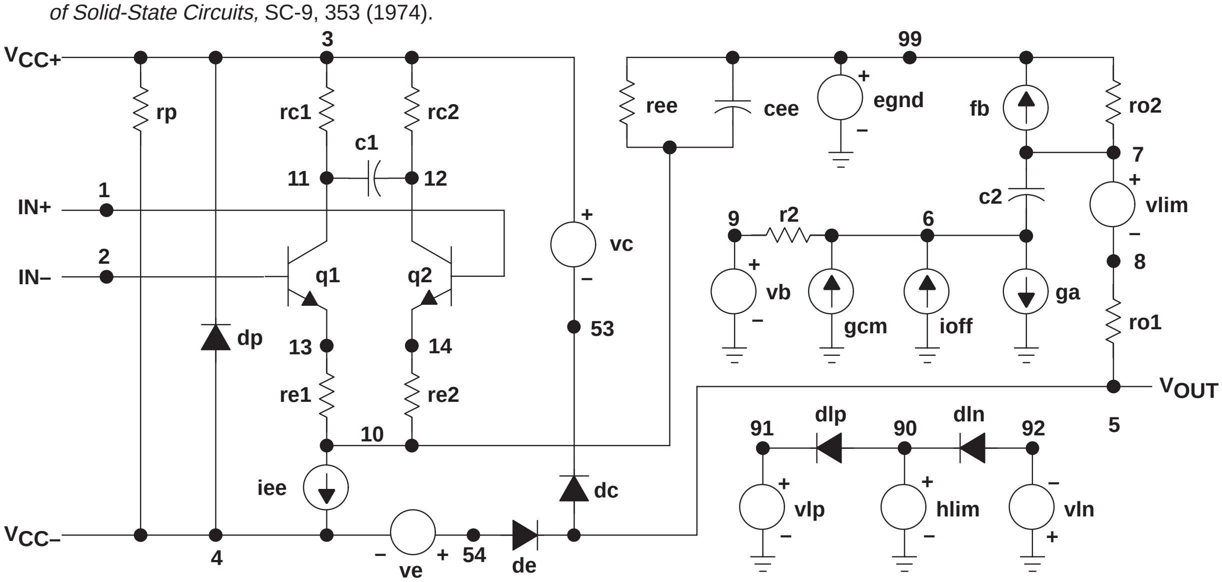
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 2) and subcircuit in Figure 40 are generated using the TLV224x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 2: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers”, *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.subckt 224X_5V–X  1 2 3 4 5
 *
 c1    11  12  9.8944E–12
 c2    6   7   30.000E–12
 cee   10  99  8.8738E–12
 dc    5   53  dy
 de    54  5   dy
 dlp   90  91  dx
 dln   92  90  dx
 dp    4   3   dx
 egnd  99  0   poly(2) (3,0) (4,0) 0 .5 .5
 fb    7   99  poly(5) vb vc ve vlp vln 0 61.404E6 –1E3 1E3 61E6 –61E6
 ga    6   0   11 12 1.0216E–6
 gcm   0   6   10 99 10.216E–12
 iee   10  4   dc 54.540E–9
 ioff  0   6   dc 5e–12
 hlim  90  0   vlim 1K
 q1    11  2   13 qx1
 q2    12  1   14 qx2
 r2    6   9   100.00E3
 rc1   3   11  978.81E3
 rc2   3   12  978.81E3
 re1   13  10  30.364E3
 re2   14  10  30.364E3
 ree   10  99  3.6670E9
 ro1   8   5   10
 ro2   7   99  10
 rp    3   4   1.4183E6
 vb    9   0   dc  0
 vc    3   53  dc  .88315
 ve    54  4   dc  .88315
 vlim  7   8   dc  0
 vlp   91  0   dc  540
 vln   0   92  dc  540
.model  dx   D(Is=800.00E–18)
.model  dy   D(Is=800.00E–18 Rs=1m Cjo=10p)
.model  qx1  NPN(Is=800.00E–18 Bf=27.270E21)
.model  qx2  NPN(Is=800.0000E–18 Bf=27.270E21)
.ends
```

Figure 40. Boyle Macromodels and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2241ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2241I	Samples
TLV2241IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBEI	Samples
TLV2241IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBEI	Samples
TLV2241IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBEI	Samples
TLV2241IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBEI	Samples
TLV2241IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2241I	Samples
TLV2241IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2241I	Samples
TLV2241IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2241I	Samples
TLV2242CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2242C	Samples
TLV2242CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2242C	Samples
TLV2242CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2242C	Samples
TLV2242ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2242I	Samples
TLV2242IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2242I	Samples
TLV2242IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ALE	Samples
TLV2242IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ALE	Samples
TLV2242IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ALE	Samples
TLV2242IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2242I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2242IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2242I	Samples
TLV2244CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2244C	Samples
TLV2244ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2244I	Samples
TLV2244IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2244I	Samples
TLV2244IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2244I	Samples
TLV2244IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2244I	Samples
TLV2244IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2244I	Samples
TLV2244IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2244I	Samples
TLV2244IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2244I	Samples
TLV2244IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2244I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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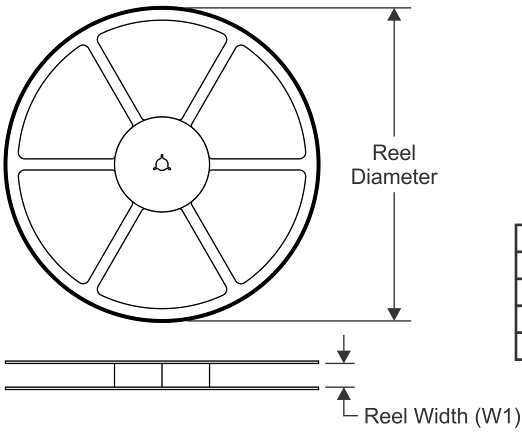
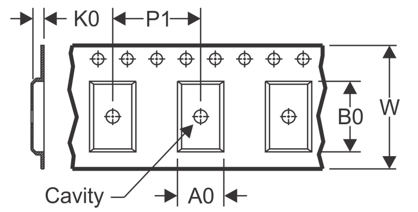
TAPE AND REEL INFORMATION

REEL DIMENSIONS

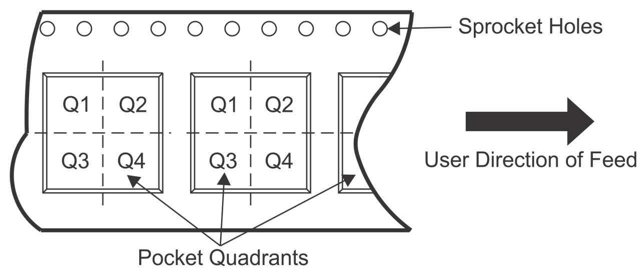


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

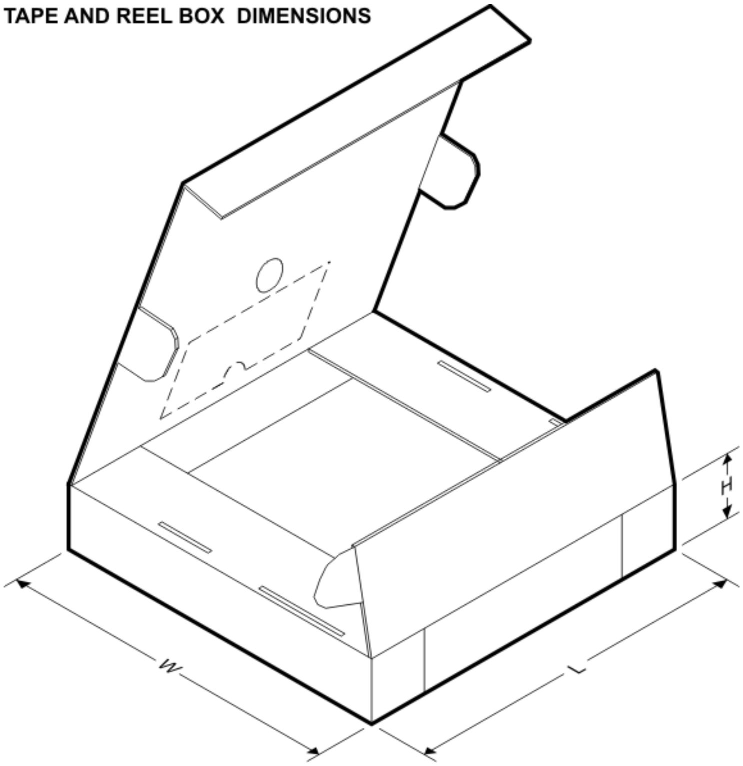
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

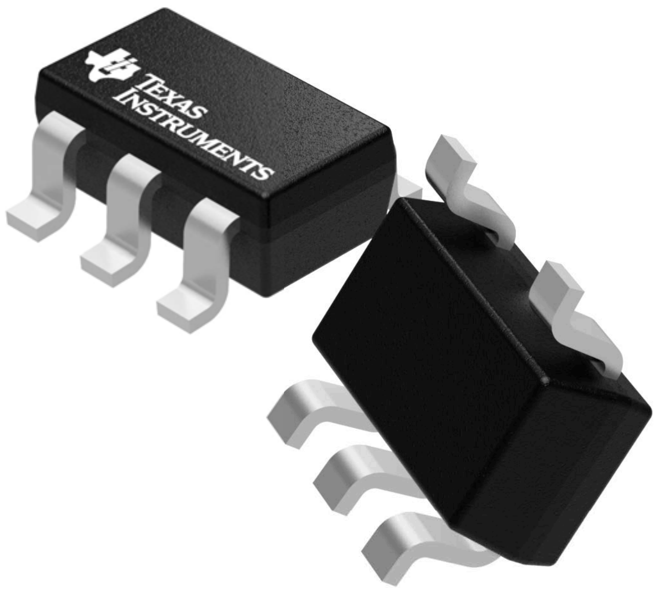
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2241IDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2241IDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2241IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2241IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2242CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2242IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2242IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2244IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2244IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2241IDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV2241IDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TLV2241IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2241IDR	SOIC	D	8	2500	367.0	367.0	38.0
TLV2242CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2242IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2242IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2244IDR	SOIC	D	14	2500	367.0	367.0	38.0
TLV2244IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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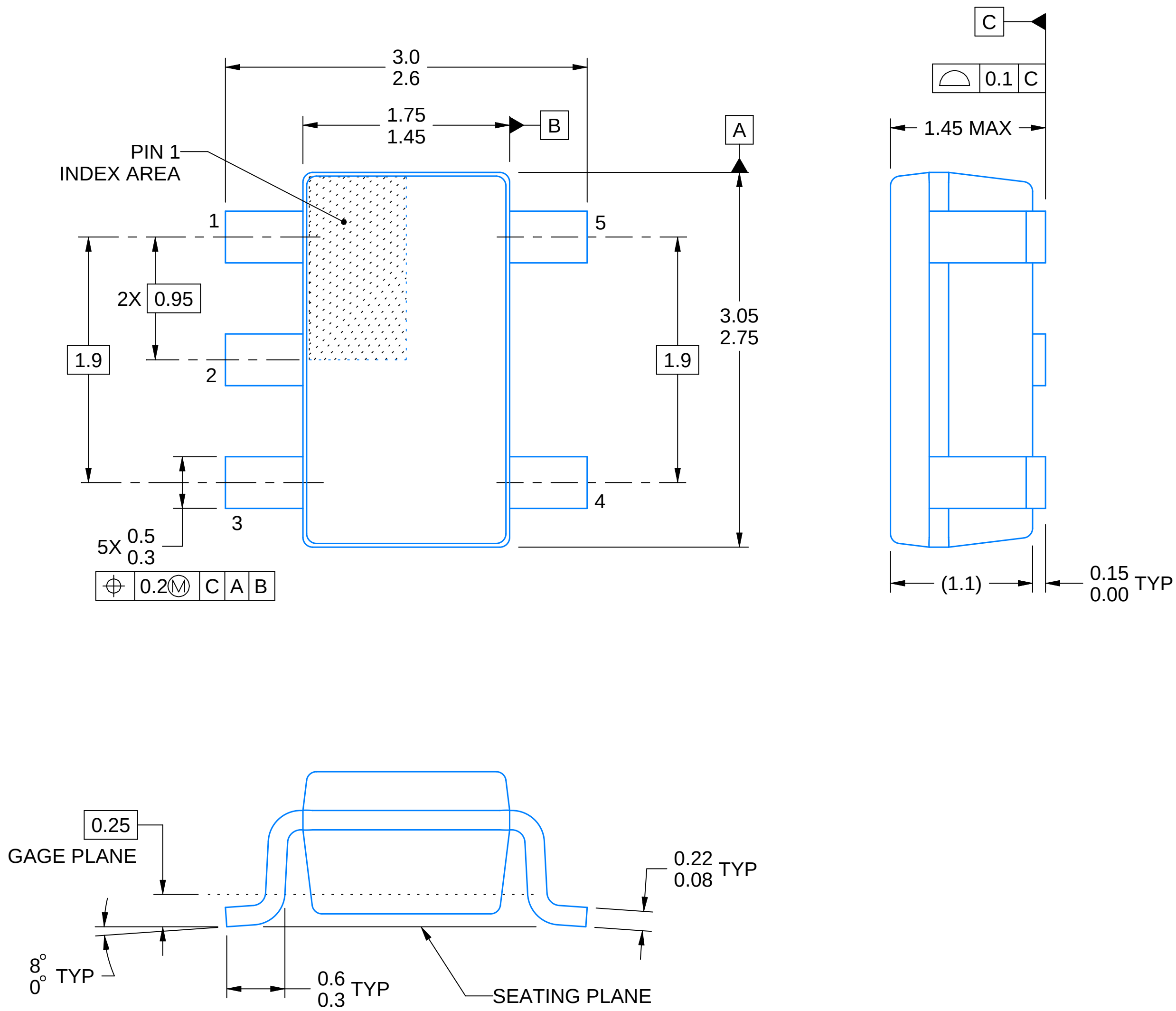
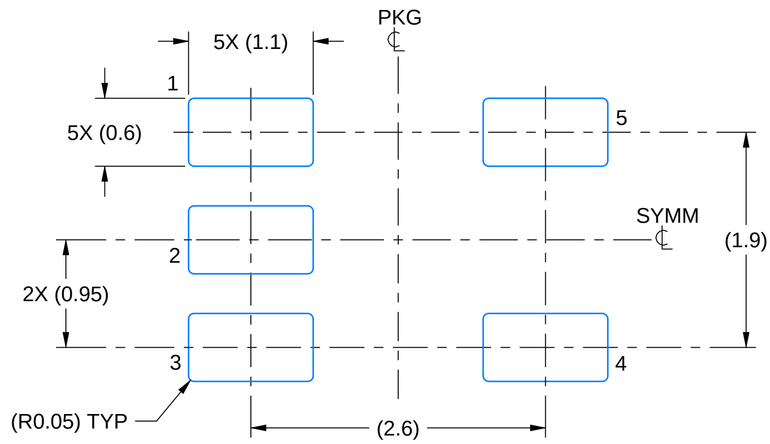


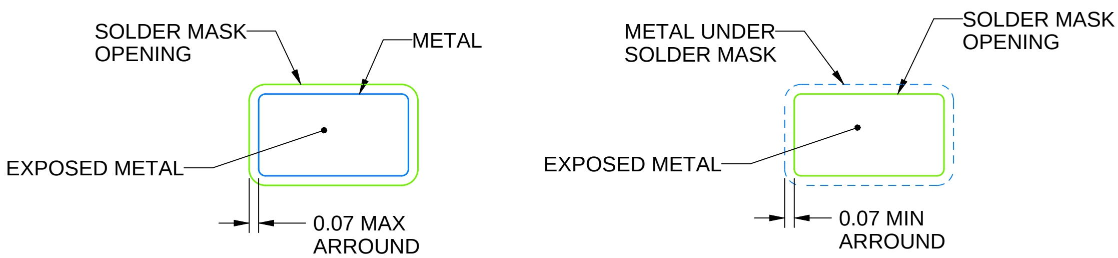
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

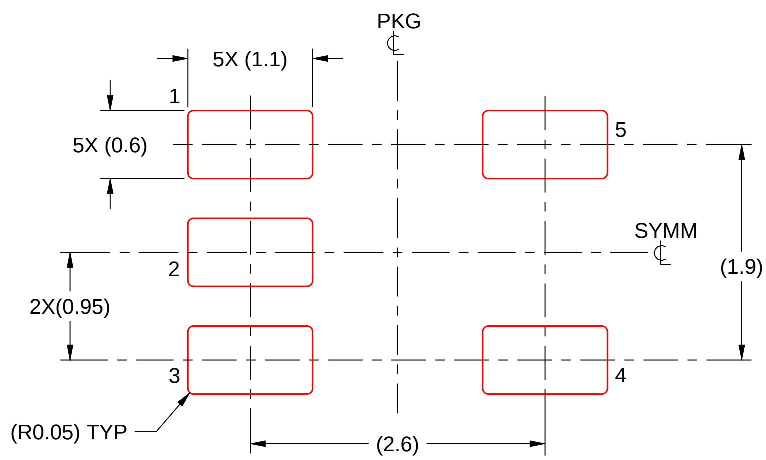
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



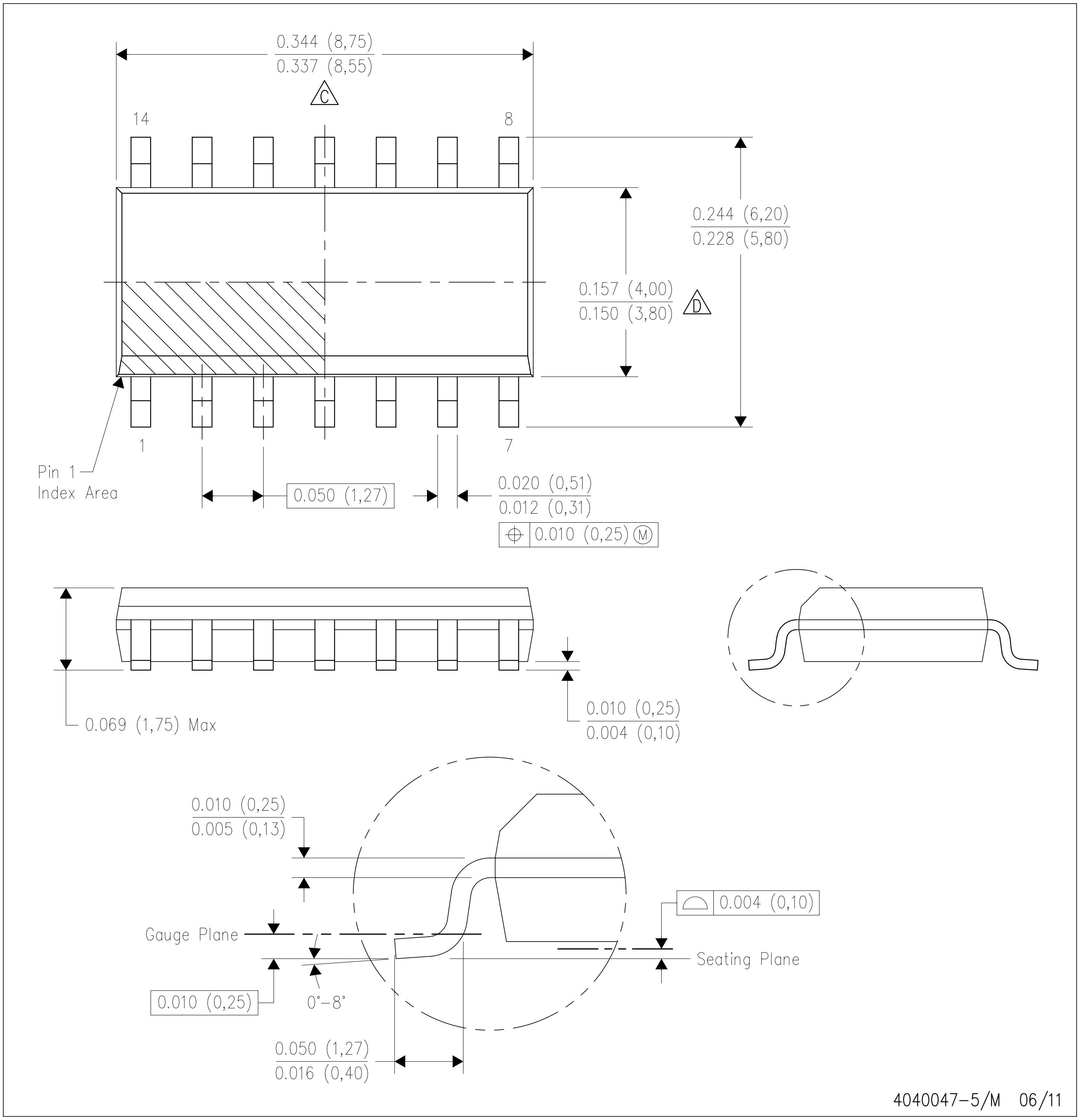
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

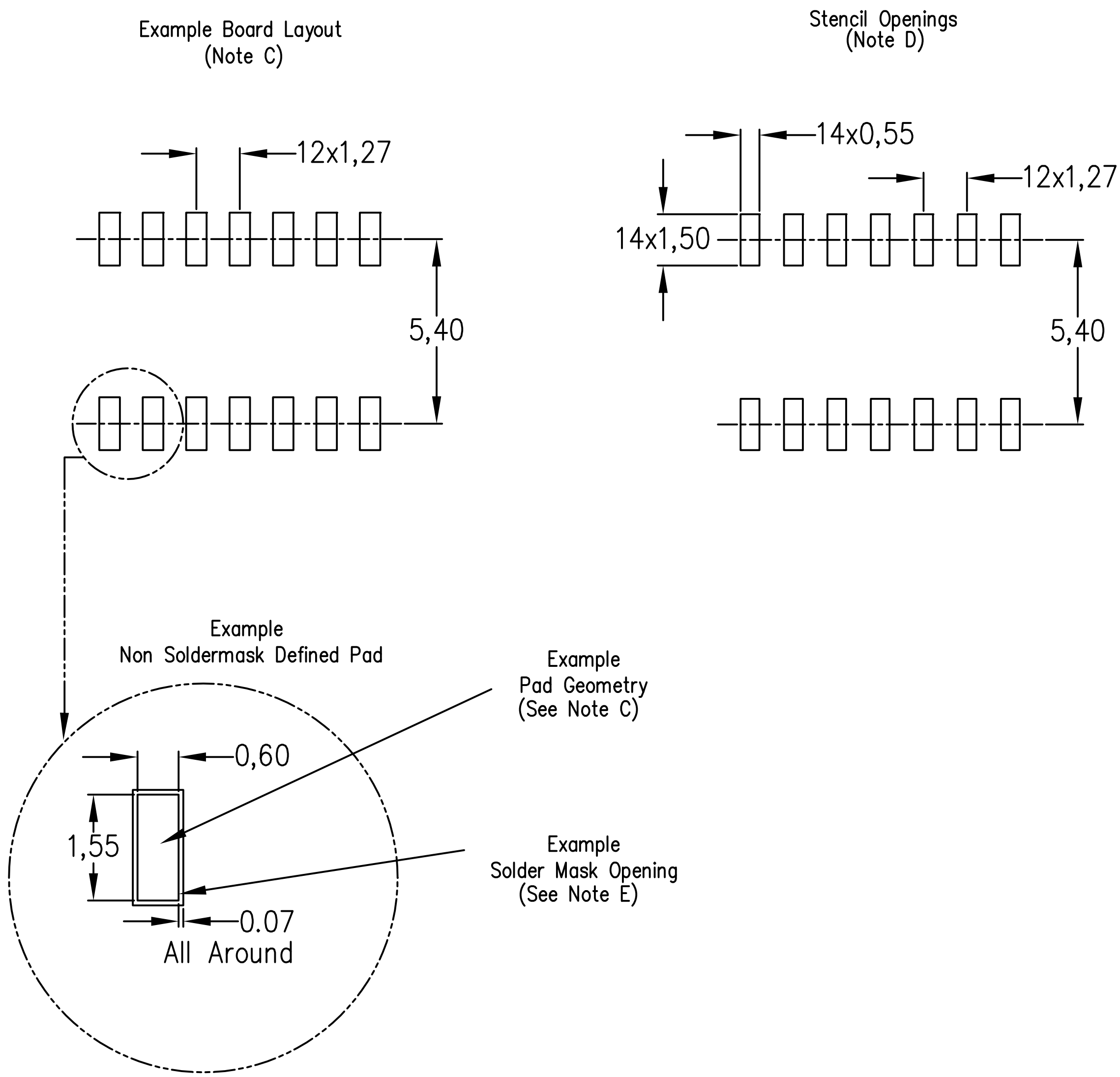
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

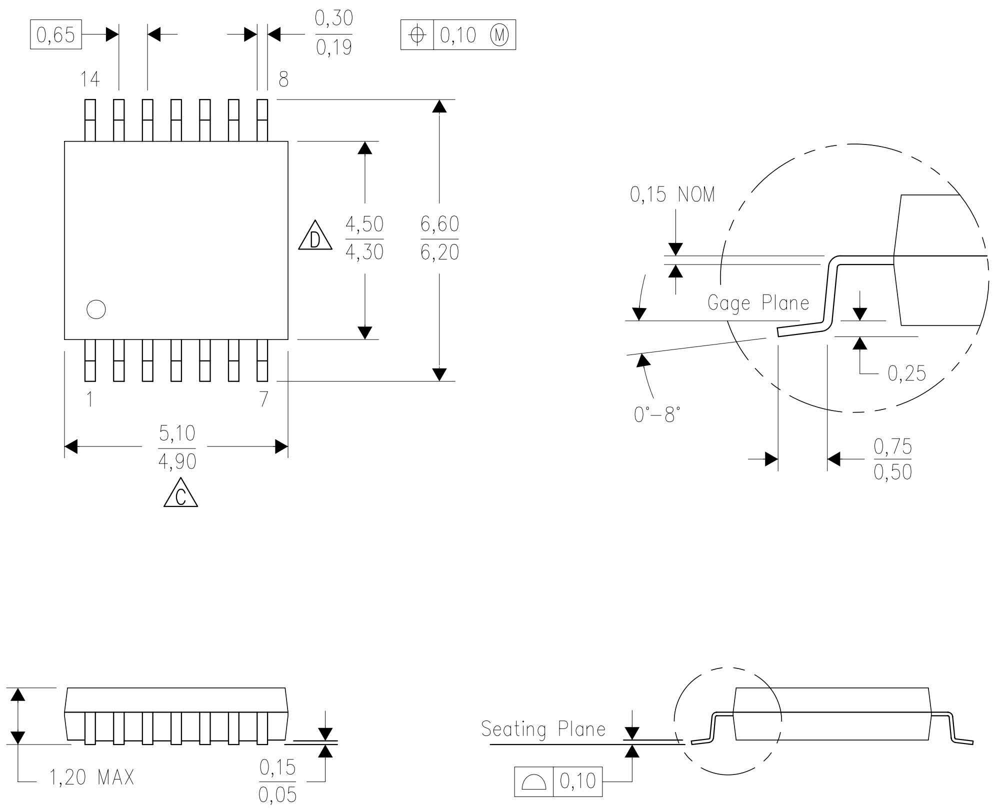
D (R-PDSO-G14) PLASTIC SMALL OUTLINE



4211283-3/E 08/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

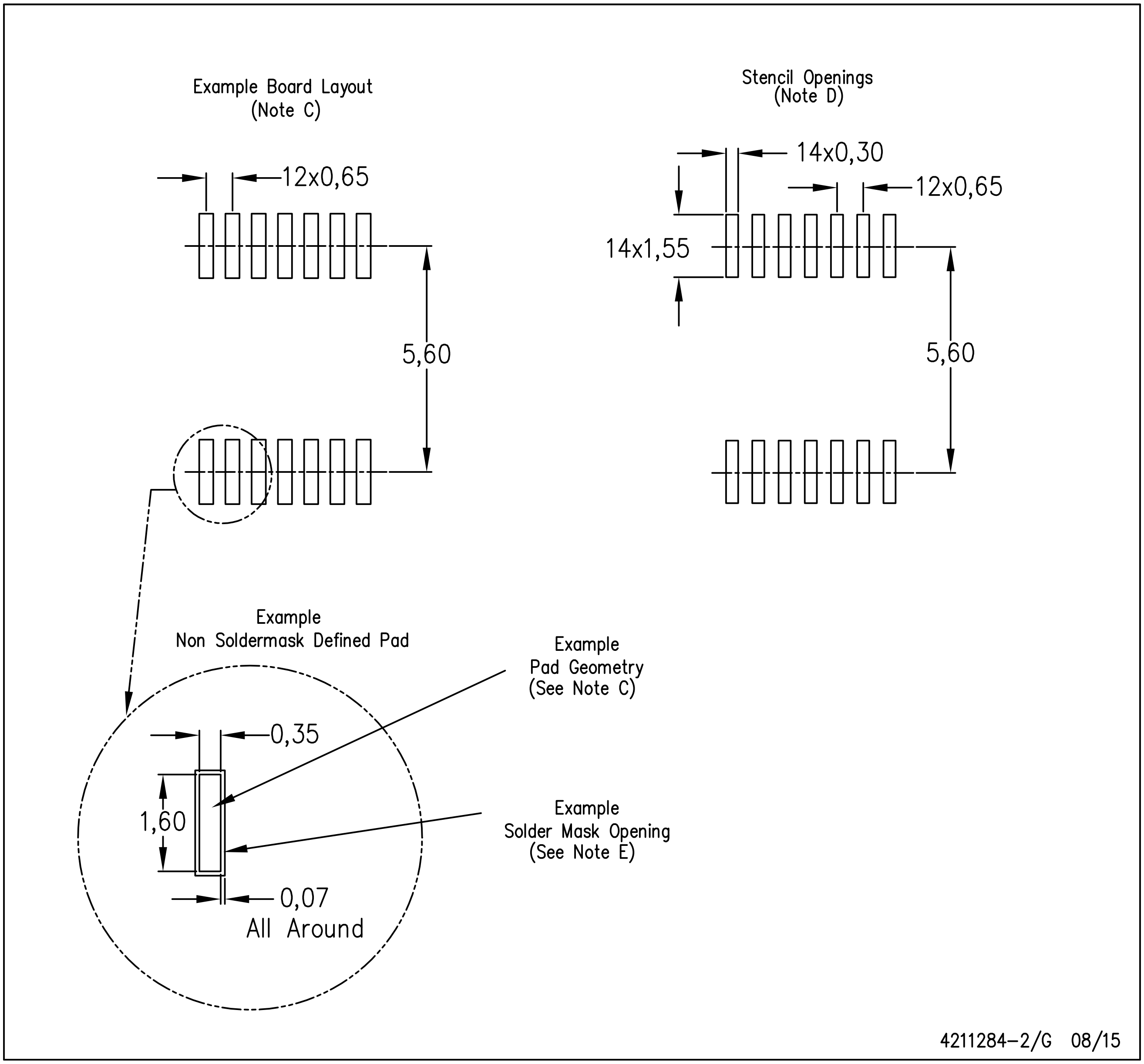
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

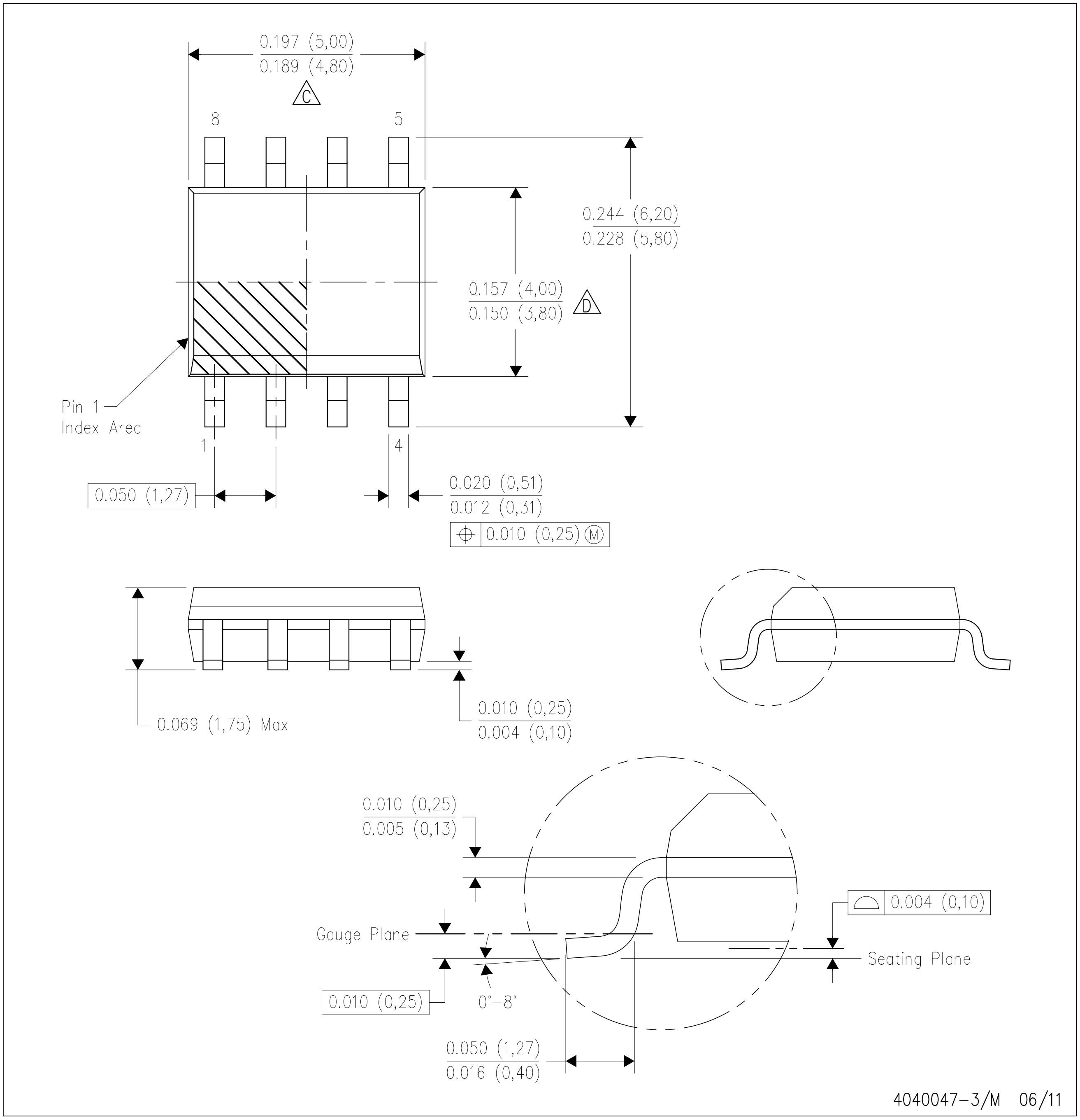
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



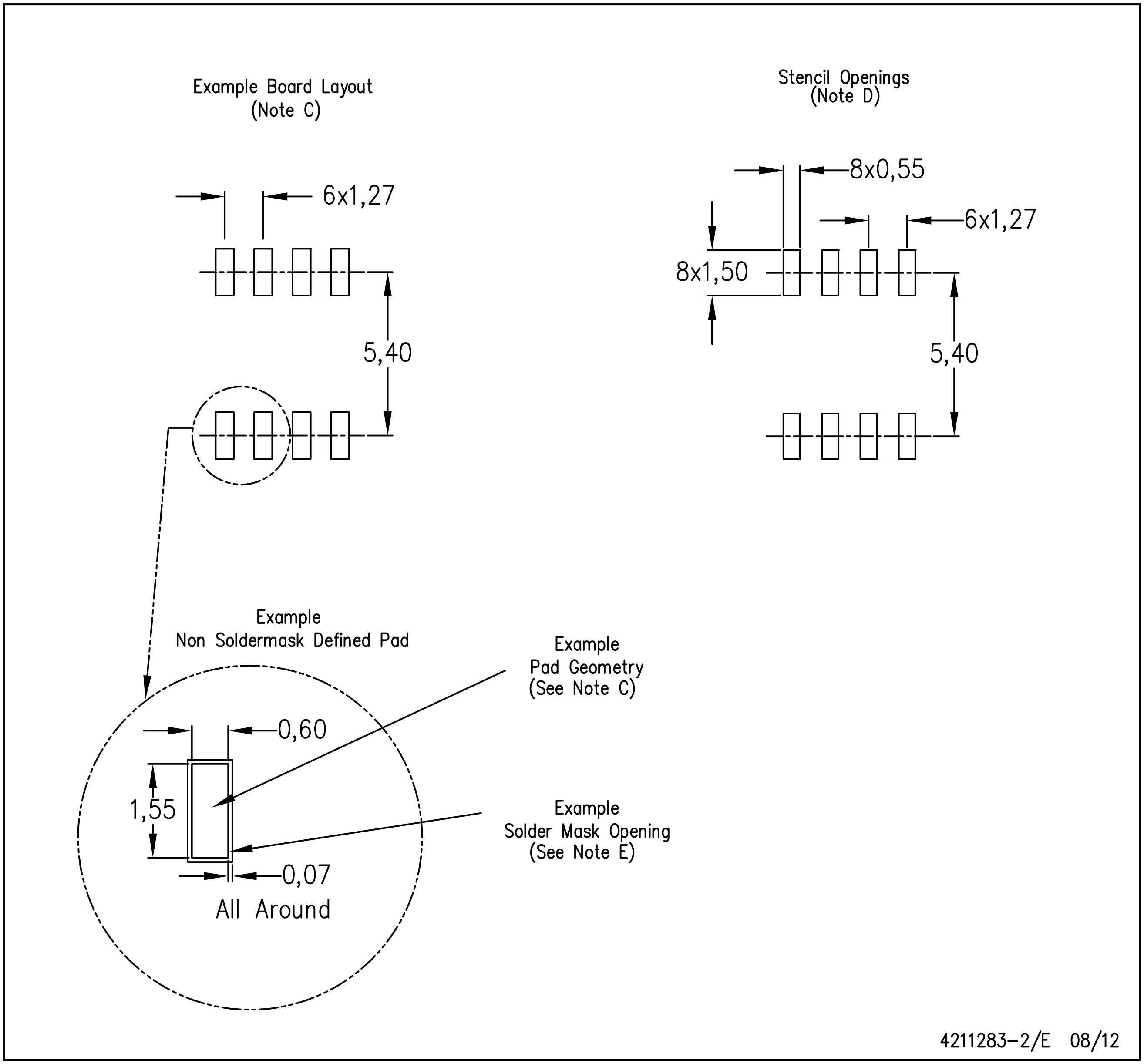
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



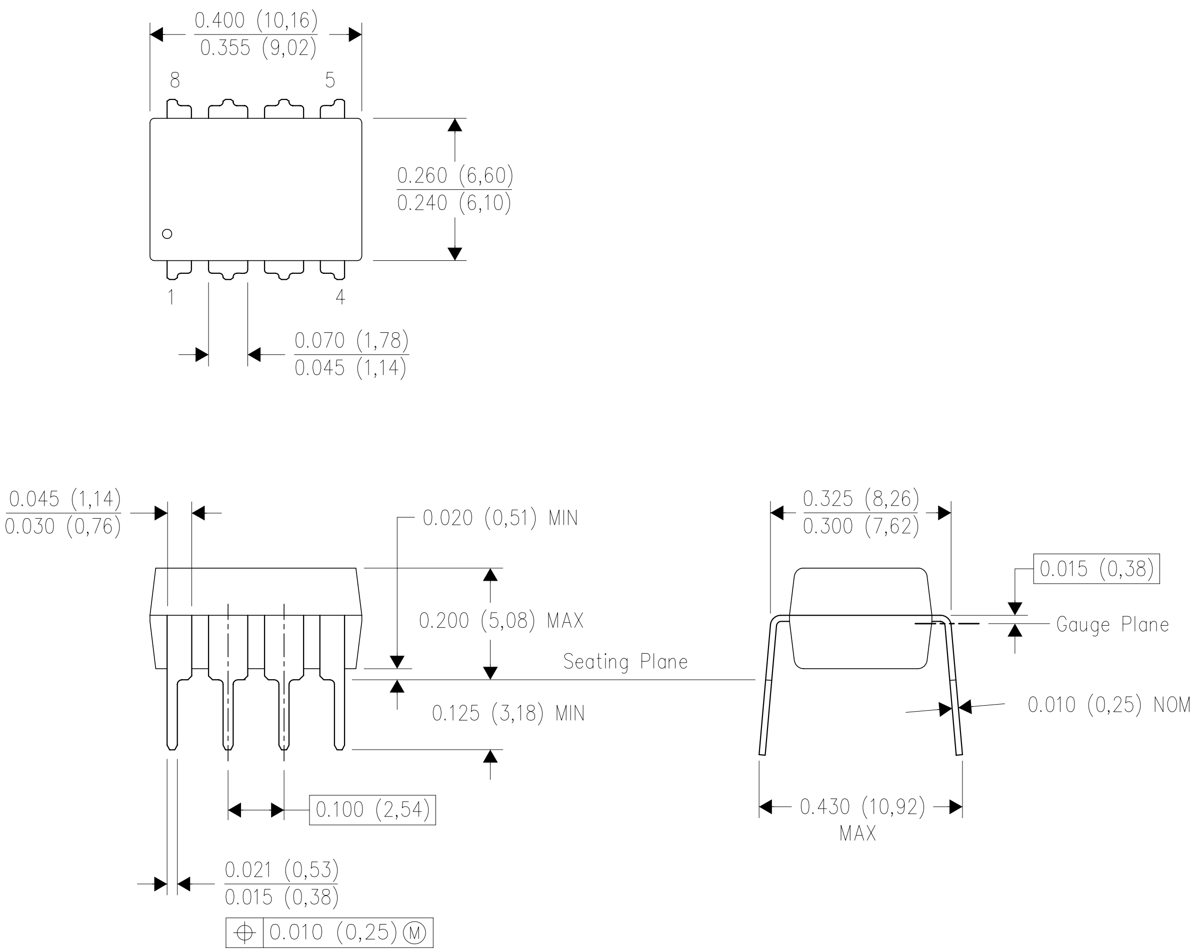
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

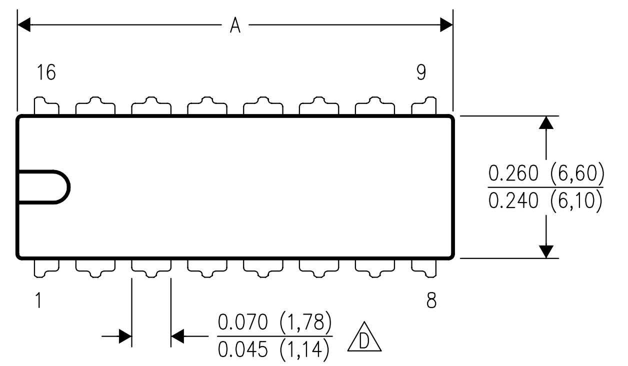


4040082/E 04/2010

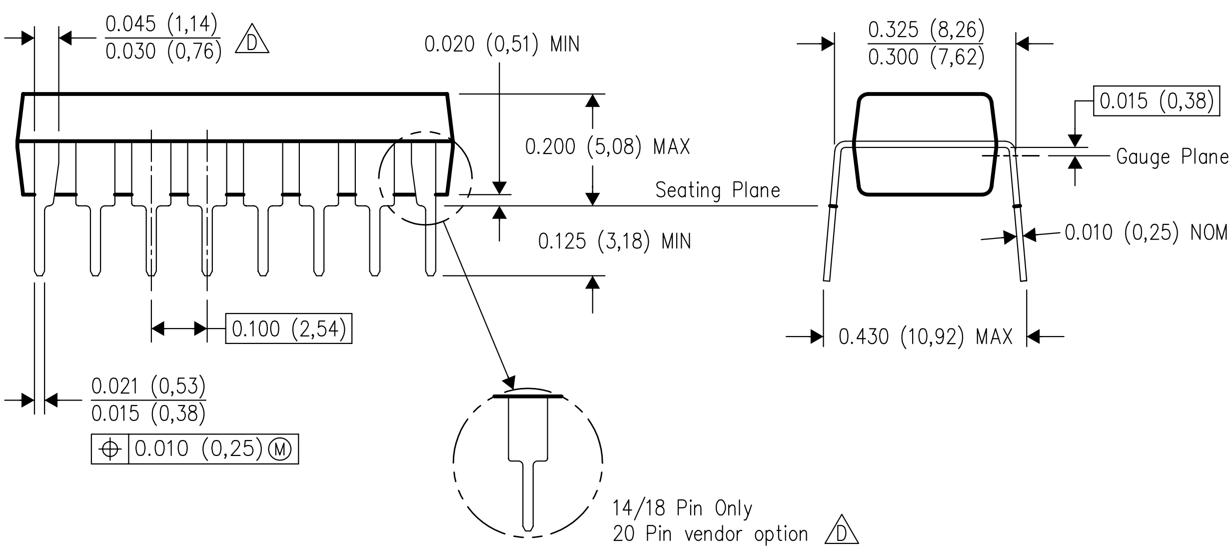
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



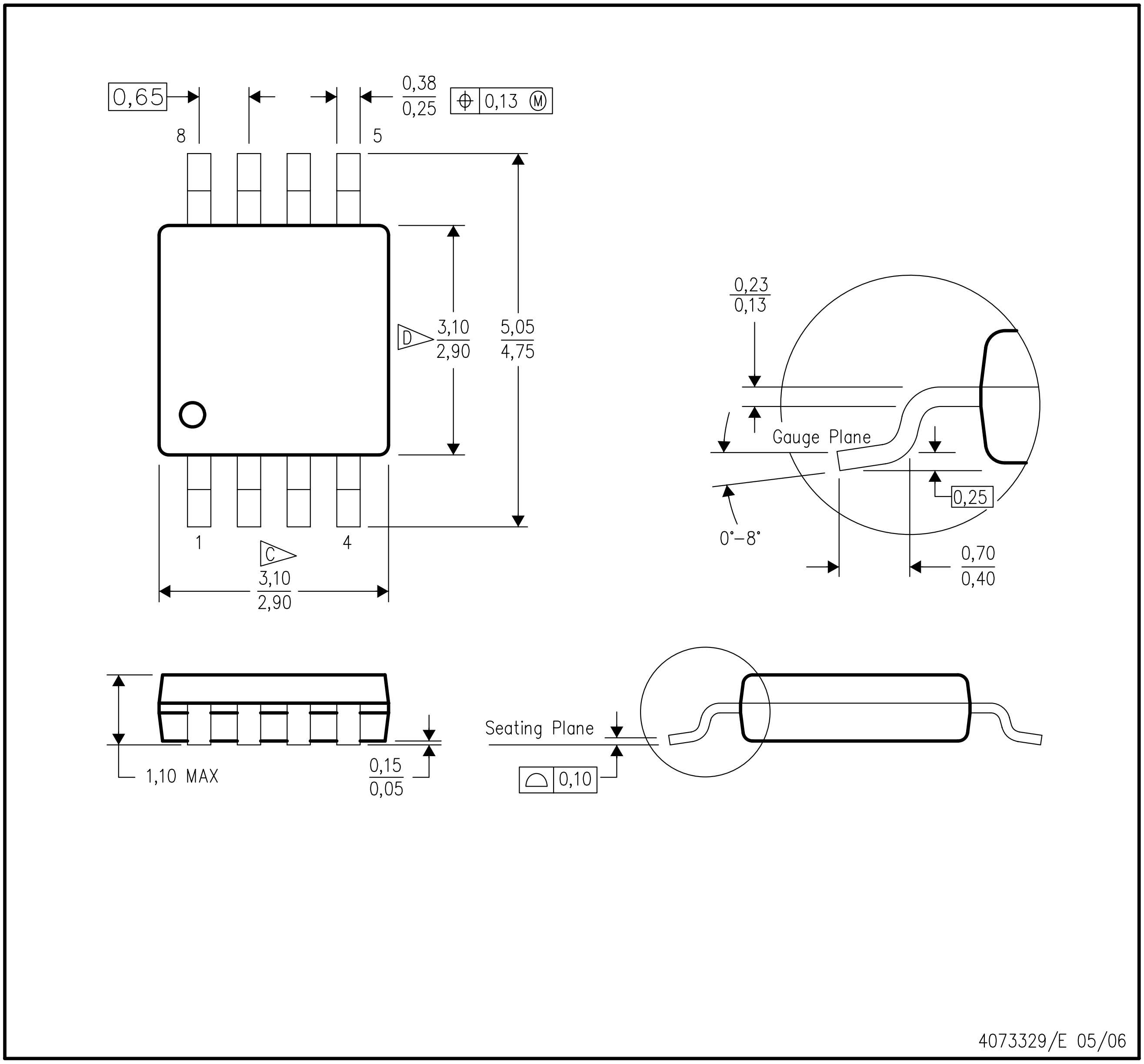
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

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