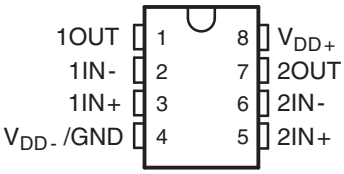
Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

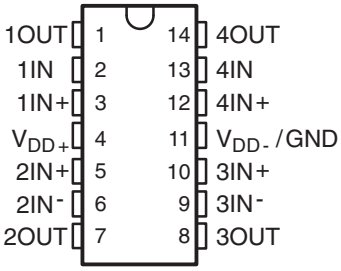
FEATURES

- **Qualified for Automotive Applications**
- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 12 nV/$\sqrt{Hz}$ Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Low Power . . . 500 μA Max**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage . . . 950 μV Max at T_A = 25°C**
- **Wide Supply Voltage Range . . . 2.7 V to 8 V**
- **Macromodel Included**

TLV2262A
PW PACKAGE
(TOP VIEW)



TLV2264A
PW PACKAGE
(TOP VIEW)



DESCRIPTION

The TLV2262 and TLV2264 are dual and quad low voltage operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single or split supply applications. The TLV226x family offers a compromise between the micropower TLV225x and the ac performance of the TLC227x. It has low supply current for battery-powered applications, while still having adequate ac performance for applications that demand it. This family is fully characterized at 3 V and 5 V and is optimized for low-voltage applications. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Figure 1 depicts the low level of noise voltage for this CMOS amplifier, which has only 200 μA (typ) of supply current per amplifier.

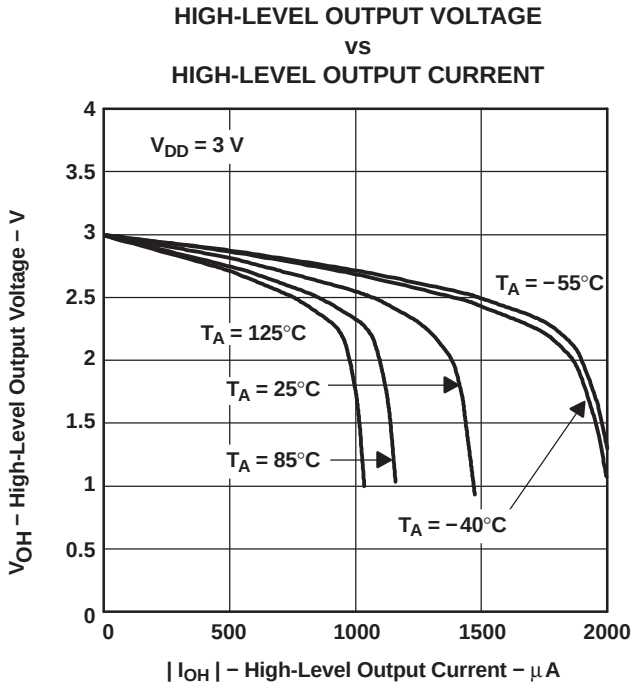


Figure 1.

The TLV226x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV226xA family is available and has a maximum input offset voltage of 950 μV.

The TLV2262/4 also makes great upgrades to the TLV2332/4 in standard designs. They offer increased output dynamic range, lower noise voltage and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442 devices. If your design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption make them ideal for high density, battery-powered equipment.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TSSOP – PW (8 pin)	Reel of 2000	TLV2262AQPWRQ1	TQ262A
	TSSOP – PW (14 pin)	Reel of 2000	TLV2264AQPWRQ1	P2264AQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)

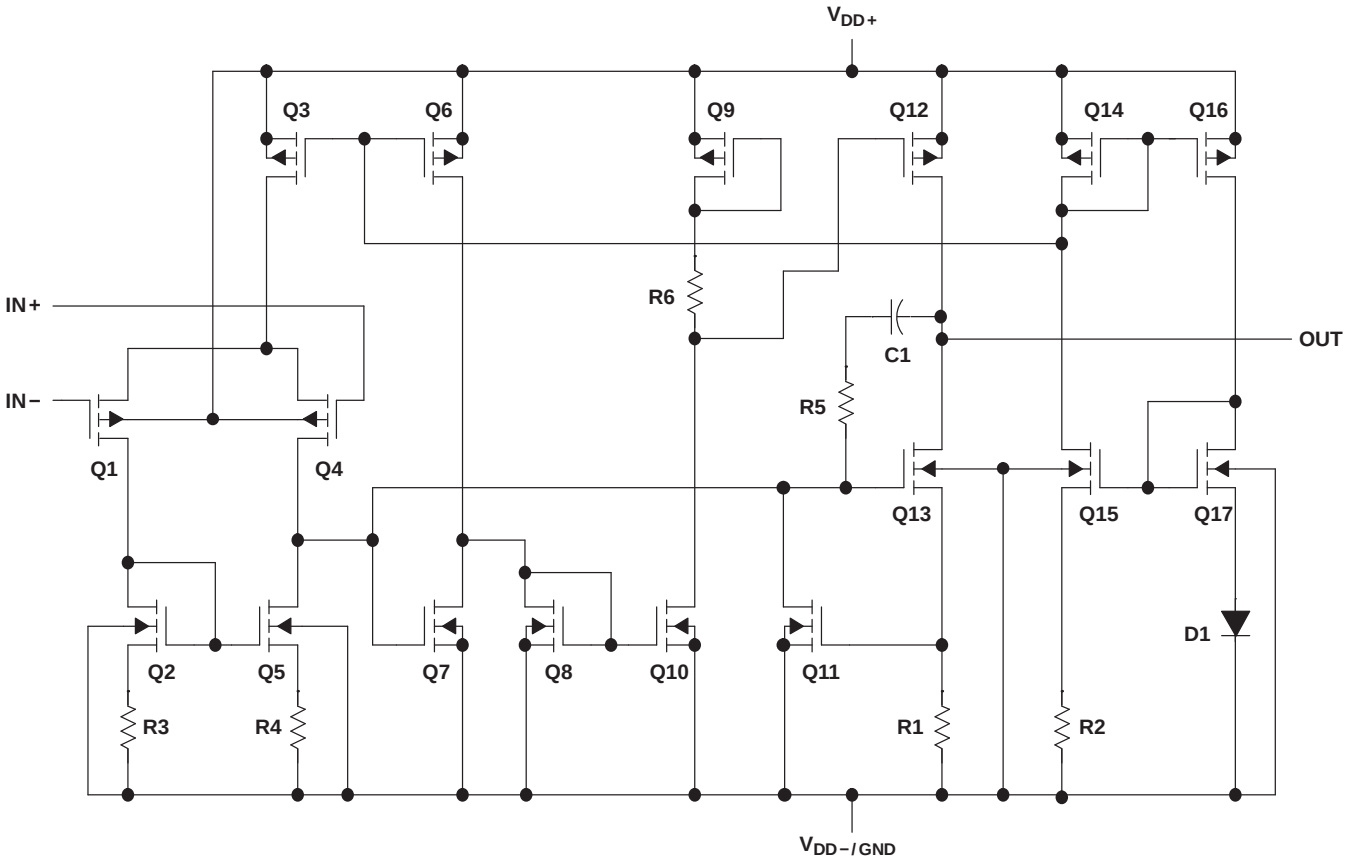


Table 1. Actual Device Component Count

COMPONENT	TLV2262	TLV2264
Transistors	38	76
Resistors	28	54
Diodes	9	18
Capacitors	3	6

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Supply voltage(2)	–0.3 V to 16 V
V_{ID}	Differential input voltage(3)	$\pm V_{DD}$
V_I	Input voltage range	(V_{DD-} – 0.3 V) to V_{DD+}
I_I	Input current, any input	±5 mA
I_O	Output current	±50 mA
	Total current into V_{DD+}	±50 mA
	Total current out of V_{DD-}	±50 mA
	Duration of short-circuit current (at or below) 25°C(4)	Unlimited
P_D	Continuous total power dissipation	See Dissipation Rating Table
T_A	Operating free-air temperature range	–40°C to 125°C
T_{stg}	Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to V_{DD-}.
(3) Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below V_{DD-} – 0.3 V.
(4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
PW-8	525 mW	4.2 mW/°C	273 mW	105 mW
PW-14	700 mW	5.6 mW/°C	364 mW	140 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
$V_{DD\pm}$	Supply voltage(1)	2.7	8	V
V_I	Input voltage	V_{DD-}	V_{DD+} –1.3	V
V_{IC}	Common-mode input voltage	V_{DD-}	V_{DD+} –1.3	V
T_A	Operating free-air temperature	–40	125	°C

(1) All voltage values, except differential voltages, are with respect to V_{DD-}.

TLV2262A ELECTRICAL CHARACTERISTICS

V_{DD} = 3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	950	mV
				Full range			1500	
α_{VIO}	Temperature coefficient of input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C to 125°C		2		µV/°C
	Input offset voltage long-term drift(1)	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.003		µV/mo
I_{IO}	Input offset current	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.5	60	pA
				125°C			800	
I_{IB}	Input bias current	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		1	60	pA
				125°C			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, | V_{IO} | ≤ 5 mV		25°C	0 to 2	–0.3 to 2.2		V
				Full range	0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = –20 µA		25°C		2.99		V
		I_{OH} = –100 µA		25°C	2.85			
				Full range	2.82			
		I_{OH} = –400 µA		25°C	2.7			
				Full range	2.55			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V	I_{OL} = 50 µA	25°C		10		mV
			I_{OL} = 500 µA	25°C		100	150	
				Full range			165	
			I_{OL} = 1 mA	25°C		200	300	
				Full range			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 50 kΩ(2)	25°C	60	100		V/mV
				Full range	25			
			R_L = 1 MΩ(2)	25°C		100		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10		25°C		270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V, R_S = 50 Ω		25°C	65	77		dB
				Full range	60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2, No load		25°C	80	100		dB
				Full range	80			
I_{DD}	Supply current	V_O = 1.5 V, No load		25°C		400	500	µA
				Full range			500	

(1) Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(2) Referenced to 1.5 V

TLV2262A OPERATING CHARACTERISTICS

V_{DD} = 3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 1.7 V, R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C	0.35	0.55		V/µs
				Full range	0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.6		µV
		f = 0.1 Hz to 10 Hz		25°C		1		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ(1)	A_V = 1	25°C		0.03		%
			A_V = 10	25°C		0.05		
	Gain-bandwidth product	f = 1 kHz, R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C		0.67		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, A_V = 1, R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C		395		kHz
t_s	Settling time	A_V = –1, Step = 1 V to 2 V, R_L = 50 kΩ(1), C_L = 100 pF(1)	To 0.1%	25°C		5.6		µs
			To 0.01%	25°C		12.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C		55		°
G_m	Gain margin	R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C		11		dB

(1) Referenced to 1.5 V

TLV2262A ELECTRICAL CHARACTERISTICS

V_{DD} = 5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	950	mV
				Full range			1500	
α_{VIO}	Temperature coefficient of input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C to 125°C		2		µV/°C
	Input offset voltage long-term drift(1)	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.003		µV/mo
I_{IO}	Input offset current	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.5	60	pA
				125°C			800	
I_{IB}	Input bias current	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		1	60	pA
				125°C			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, | V_{IO} | ≤ 5 mV		25°C	0 to 4	–0.3 to 4.2		V
				Full range	0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = –20 µA		25°C		4.99		V
		I_{OH} = –100 µA		25°C	4.85	4.94		
				Full range	4.82			
		I_{OH} = –400 µA		25°C	4.7	4.85		
				Full range	4.5			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V	I_{OL} = 50 µA	25°C		0.01		V
			I_{OL} = 500 µA	25°C		0.09	0.15	
				Full range			0.15	
			I_{OL} = 1 mA	25°C		0.2	0.3	
				Full range			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ(2)	25°C	80	170		V/mV
				Full range	50			
			R_L = 1 MΩ(2)	25°C		550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10		25°C		240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	83		dB
				Full range	70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, No load		25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 2.5 V, No load		25°C		400	500	µA
				Full range			500	

(1) Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(2) Referenced to 2.5 V

TLV2262A OPERATING CHARACTERISTICS

V_{DD} = 5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C	0.35	0.55		V/µs
				Full range	0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ(1)	A_V = 1	25°C		0.017		%
			A_V = 10	25°C		0.03		
	Gain-bandwidth product	f = 50 kHz, R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C		0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C		185		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ(1), C_L = 100 pF(1)	To 0.1%	25°C		6.4		µs
			To 0.01%	25°C		14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C		56		°
G_m	Gain margin	R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C		11		dB

(1) Referenced to 2.5 V

TLV2264A ELECTRICAL CHARACTERISTICS

V_{DD} = 3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	950	mV
				Full range			1500	
α_{VIO}	Temperature coefficient of input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C to 125°C		2		µV/°C
	Input offset voltage long-term drift(1)	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.003		µV/mo
I_{IO}	Input offset current	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.5	60	pA
				125°C			800	
I_{IB}	Input bias current	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		1	60	pA
				125°C			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, | V_{IO} | ≤ 5 mV		25°C	0 to 2	–0.3 to 2.2		V
				Full range	0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = –20 µA		25°C		2.99		V
		I_{OH} = –100 µA		25°C	2.85			
				Full range	2.82			
		I_{OH} = –400 µA		25°C	2.7			
				Full range	2.6			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V	I_{OL} = 50 µA	25°C		10		mV
			I_{OL} = 500 µA	25°C		100	150	
				Full range			150	
			I_{OL} = 1 mA	25°C		200	300	
				Full range			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 50 kΩ(2)	25°C	60	100		V/mV
				Full range	25			
			R_L = 1 MΩ(2)	25°C		100		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10		25°C		270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V, R_S = 50 Ω		25°C	65	77		dB
				Full range	60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2, No load		25°C	80	100		dB
				Full range	80			
I_{DD}	Supply current	V_O = 1.5 V, No load		25°C		0.8	1	mA
				Full range			1	

(1) Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(2) Referenced to 1.5 V

TLV2264A OPERATING CHARACTERISTICS

V_{DD} = 3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 1.7 V, R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C	0.35	0.55		V/µs
				Full range	0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.6		µV
		f = 0.1 Hz to 10 Hz		25°C		1		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ(1)	A_V = 1	25°C		0.03		%
			A_V = 10	25°C		0.05		
	Gain-bandwidth product	f = 1 kHz, R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C		0.67		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, A_V = 1, R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C		395		kHz
t_s	Settling time	A_V = –1, Step = 1 V to 2 V, R_L = 50 kΩ(1), C_L = 100 pF(1)	To 0.1%	25°C		5.6		µs
			To 0.01%	25°C		12.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C		55		°
G_m	Gain margin	R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C		11		dB

(1) Referenced to 1.5 V

TLV2264A ELECTRICAL CHARACTERISTICS

V_{DD} = 5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	950	mV
				Full range			1500	
α_{VIO}	Temperature coefficient of input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C to 125°C		2		µV/°C
	Input offset voltage long-term drift(1)	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.003		µV/mo
I_{IO}	Input offset current	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.5	60	pA
				125°C			800	
I_{IB}	Input bias current	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		1	60	pA
				125°C			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, | V_{IO} | ≤ 5 mV		25°C	0 to 4	–0.3 to 4.2		V
				Full range	0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = –20 µA		25°C		4.99		V
		I_{OH} = –100 µA		25°C	4.85	4.94		
				Full range	4.82			
		I_{OH} = –400 µA		25°C	4.7	4.85		
				Full range	4.5			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V	I_{OL} = 50 µA	25°C		0.01		V
			I_{OL} = 500 µA	25°C		0.09	0.15	
				Full range			0.15	
			I_{OL} = 1 mA	25°C		0.2	0.3	
				Full range			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ(2)	25°C	80	170		V/mV
				Full range	50			
			R_L = 1 MΩ(2)	25°C		550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10		25°C		240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	83		dB
				Full range	70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, No load		25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 2.5 V, No load		25°C		0.8	1	mA
				Full range			1	

(1) Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(2) Referenced to 2.5 V

TLV2264A OPERATING CHARACTERISTICS

V_{DD} = 5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C	0.35	0.55		V/µs
				Full range	0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ(1)	A_V = 1	25°C		0.017		%
			A_V = 10	25°C		0.03		
	Gain-bandwidth product	f = 50 kHz, R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C		0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C		185		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ(1), C_L = 100 pF(1)	To 0.1%	25°C		6.4		µs
			To 0.01%	25°C		14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C		56		°
G_m	Gain margin	R_L = 50 kΩ(1), C_L = 100 pF(1)		25°C		11		dB

(1) Referenced to 2.5 V

TYPICAL CHARACTERISTICS

For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V. Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	2–5
		vs Common–mode voltage	6, 7
α_{VIO}	Input offset voltage temperature coefficient	Distribution	8–11
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free–air temperature	12
V_I	Input voltage	vs Supply voltage	13
		vs Free–air temperature	14
V_{OH}	High-level output voltage	vs High-level output current	15, 18
V_{OL}	Low-level output voltage	vs Low-level output current	16, 17, 19
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	20
I_{OS}	Short-circuit output current	vs Supply voltage	21
		vs Free-air temperature	22
V_{ID}	Differential input voltage	vs Output voltage	23, 24
A_{VD}	Differential voltage amplification	vs Load resistance	25
A_{VD}	Large-signal differential voltage amplification	vs Frequency	26, 27
		vs Free-air temperature	28, 29
z_o	Output impedance	vs Frequency	30, 31
CMRR	Common-mode rejection ratio	vs Frequency	32
		vs Free-air temperature	33
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	34, 35
		vs Free-air temperature	36, 37
I_{DD}	Supply current	vs Free-air temperature	38, 39
SR	Slew rate	vs Load capacitance	40
		vs Free-air temperature	41
V_O	Inverting large-signal pulse response		42, 43
V_O	Voltage-follower large-signal pulse response		44, 45
V_O	Inverting small-signal pulse response		46, 47
V_O	Voltage-follower small-signal pulse response		48, 49
V_n	Equivalent input noise voltage	vs Frequency	50, 51
	Input noise voltage	Over a 10-second period	52
	Integrated noise voltage	vs Frequency	53
THD+N	Total harmonic distortion plus noise	vs Frequency	54
	Gain-bandwidth product	vs Supply voltage	55
		vs Free-air temperature	56
ϕ_m	Phase margin	vs Frequency	26, 27
		vs Load capacitance	57
G_m	Gain margin	vs Load capacitance	58
B_1	Unity-gain bandwidth	vs Load capacitance	59
	Overestimation of phase margin	vs Load capacitance	60

DISTRIBUTION OF TLV2262
INPUT OFFSET VOLTAGE

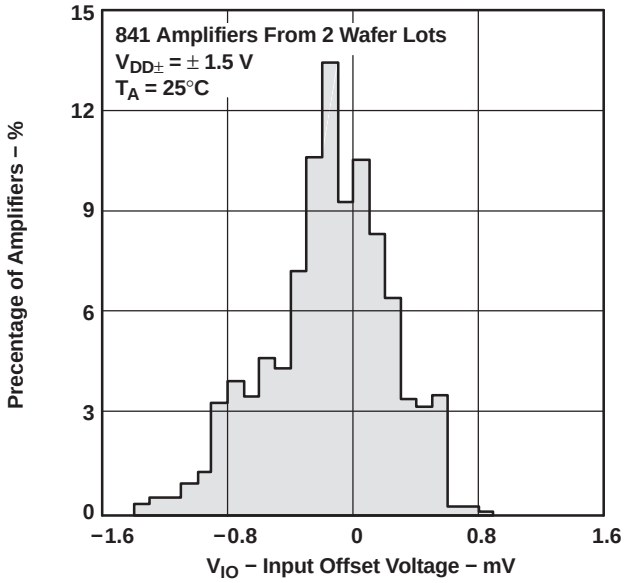


Figure 2.

DISTRIBUTION OF TLV2262
INPUT OFFSET VOLTAGE

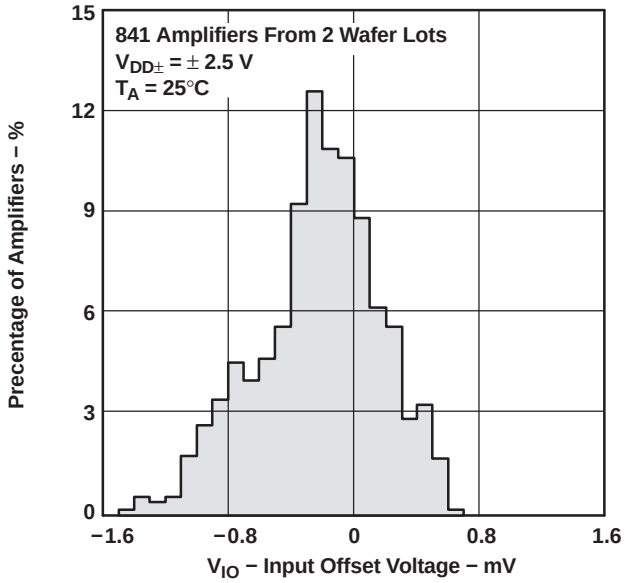


Figure 3.

DISTRIBUTION OF TLV2264
INPUT OFFSET VOLTAGE

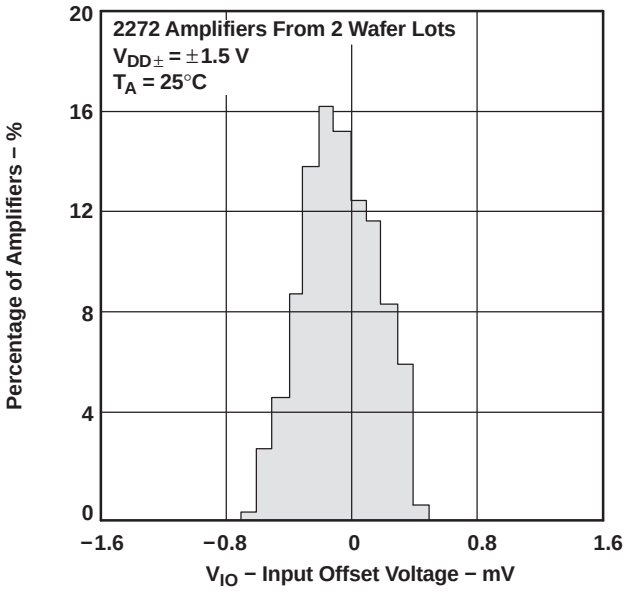


Figure 4.

DISTRIBUTION OF TLV2264
INPUT OFFSET VOLTAGE

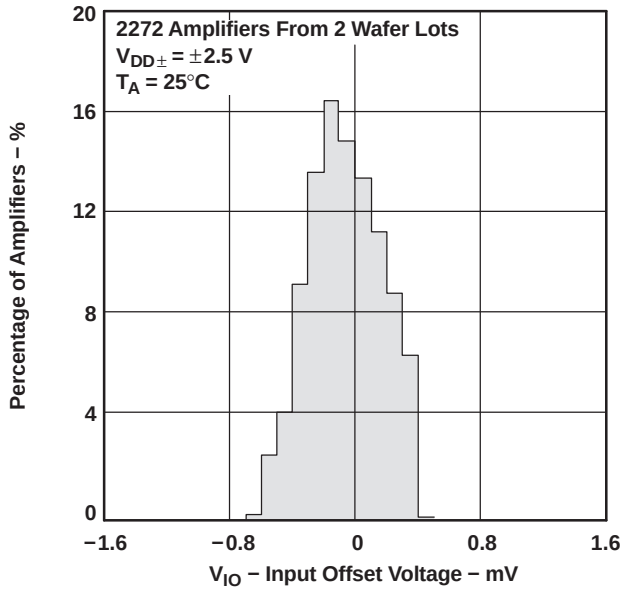


Figure 5.

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

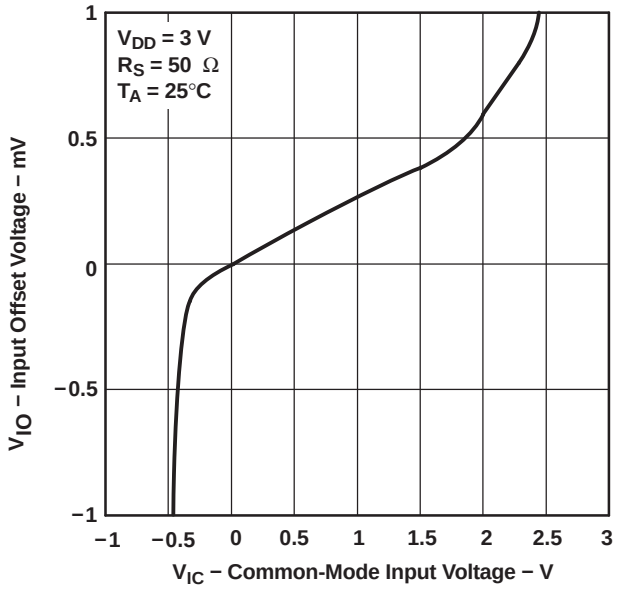


Figure 6.

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

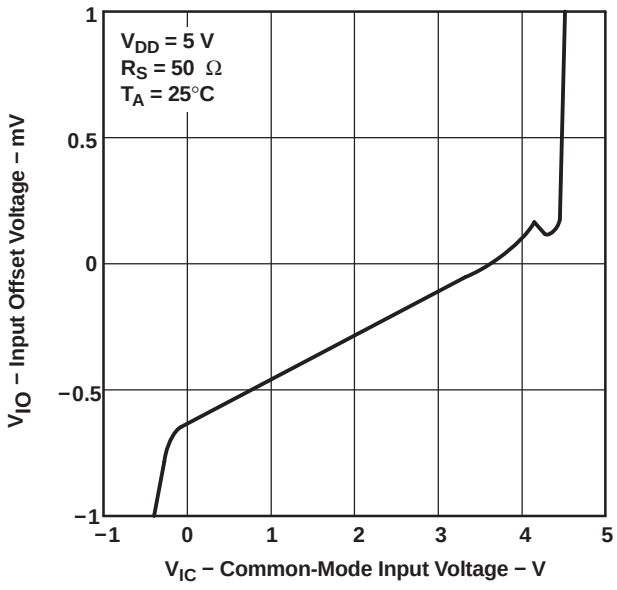


Figure 7.

DISTRIBUTION OF TLV2262 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT

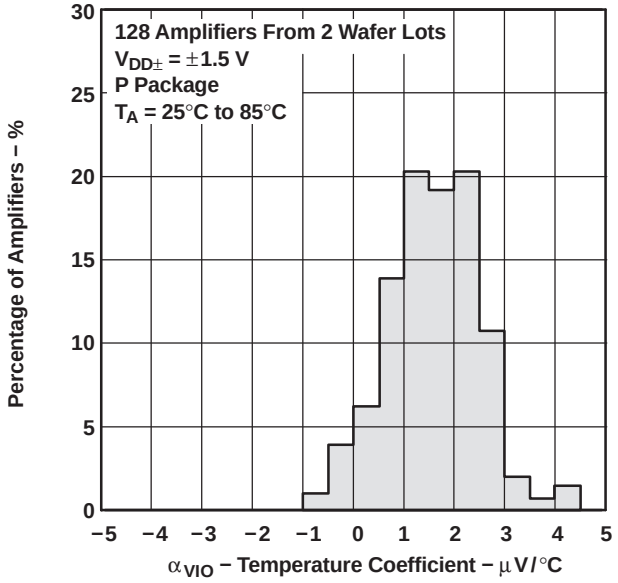


Figure 8.

DISTRIBUTION OF TLV2262 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT

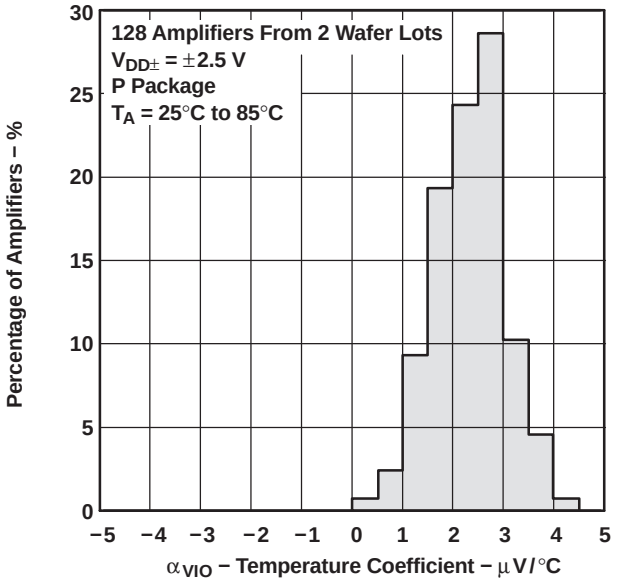


Figure 9.

DISTRIBUTION OF TLV2264 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

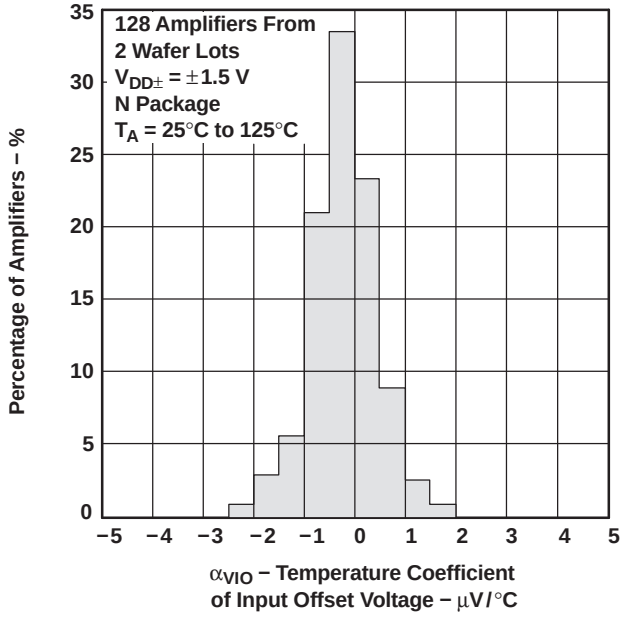


Figure 10.

DISTRIBUTION OF TLV2264 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

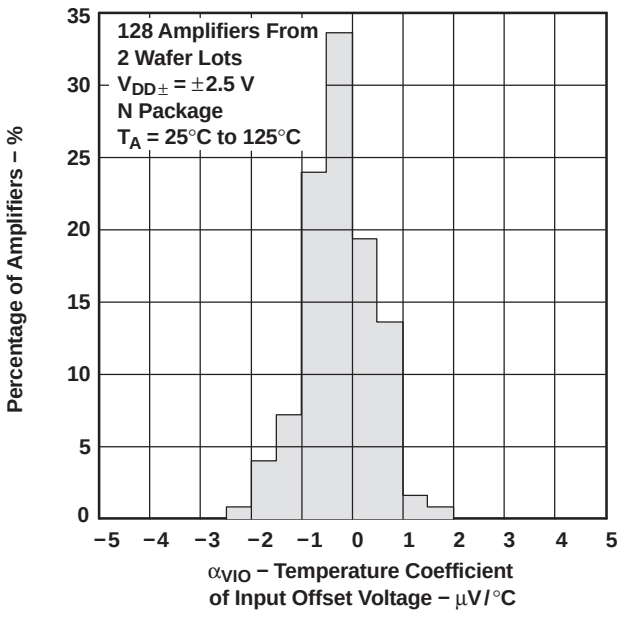


Figure 11.

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

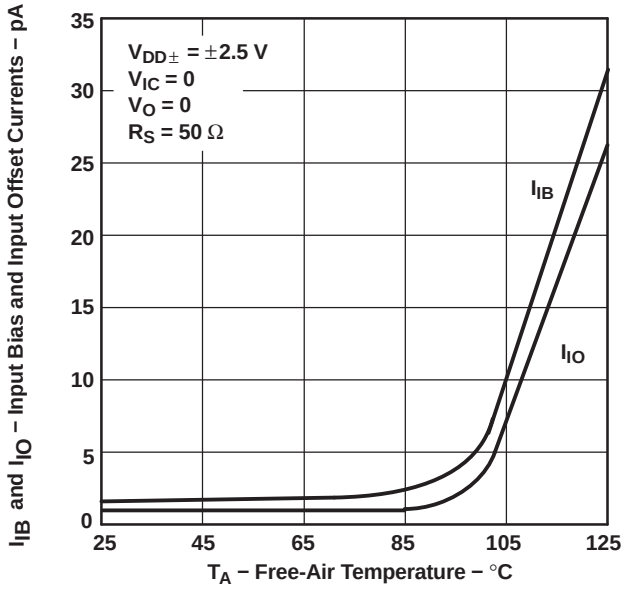


Figure 12.

INPUT VOLTAGE vs SUPPLY VOLTAGE

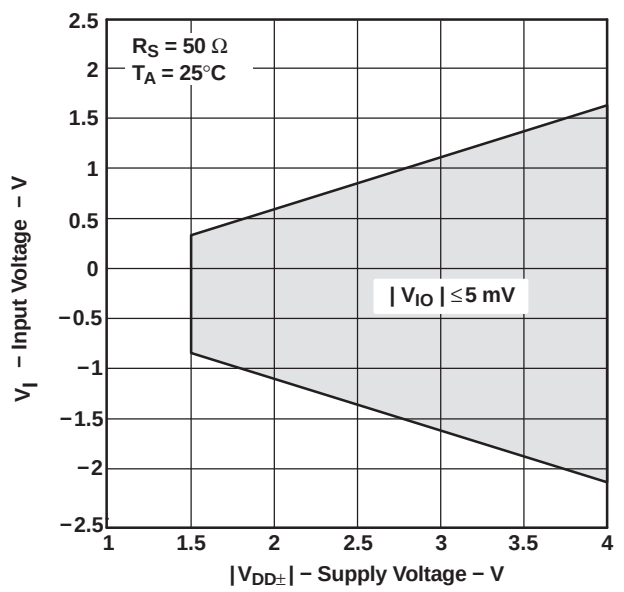


Figure 13.

INPUT VOLTAGE vs FREE-AIR TEMPERATURE

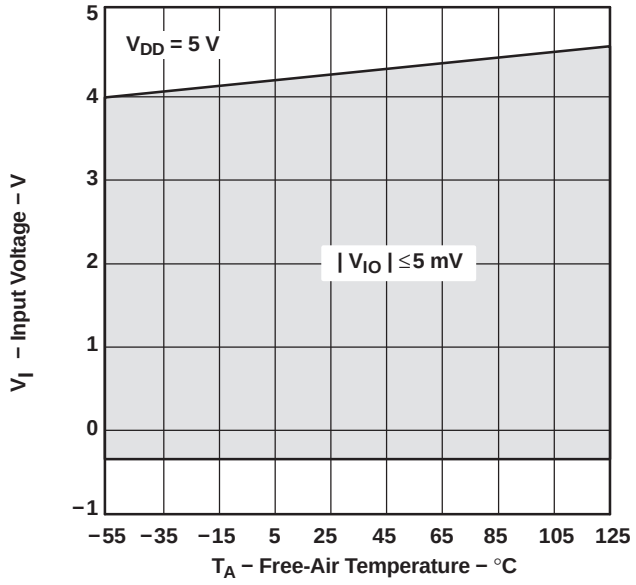


Figure 14.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

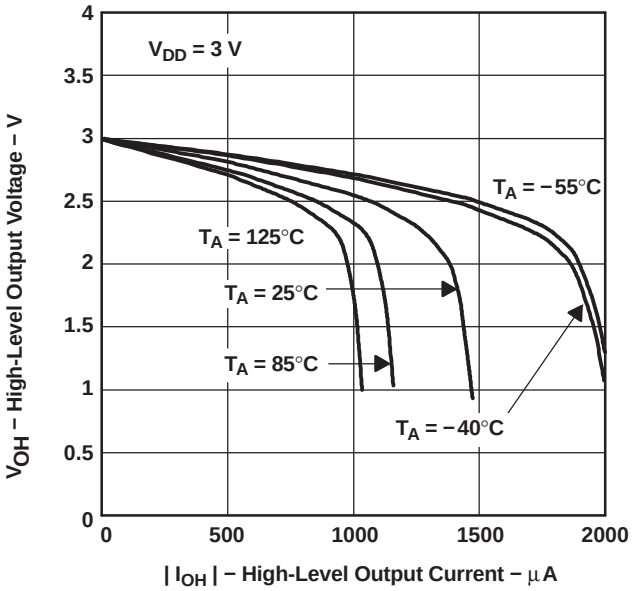


Figure 15.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

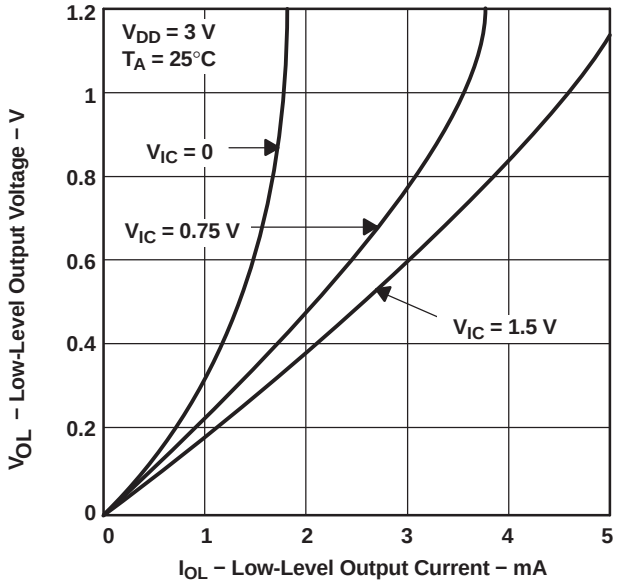


Figure 16.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

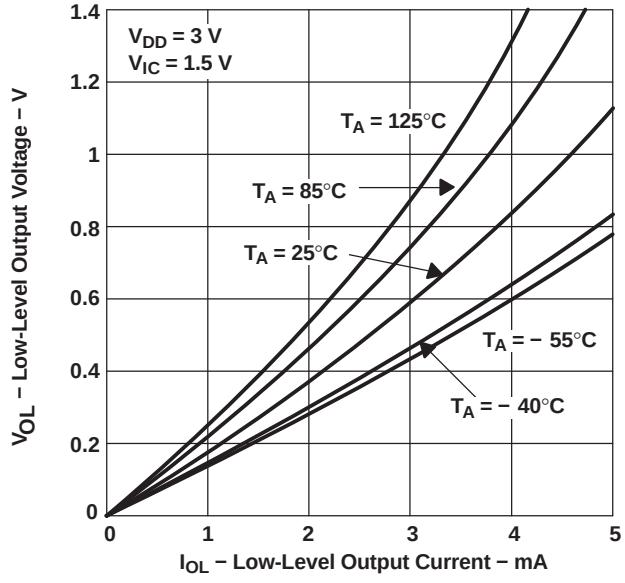


Figure 17.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

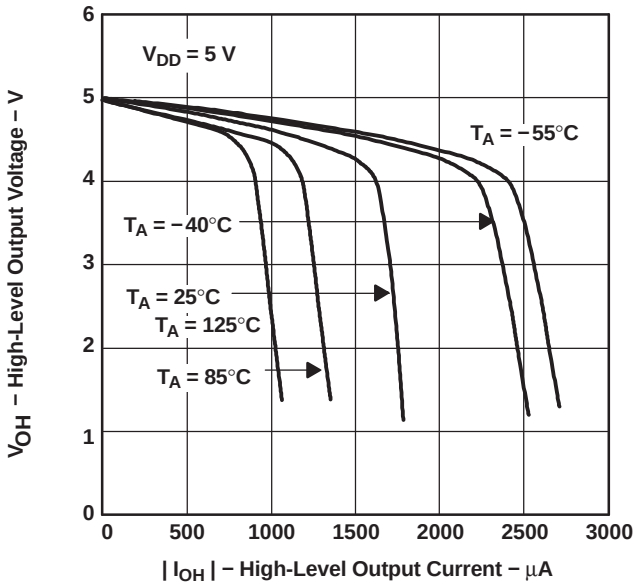


Figure 18.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

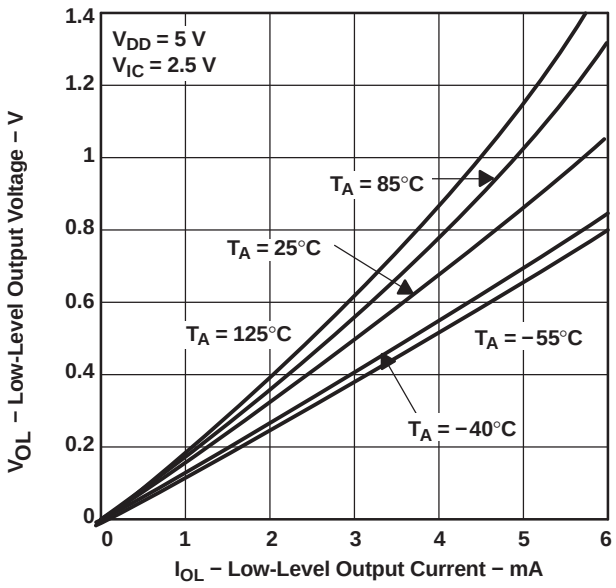


Figure 19.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

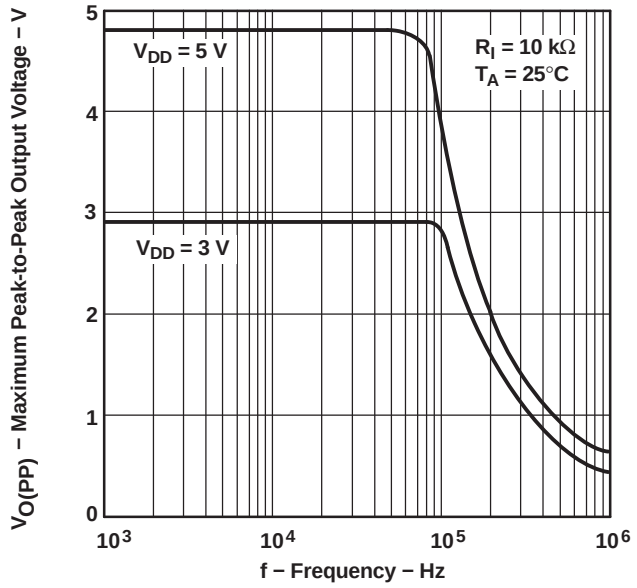


Figure 20.

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

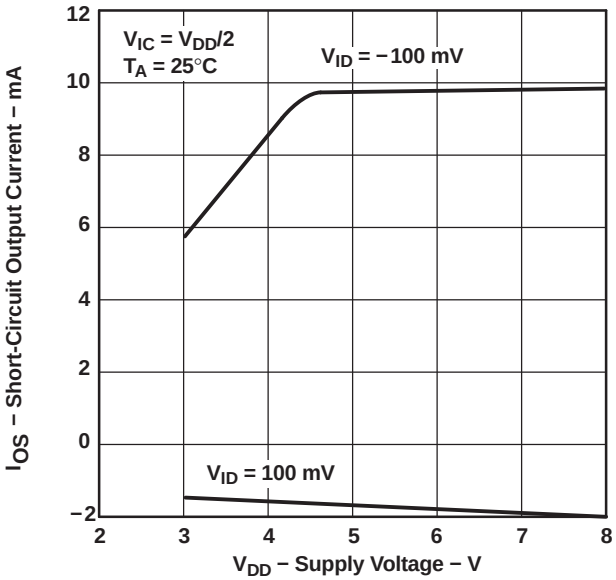


Figure 21.

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

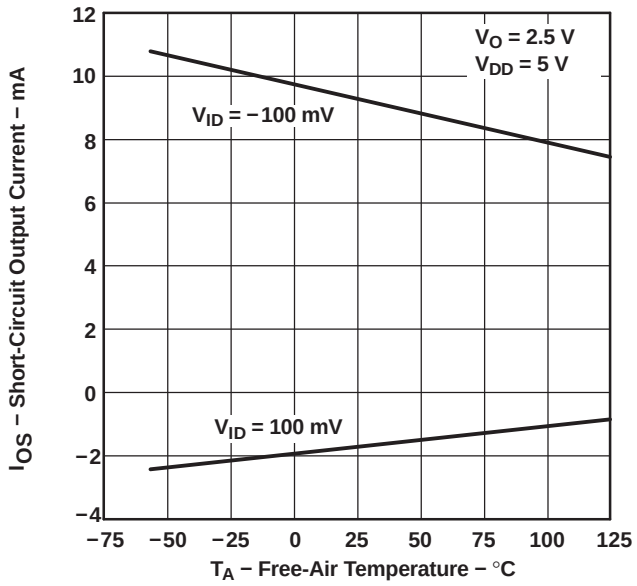


Figure 22.

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

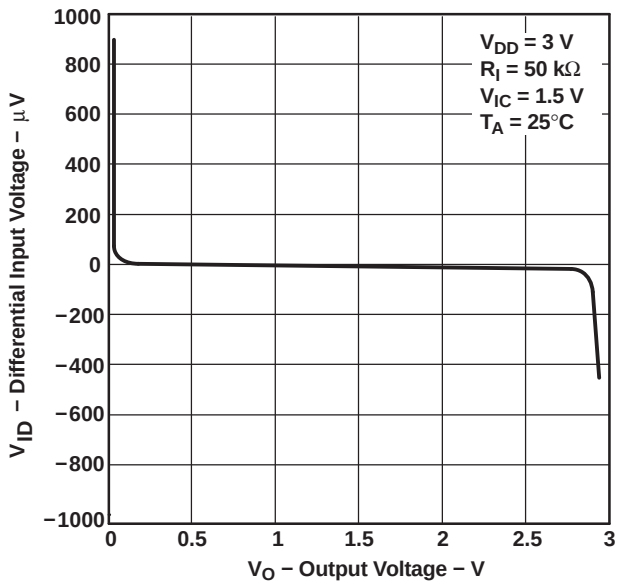


Figure 23.

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

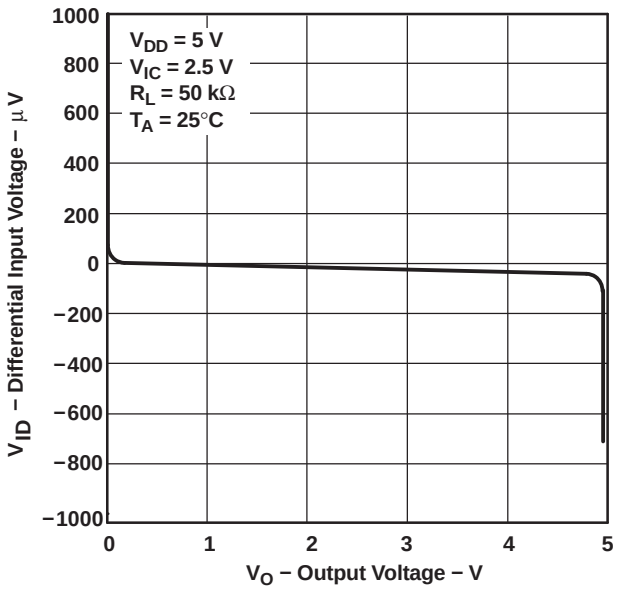


Figure 24.

DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

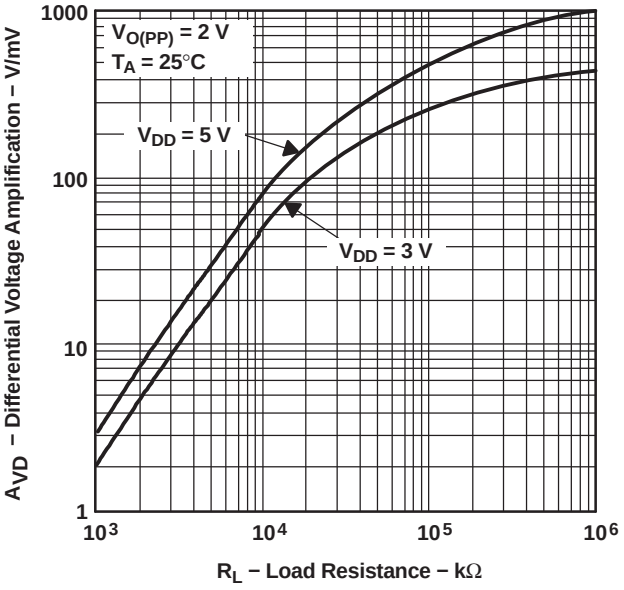


Figure 25.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

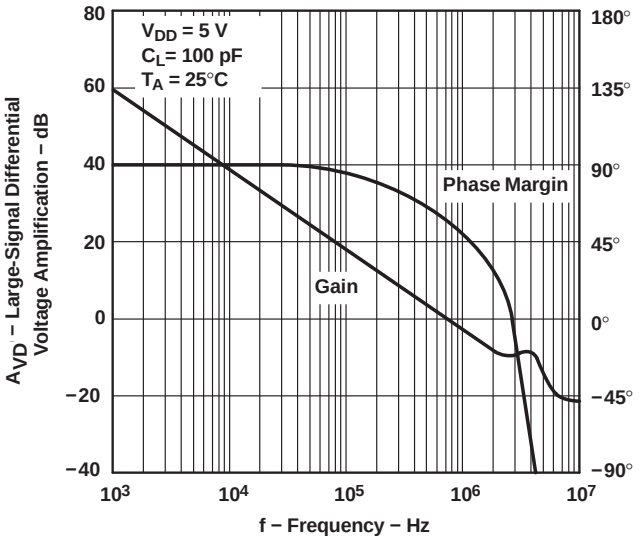


Figure 26.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

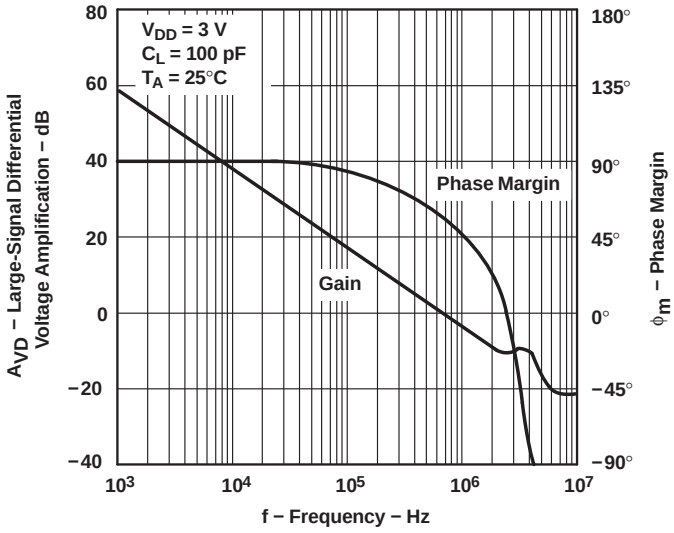


Figure 27.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

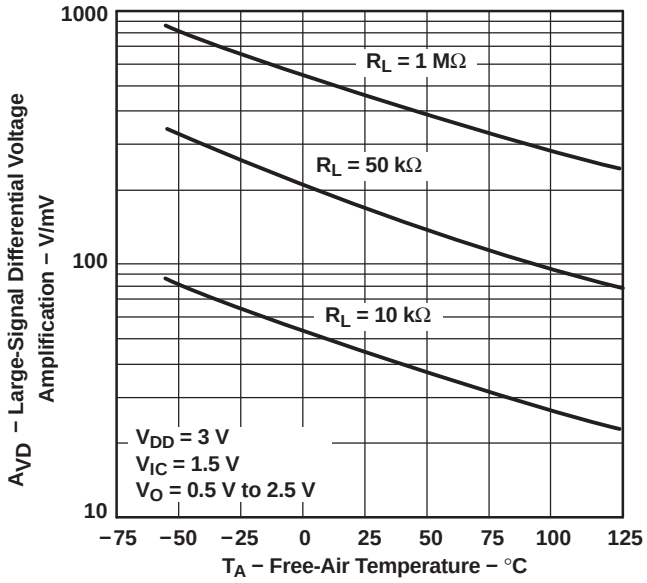


Figure 28.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

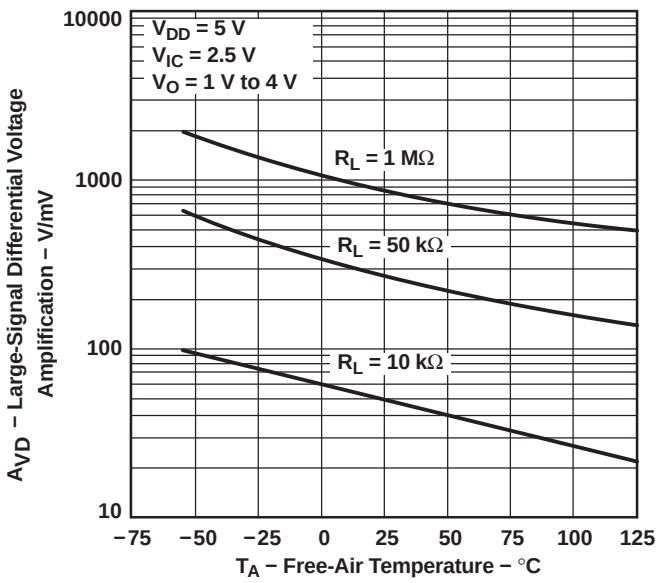


Figure 29.

OUTPUT IMPEDANCE vs FREQUENCY

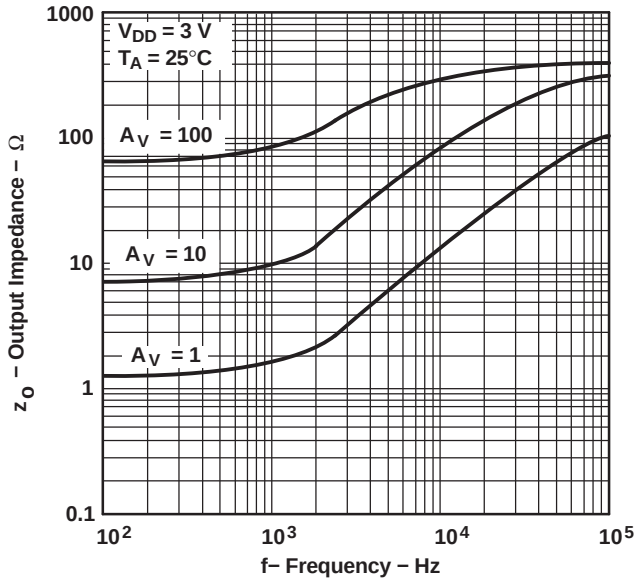


Figure 30.

OUTPUT IMPEDANCE vs FREQUENCY

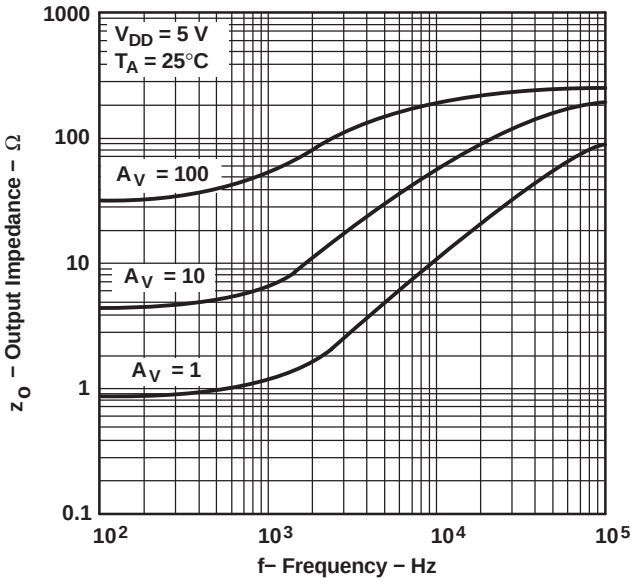


Figure 31.

COMMON-MODE REJECTION RATIO vs FREQUENCY

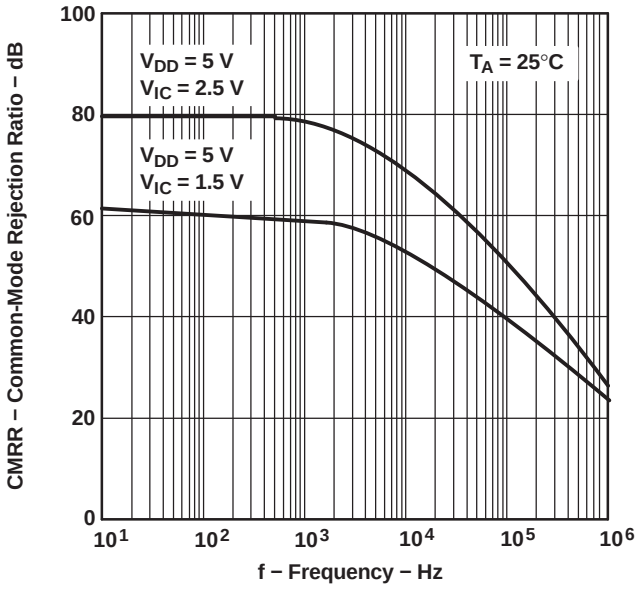


Figure 32.

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

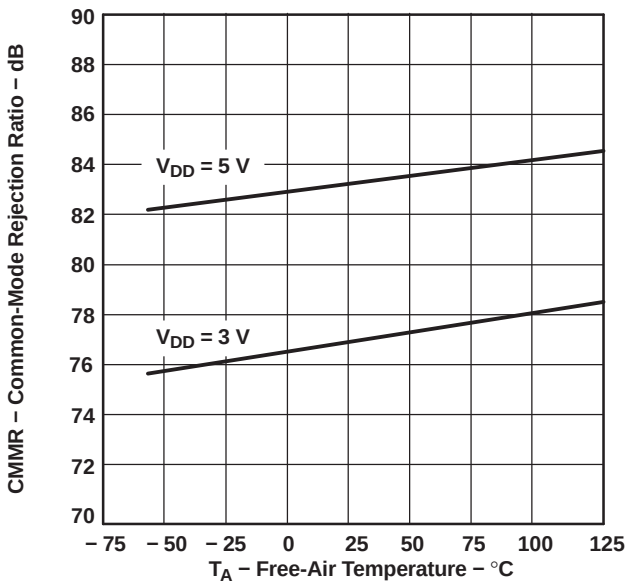


Figure 33.

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

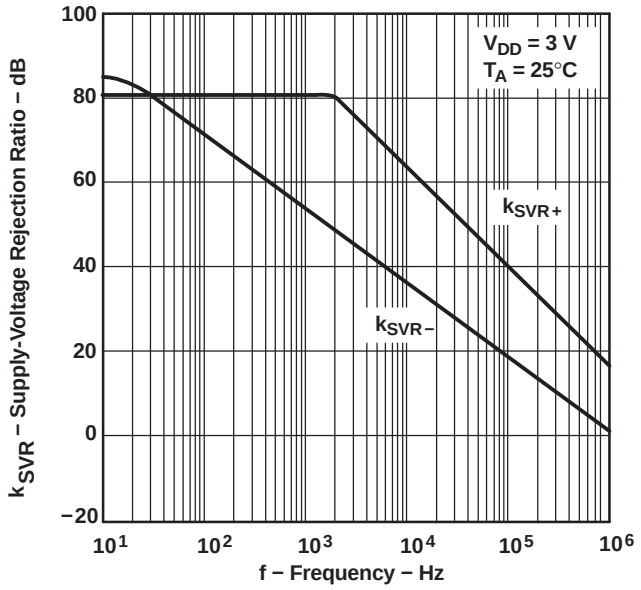


Figure 34.

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

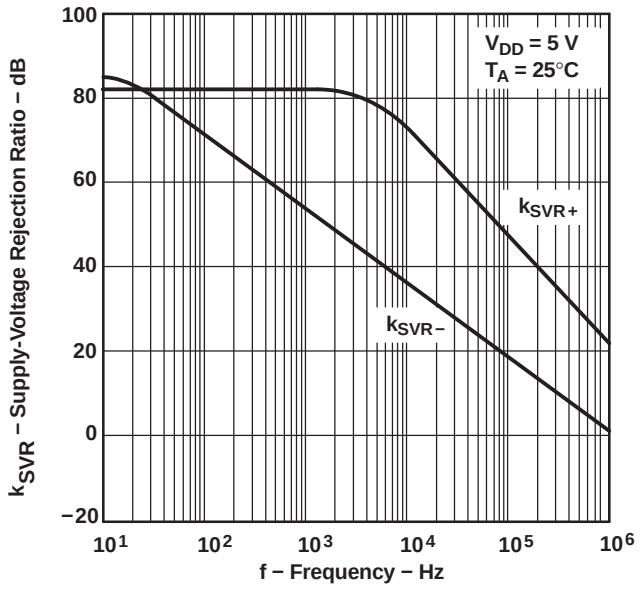


Figure 35.

TLV2262
SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

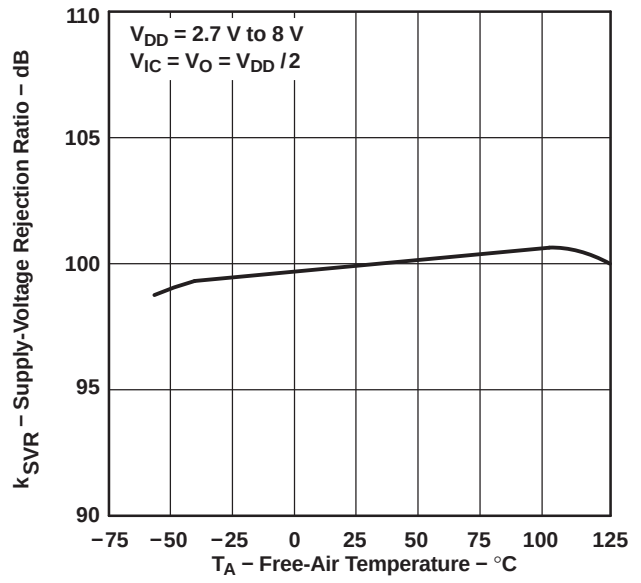


Figure 36.

TLV2264
SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

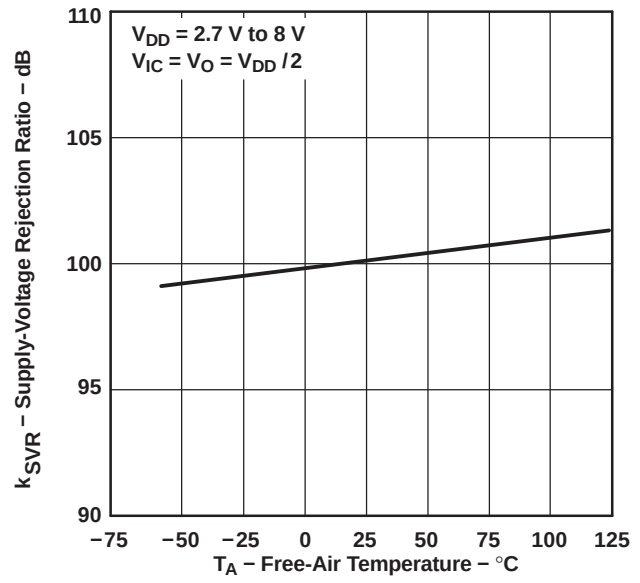


Figure 37.

TLV2262
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

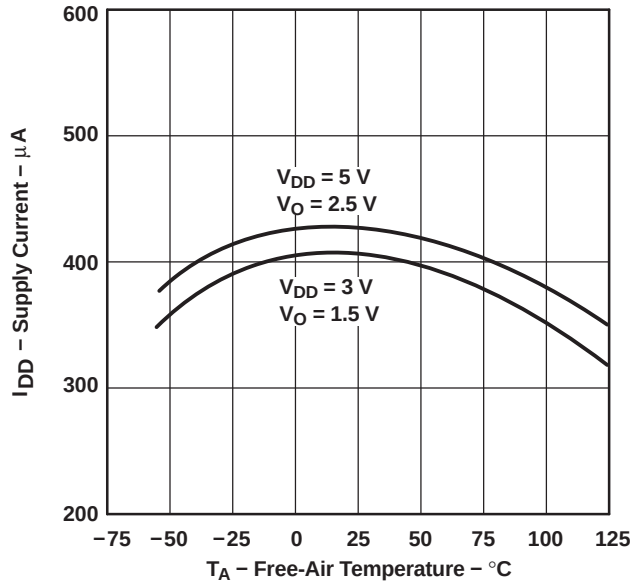


Figure 38.

TLV2264
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

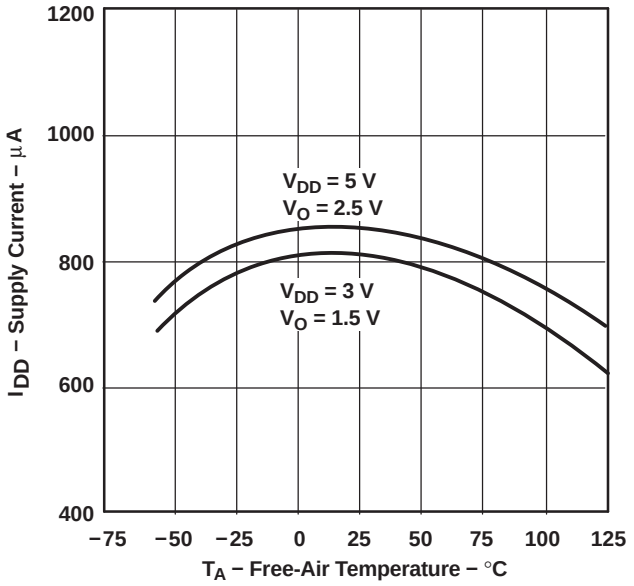


Figure 39.

SLEW RATE
vs
LOAD CAPACITANCE

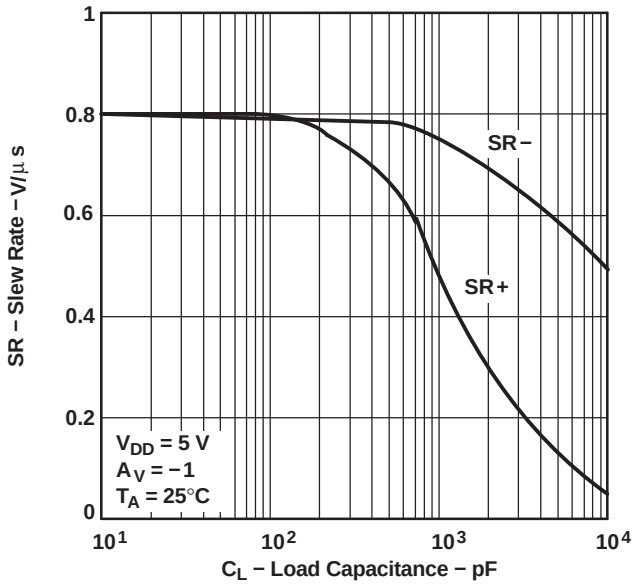


Figure 40.

SLEW RATE
vs
FREE-AIR TEMPERATURE

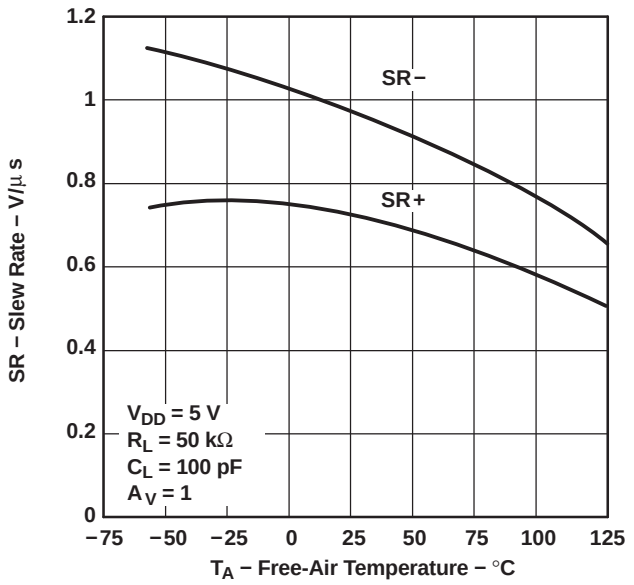


Figure 41.

INVERTING LARGE-SIGNAL PULSE RESPONSE

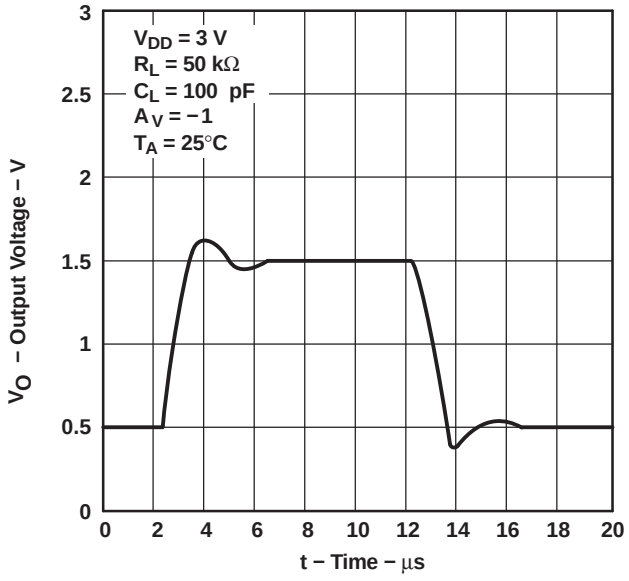


Figure 42.

INVERTING LARGE-SIGNAL PULSE RESPONSE

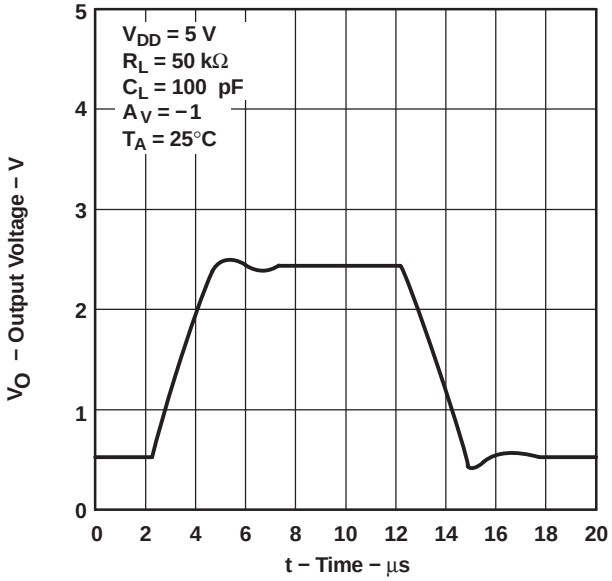


Figure 43.

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

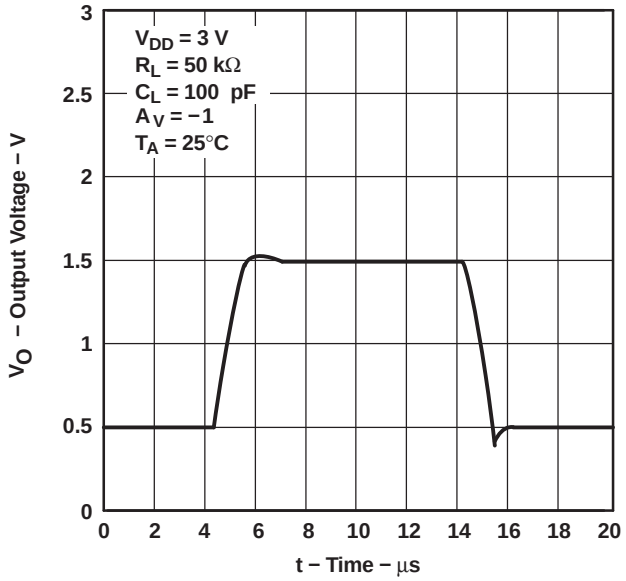


Figure 44.

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

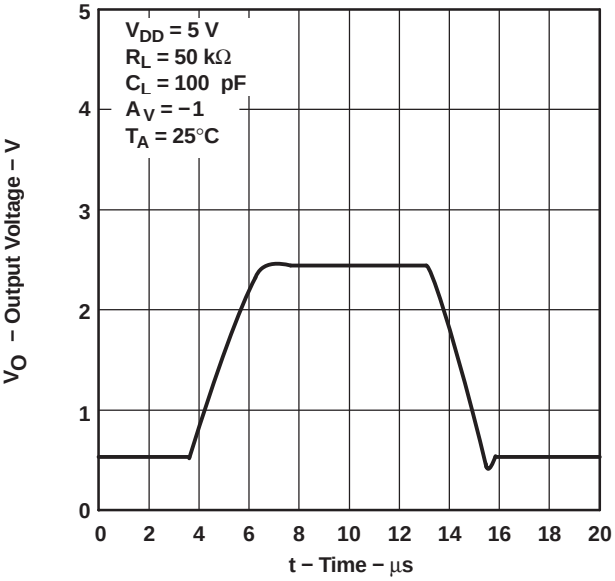


Figure 45.

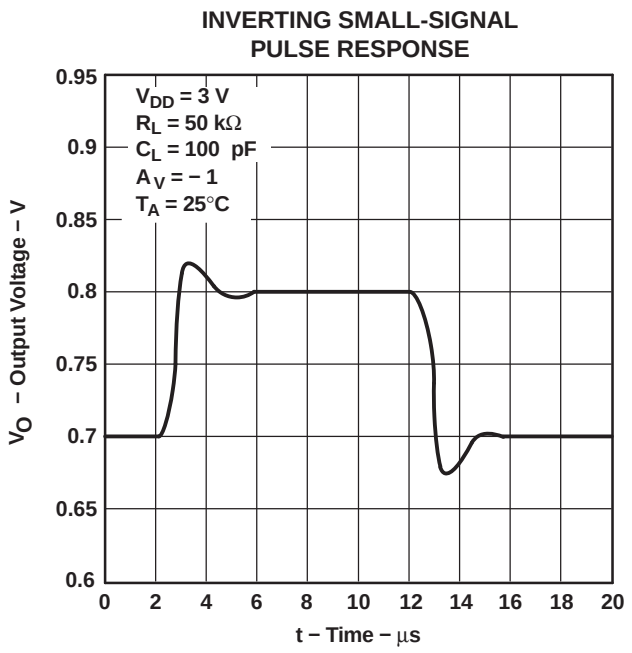


Figure 46.

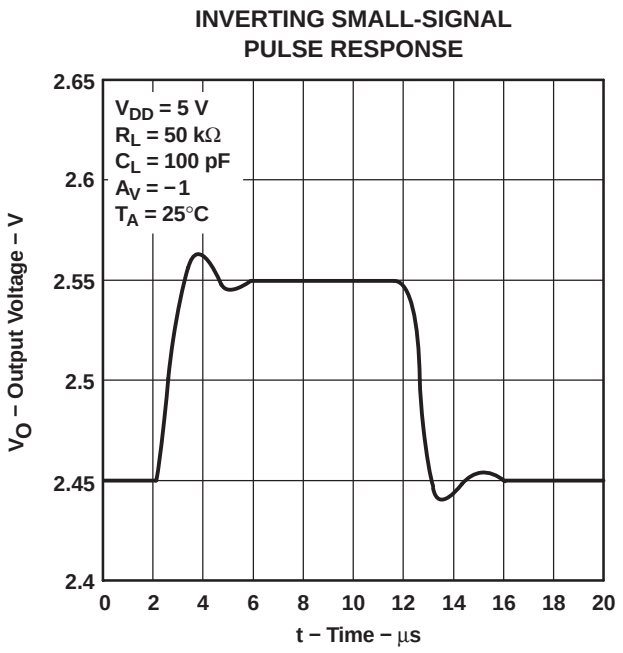


Figure 47.

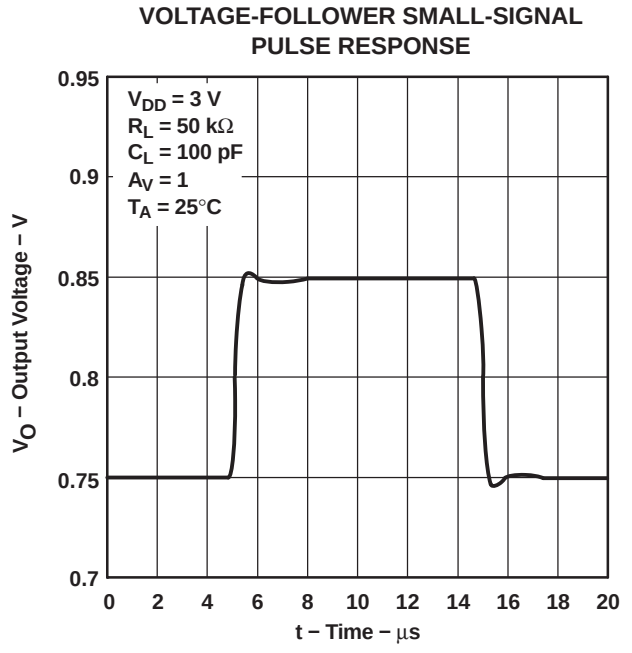


Figure 48.

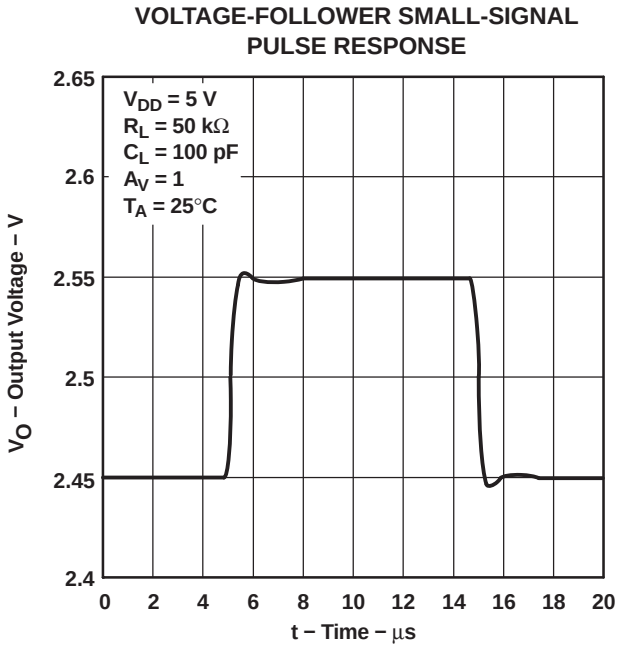


Figure 49.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

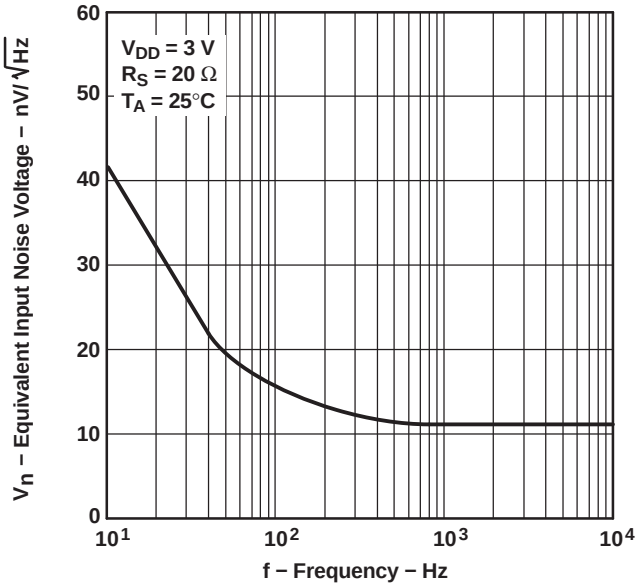


Figure 50.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

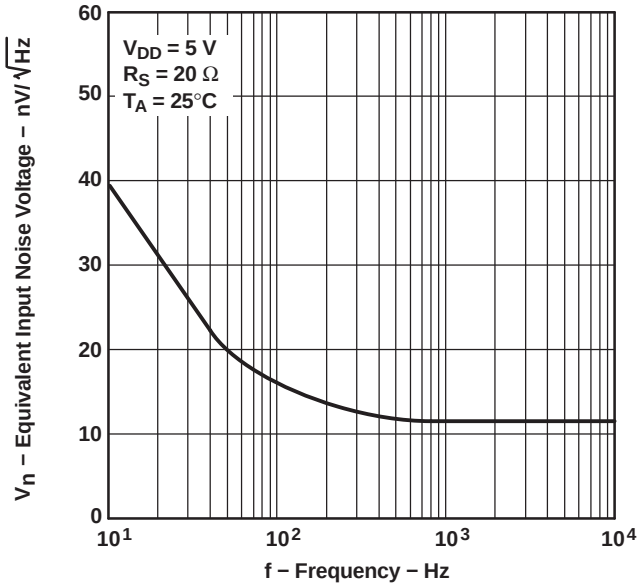


Figure 51.

INPUT NOISE VOLTAGE OVER
A 10-SECOND PERIOD

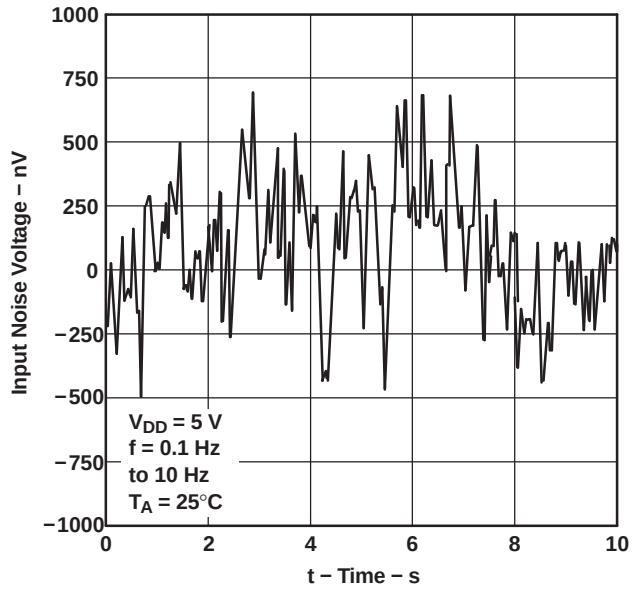


Figure 52.

INTEGRATED NOISE VOLTAGE
vs
FREQUENCY

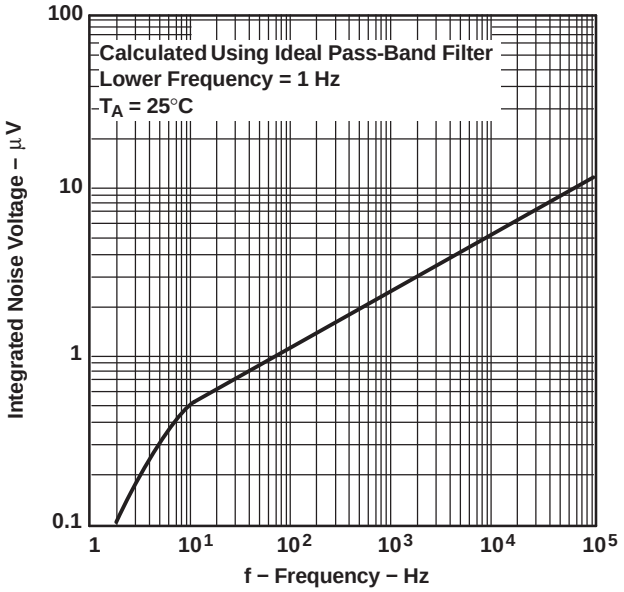


Figure 53.

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

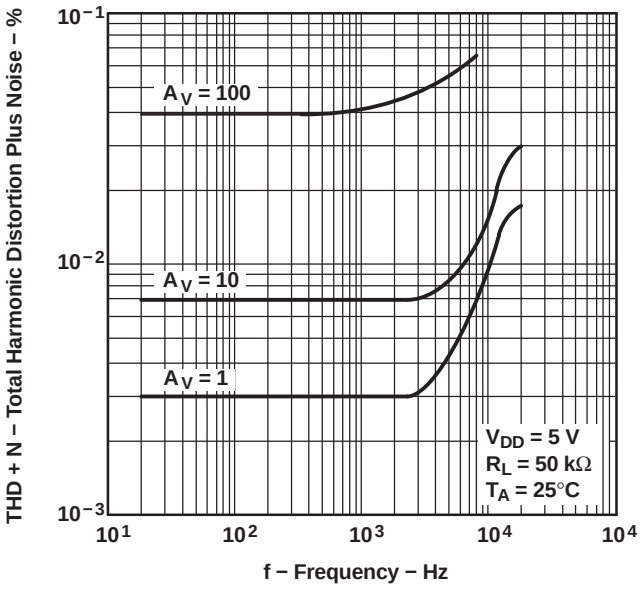


Figure 54.

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

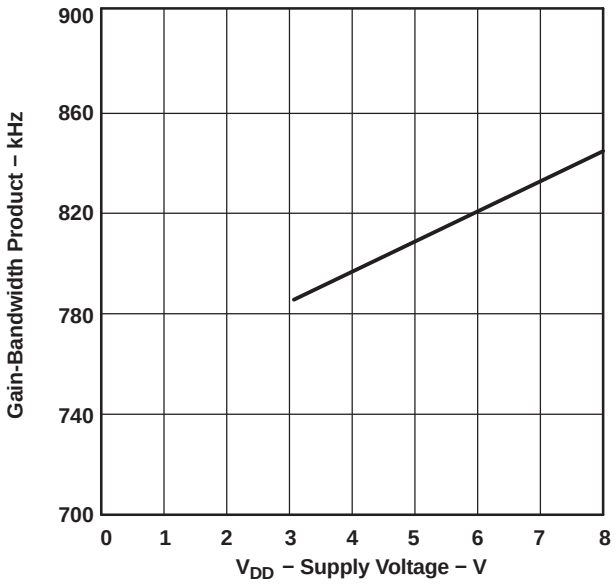


Figure 55.

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

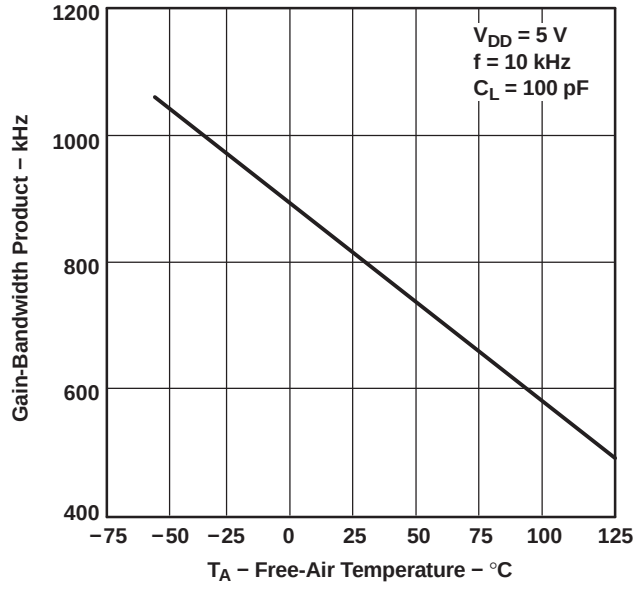


Figure 56.

PHASE MARGIN vs LOAD CAPACITANCE

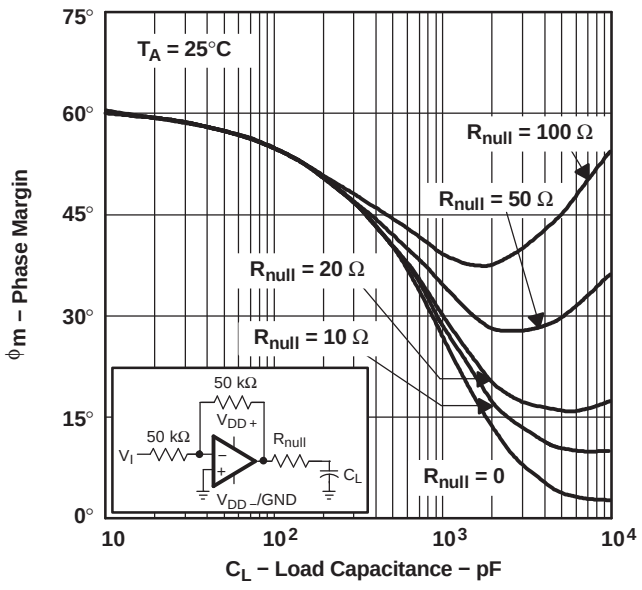


Figure 57.

GAIN MARGIN
vs
LOAD CAPACITANCE

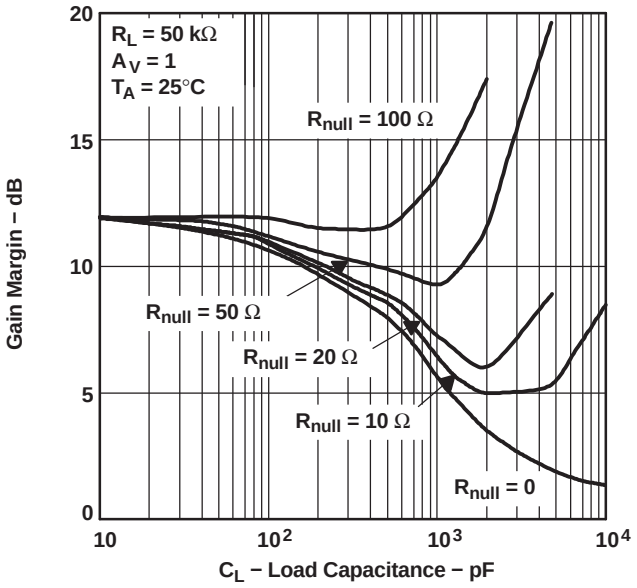


Figure 58.

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

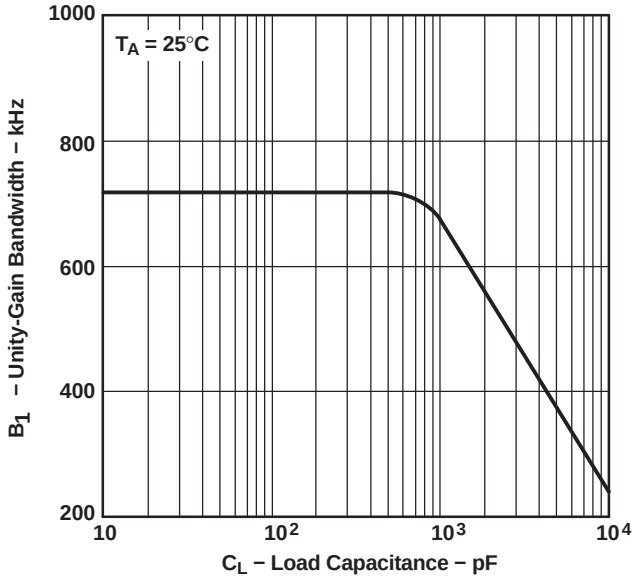
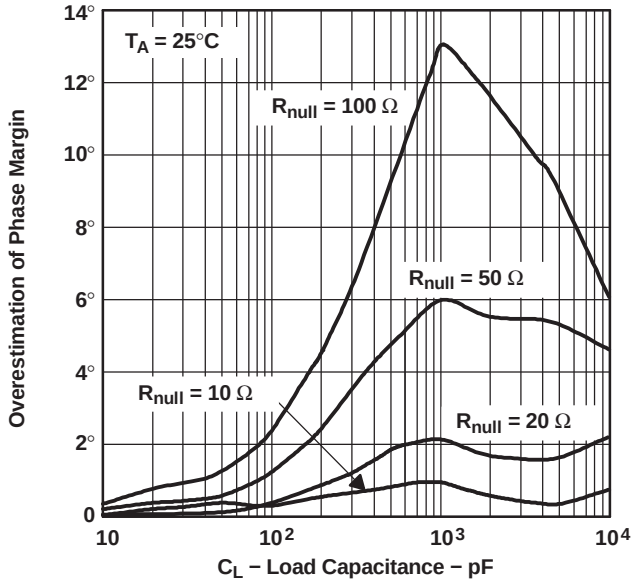


Figure 59.

OVERESTIMATION OF PHASE MARGIN
vs
LOAD CAPACITANCE



NOTE: See application information.

Figure 60.

APPLICATION INFORMATION

Driving Large Capacitive Loads

The TLV226x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 51 and Figure 52 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see Figure 61) improves the gain and phase margins when driving large capacitive loads. Figure 51 and Figure 52 show the effects of adding series resistances of 10 Ω, 20 Ω, 50 Ω, and 100 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, Equation 1 can be used.

$$\Delta\theta_{m1} = \tan^{-1}\left(2 \times \pi \times UGBW \times R_{null} \times C_L\right) \quad (1)$$

Where :

$\Delta\theta_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53). To use Equation 1, UGBW must be approximated from Figure 53.

Using Equation 1 alone overestimates the improvement in phase margin as illustrated in Figure 60. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in Equation 2.

$$F = \frac{1}{1 + g_m \times R_{null}} \quad (2)$$

Where :

F = factor reducing frequency of pole
g_m = small-signal output transconductance (typically 4.83×10^{-3} mhos)
R_{null} = output series resistance

For the TLV226x, the pole associated with the load is typically 7 MHz with 100-pF load capacitance. This value varies inversely with C_L: at C_L = 10 pF, use 70 MHz, at C_L = 1000 pF, use 700 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone (see Equation 1). Equation 3 approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the Equation 1 to better approximate the improvement in phase margin.

$$\Delta\theta_{m2} = \tan^{-1}\left[\frac{UGBW}{(F \times P_2)}\right] - \tan^{-1}\left(\frac{UGBW}{P_2}\right) \quad (3)$$

Where :

$\Delta\theta_{m2}$ = reduction in phase margin
UGBW = unity-gain bandwidth frequency
F = factor from equation (2)
P_2 = unadjusted pole (70 MHz @ 10 pF, 7 MHz @ 100 pF, etc.)

Using these equations with Figure 60 and Figure 61 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.

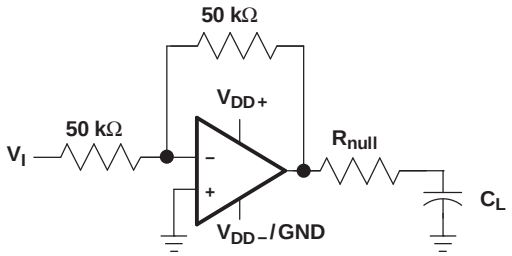


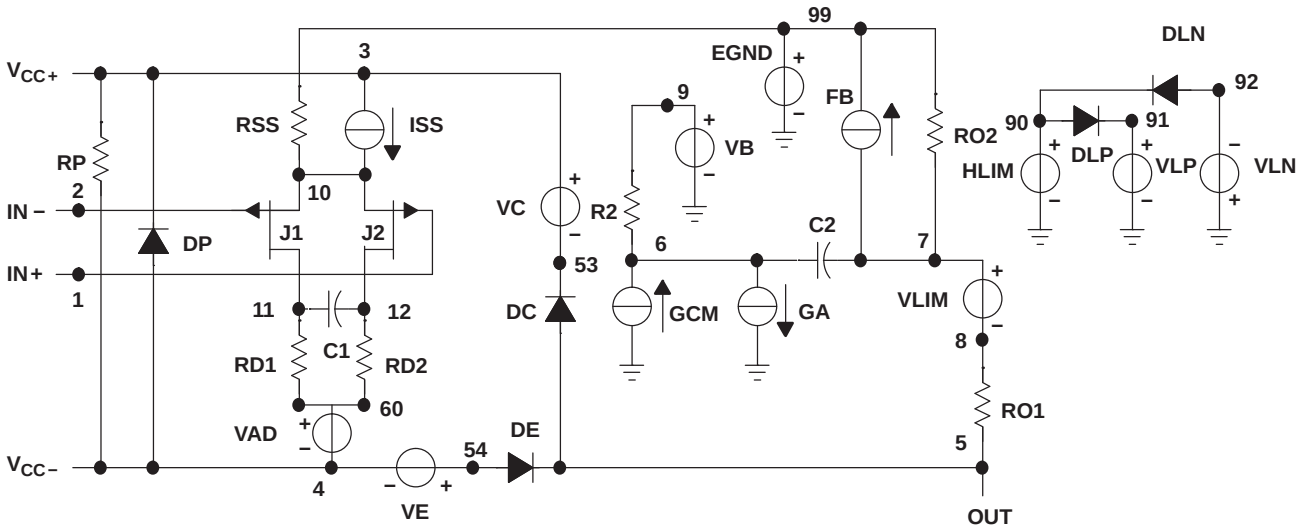
Figure 61. Series-Resistance Circuit

Macromodel Information

Macromodel information provided was derived using Microsim Parts™, the model generation software used with Microsim PSpice™. The Boyle macromodel(1) and subcircuit in Figure 62 are generated using the TLV226x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

(1) G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).




```
.SUBCKT TLV226x 1 2 3 4 5
C1        11      12      5.5E−12
C2        6       7       20.00E−12
DC        5       53      DX
DE        54      5       DX
DLP       90      91      DX
DLN       92      90      DX
DP        4       3       DX
EGND      99      0       POLY (2) (3,0) (4,0) 0 .5 .5
FB        7       99      POLY (5) VB VC VE VLP
+ VLN 0 8.84E6 −10E6 10E6 10E6 −10E6
GA        6       0       11      12 62.83E−6
GCM       0       6       10      99 12.34E−9
ISS       3       10      DC 11.05E−6
HLIM      90      0       VLIM 1K
J1        11      2       10 JX
J2        12      1       10 JX
R2        6       9       100.0E3
RD1       60      11      15.92E3
RD2       60      12      15.92E3
R01       8       5       135
R02       7       99      135
RP        3       4       15.87E3
RSS       10      99      18.18E6
VAD       60      4       −.5
VB        9       0       DC 0
VC        3       53      DC .615
VE        54      4       DC .615
VLIM      7       8       DC 0
VLP       91      0       DC 1
VLN       0       92      DC 5.1
.MODEL DX D (IS=800.0E−18)
.MODEL JX PJF (IS=500.0E−15 BETA=325E−6
+ VTO=−.08)
.ENDS
```

Figure 62. Boyle Macromodel and Subcircuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2262AQPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TQ262A	Samples
TLV2264AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P2264AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV2262A-Q1, TLV2264A-Q1 :

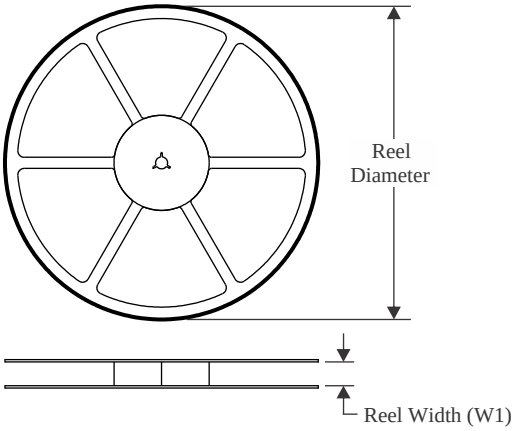
- Catalog: TLV2262A, TLV2264A
- Military: TLV2262AM, TLV2264AM

NOTE: Qualified Version Definitions:

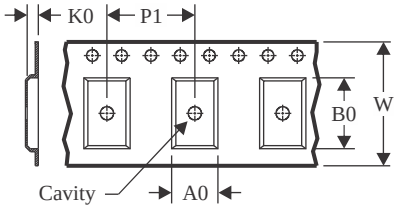
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

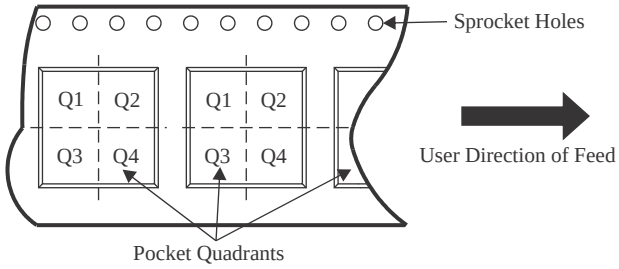


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

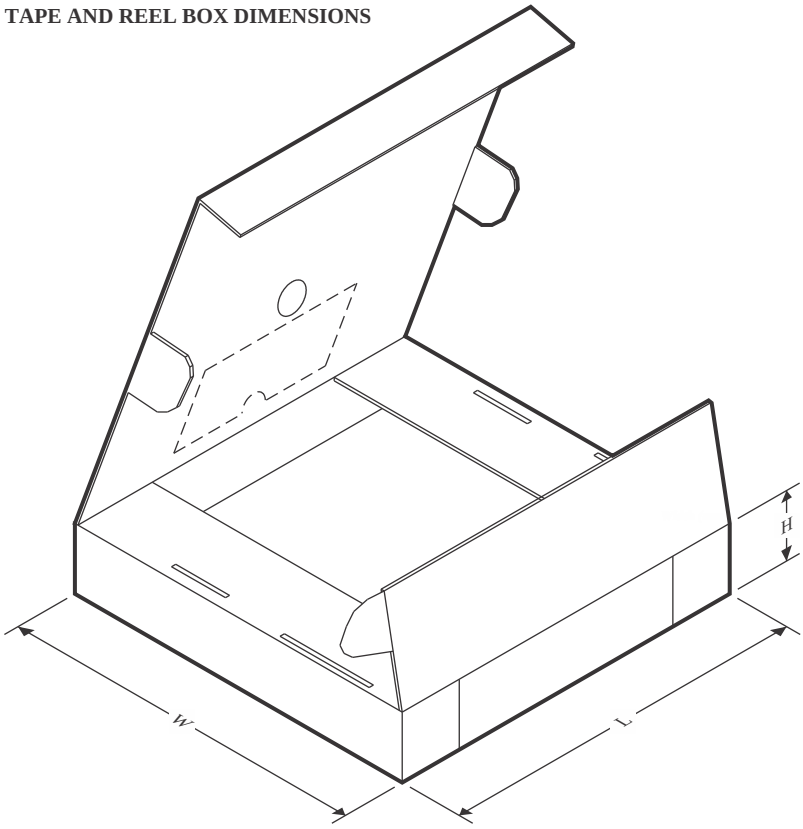
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2262AQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2264AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

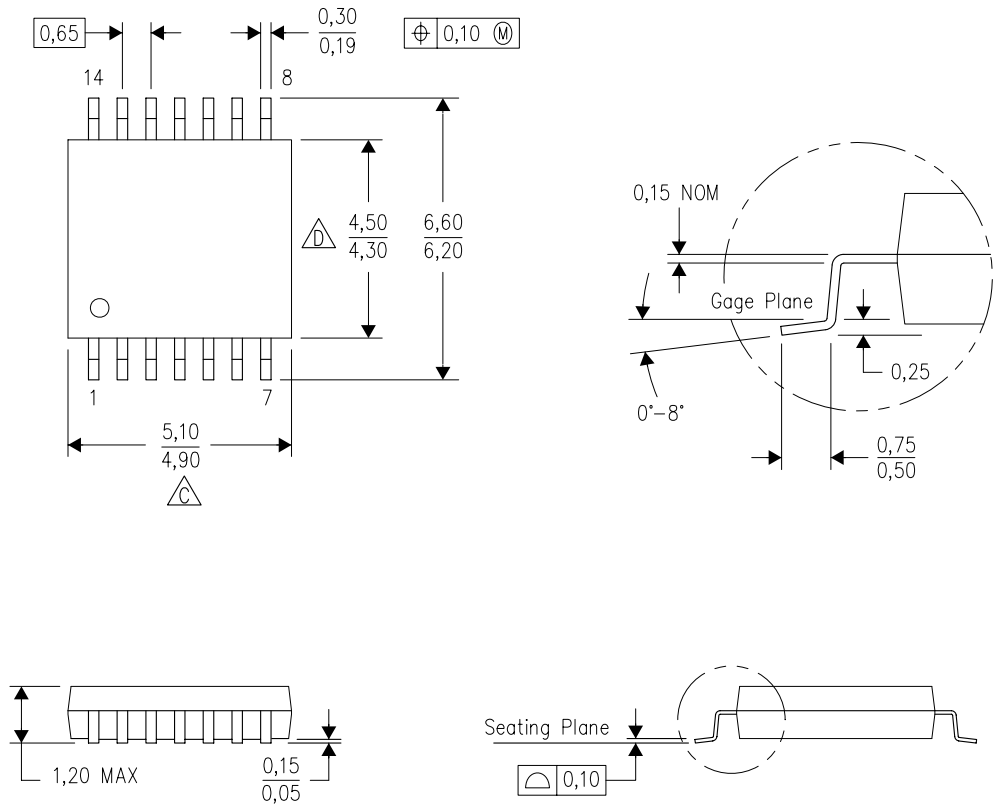
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2262AQPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
TLV2264AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

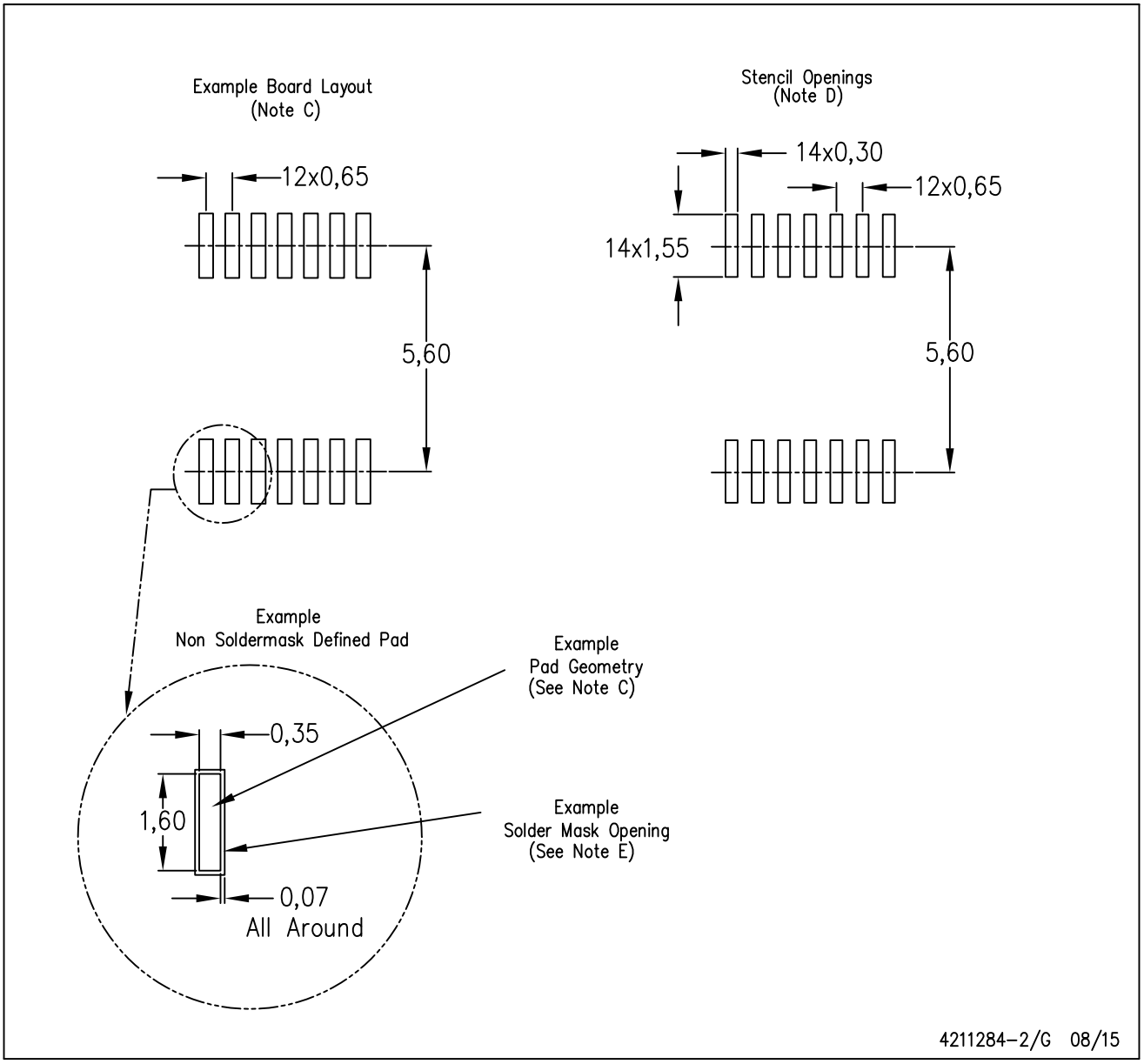
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



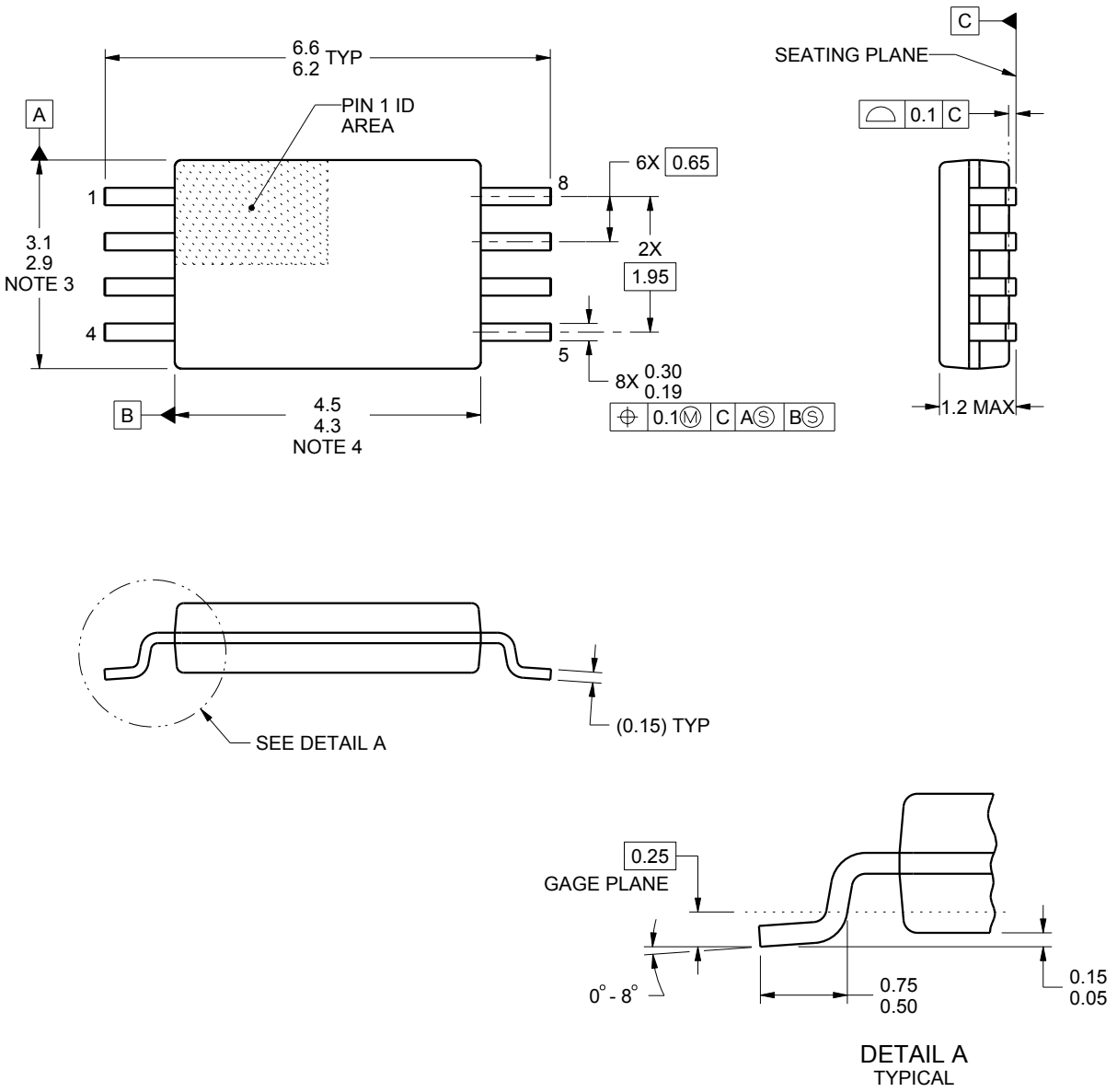
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0008A

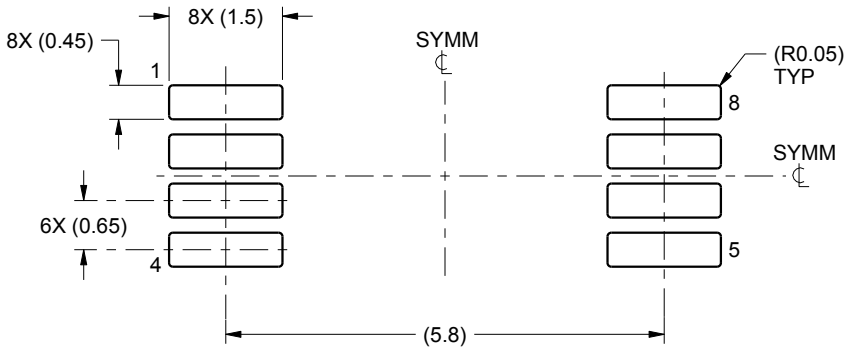
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

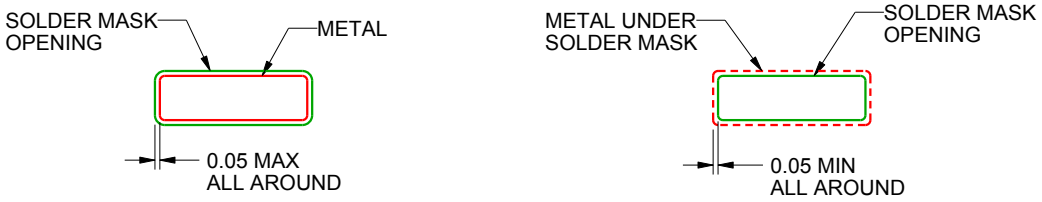


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

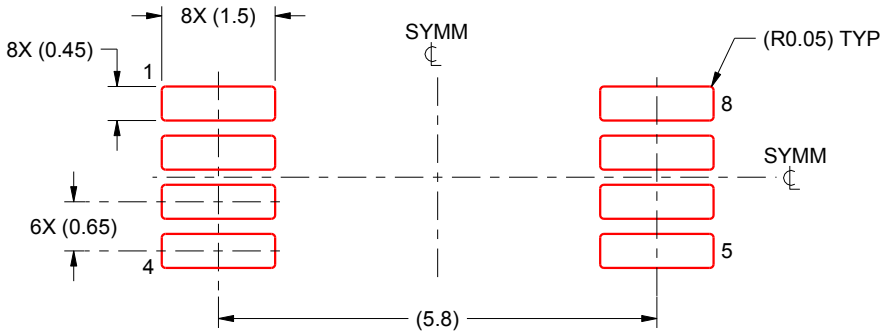


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265