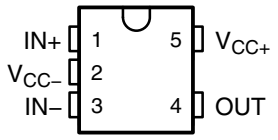
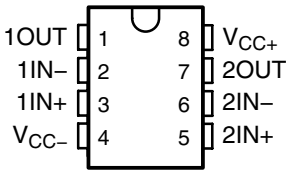
SLOS195H – FEBRUARY 1997 – REVISED JUNE 2007

- **Low Supply-Voltage Operation . . . V_{CC} = ±1 V Min**
- **Wide Bandwidth . . . 7 MHz Typ at V_{CC}± = ±2.5 V**
- **High Slew Rate . . . 3 V/μs Typ at V_{CC}± = ±2.5 V**
- **Wide Output Voltage Swing . . . ±2.4 V Typ at V_{CC}± = ±2.5 V, R_L = 10 kΩ**
- **Low Noise . . . 8 nV/√Hz Typ at f = 1 kHz**

TLV2361 . . . DBV PACKAGE
(TOP VIEW)



TLV2362 . . . D, DGK, P, PS, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The TLV236x devices are high-performance dual operational amplifiers built using an original Texas Instruments bipolar process. These devices can be operated at a very low supply voltage (±1 V), while maintaining a wide output swing. The TLV236x devices offer a dramatically improved dynamic range of signal conditioning in low-voltage systems. The TLV236x devices also provide higher performance than other general-purpose operational amplifiers by combining higher unity-gain bandwidth and faster slew rate. With their low distortion and low-noise performance, these devices are well suited for audio applications.

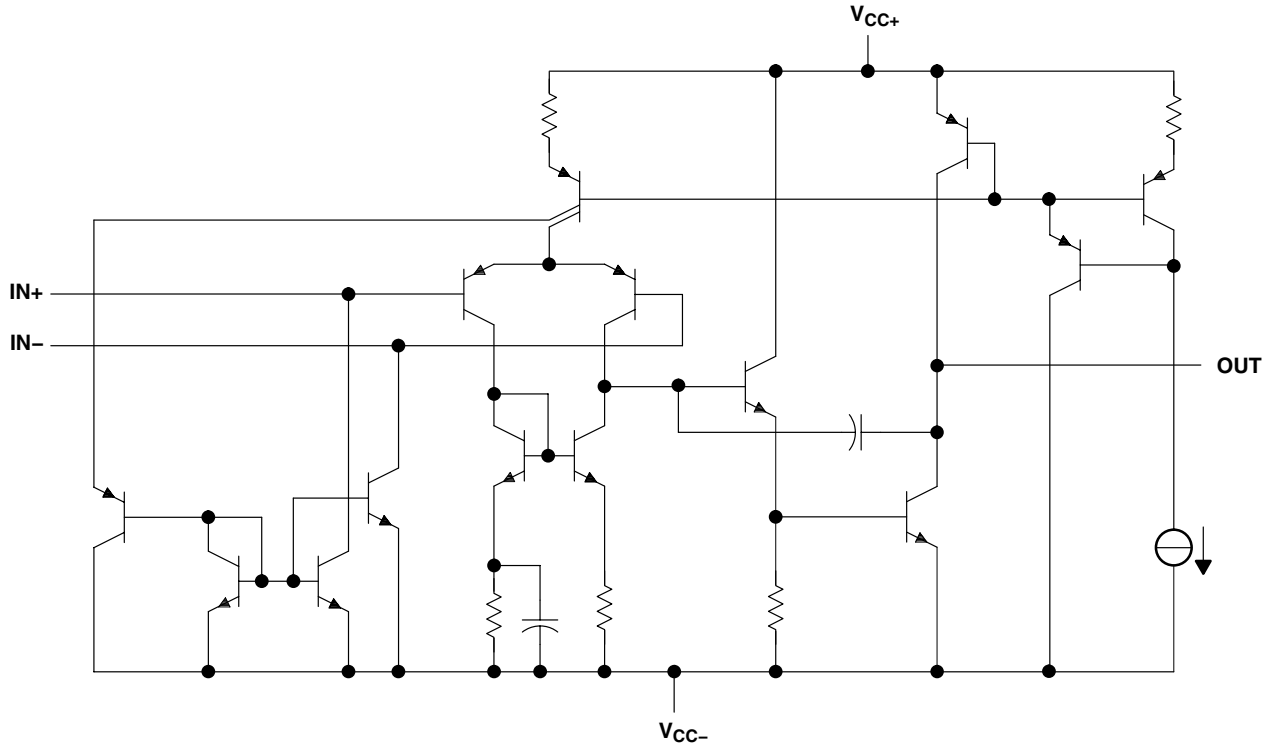
ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–0°C to 70°C	SOT-23-5 (DBV)	Reel of 3000	TLV2361CDBVR	YC3_
		Reel of 250	TLV2361CDBVT	
–40°C to 85°C	SOT-23-5 (DBV)	Reel of 3000	TLV2361IDBVR	YC4_
		Reel of 250	TLV2361IDBVT	
	MSOP/VSSOP (DGK)	Reel of 2500	TLV2362IDGKR	YBS
	PDIP (P)	Tube of 50	TLV2362IP	TLV2362IP
	SOIC (D)	Tube of 75	TLV2362ID	2362I
		Reel of 2500	TLV2362IDR	
	SOP (PS)	Reel of 2000	TLV2362IPSR	TY2362
	TSSOP (PW)	Tube of 150	TLV2362IPW	TY2362
		Reel of 2000	TLV2362IPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT		
COMPONENT	TLV2361	TLV2362
Transistors	30	46
Resistors	6	11
Diodes	1	1
Capacitors	2	4
JFET	1	1

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) . . . . . 3.5 V
Supply voltage, V_{CC-} (see Note 1) . . . . . –3.5 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±3.5 V
Input voltage, V_I (any input) (see Notes 1 and 3) . . . . . $V_{CC}±$
Output voltage, V_O . . . . . ±3.5 V
Output current, I_O . . . . . 20 mA
Duration of short-circuit current at (or below) 25°C (output shorted to GND) . . . . . Unlimited
Package thermal impedance, θ_{JA} (see Notes 4 and 5): D package . . . . . 97°C/W
DBV package . . . . . 206°C/W
DGK package . . . . . 172°C/W
P package . . . . . 85°C/W
PS package . . . . . 95°C/W
PW package . . . . . 149°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. All input voltage values must not exceed V_{CC}.
4. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		±1	±2.5	V
T_A	Operating free-air temperature	TLV2361C	0	70	°C
		TLV2361I, TLV2362I	–40	85	

TLV2361 and TLV2362 electrical characteristics, $V_{CC}\pm$ = ±1.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0,	V_{IC} = 0		25°C		1	6	mV
					Full range			7.5	
I_{IO}	Input offset current	V_O = 0,	V_{IC} = 0		25°C		5	100	nA
					Full range			150	
I_{IB}	Input bias current	V_O = 0,	V_{IC} = 0		25°C		20	150	nA
					Full range			250	
V_{IC}	Common-mode input voltage	$\|V_{IO}\| \le$ 7.5 mV			25°C	±0.5			V
					Full range	±0.5			
V_{OM+}	Maximum positive-peak output voltage	R_L = 10 kΩ			25°C	1.2	1.4		V
		$R_L \ge$ 10 kΩ			Full range	1.2			
V_{OM-}	Maximum negative-peak output voltage	R_L = 10 kΩ			25°C	–1.2	–1.4		V
		$R_L \ge$ 10 kΩ			Full range	–1.2			
I_{CC}	Supply current (per amplifier)	V_O = 0,	No load		25°C		1.4	2.25	mA
					Full range			2.75	mA
A_{VD}	Large-signal differential voltage amplification	V_O = ±1 V,	R_L = 10 kΩ	TLV2361	25°C	60	80		dB
				TLV2362			55		
CMRR	Common-mode rejection ratio	V_{IC} = ±0.5 V			25°C		75		dB
k_{SVR}	Supply-voltage rejection ratio	$V_{CC}\pm$ = ±1.5 V to ±2.5 V			25°C		80		dB

TLV2361 and TLV2362 operating characteristics, $V_{CC}\pm$ = ±1.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			TYP	UNIT
SR	Slew rate	A_V = 1,	V_I = ±0.5 V		2.5	V/μs
B_1	Unity-gain bandwidth	A_V = 40,	R_L = 10 kΩ,	C_L = 100 pF	6	MHz
V_n	Equivalent input noise voltage	R_S = 100 Ω,	R_F = 10 kΩ,	f = 1 kHz	9	nV/√Hz

TLV2361 and TLV2362 electrical characteristics, $V_{CC}\pm$ = ±2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0,	V_{IC} = 0		25°C		1	6	mV
					Full range			7.5	
I_{IO}	Input offset current	V_O = 0,	V_{IC} = 0		25°C		5	100	nA
					Full range			150	
I_{IB}	Input bias current	V_O = 0,	V_{IC} = 0		25°C		20	150	nA
					Full range			250	
V_{IC}	Common-mode input voltage	$\|V_{IO}\| \le$ 7.5 mV			25°C	±1.5			V
					Full range	±1.4			
V_{OM+}	Maximum positive-peak output voltage	R_L = 10 kΩ			25°C	2	2.4		V
		$R_L \ge$ 10 kΩ			Full range	2			
V_{OM-}	Maximum negative-peak output voltage	R_L = 10 kΩ			25°C	–2	–2.4		V
		$R_L \ge$ 10 kΩ			Full range	–2			
I_{CC}	Supply current (per amplifier)	V_O = 0,	No load		25°C		1.75	2.5	mA
					Full range			3	
A_{VD}	Large-signal differential voltage amplification	V_O = ±1 V,	R_L = 10 kΩ	TLV2361	25°C	60	80		dB
				TLV2362			60		
CMRR	Common-mode rejection ratio	V_{IC} = ±0.5 V			25°C		85		dB
k_{SVR}	Supply-voltage rejection ratio	$V_{CC}\pm$ = ±1.5 V to ±2.5 V			25°C		80		dB

TLV2361 and TLV2362 operating characteristics, $V_{CC}\pm$ = ±2.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			TYP	UNIT
SR	Slew rate	A_V = 1,	V_I = ±0.5 V		3	V/μs
B_1	Unity-gain bandwidth	A_V = 40,	R_L = 10 kΩ,	C_L = 100 pF	7	MHz
V_n	Equivalent input noise voltage	R_S = 100 Ω,	R_F = 10 kΩ,	f = 1 kHz	8	nV/√Hz
THD + N	Total harmonic distortion, plus noise	A_V = 1,	V_O = ±1.2 V,	R_L = 10 kΩ, f = 3 kHz	0.004	%

TYPICAL CHARACTERISTICS

Table of Graphs

GRAPH TITLE	FIGURE
Supply current vs Free-air temperature	1
Supply current vs Supply voltage	2
Maximum positive output voltage vs Output current	3
Maximum negative output voltage vs Output current	4
Maximum peak-to-peak output voltage vs Frequency	5
Equivalent input noise voltage vs Frequency	6
Total harmonic distortion vs Frequency	7
Total harmonic distortion vs Output voltage	8

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

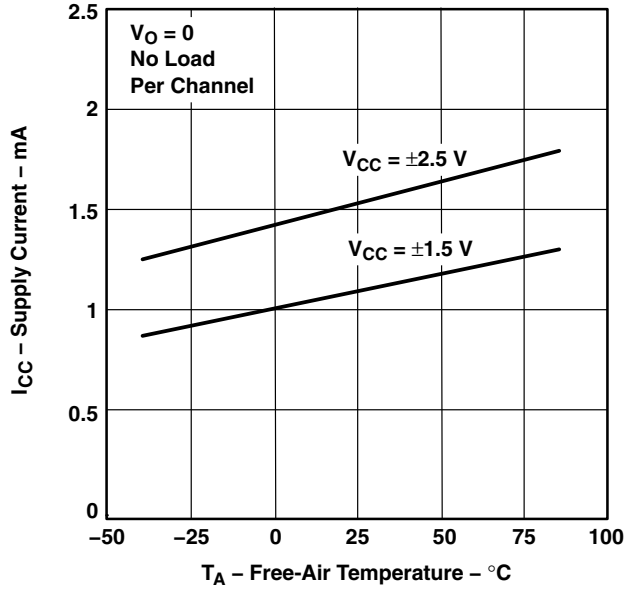


Figure 1

SUPPLY CURRENT vs SUPPLY VOLTAGE

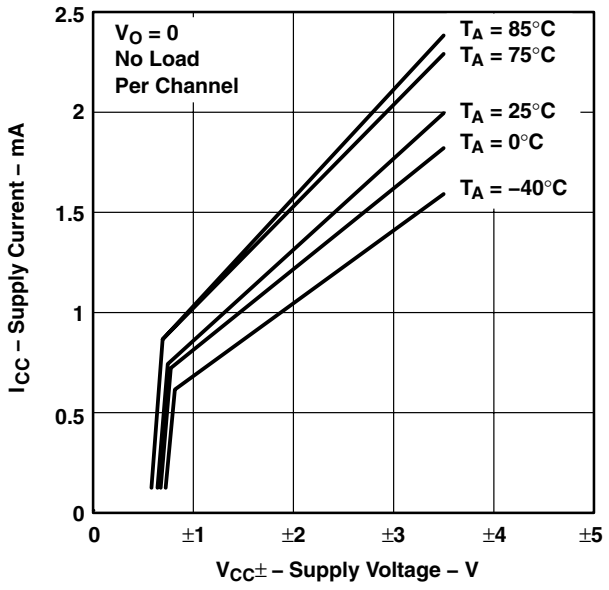


Figure 2

MAXIMUM POSITIVE OUTPUT VOLTAGE vs OUTPUT CURRENT

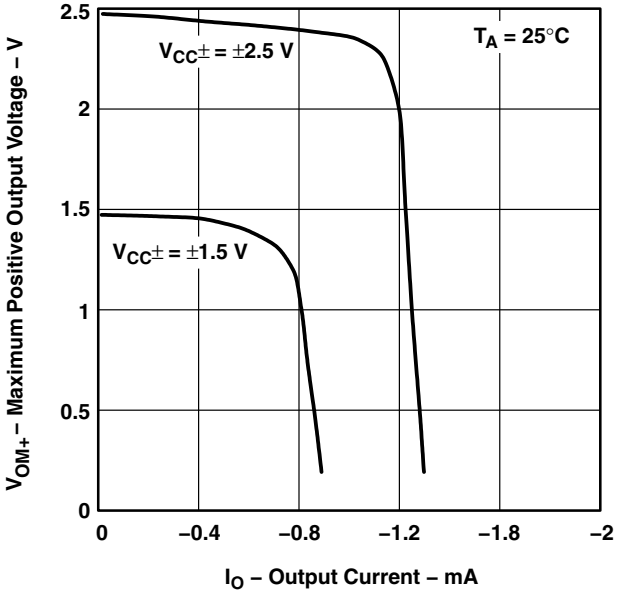


Figure 3

MAXIMUM NEGATIVE OUTPUT VOLTAGE vs OUTPUT CURRENT

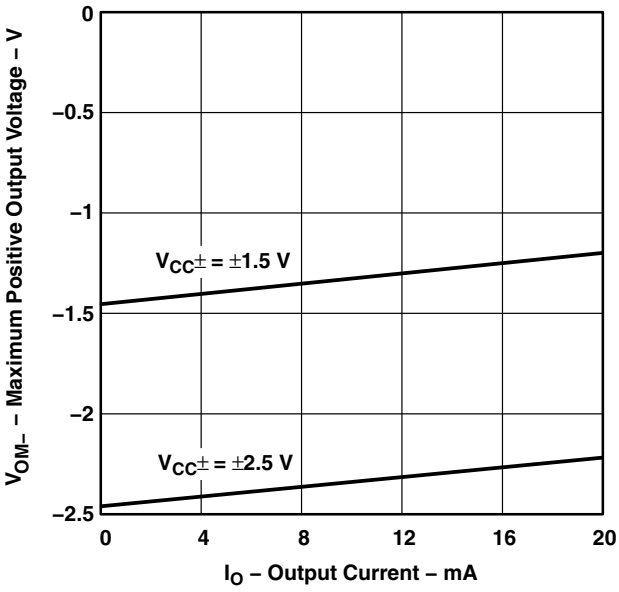


Figure 4

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

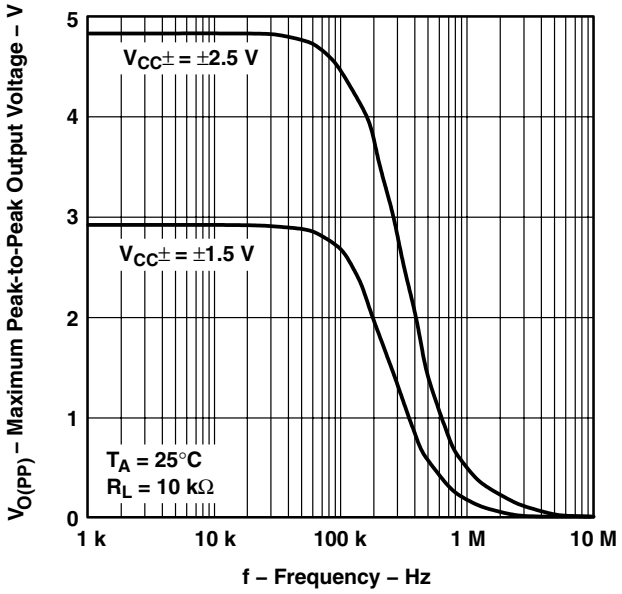


Figure 5

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

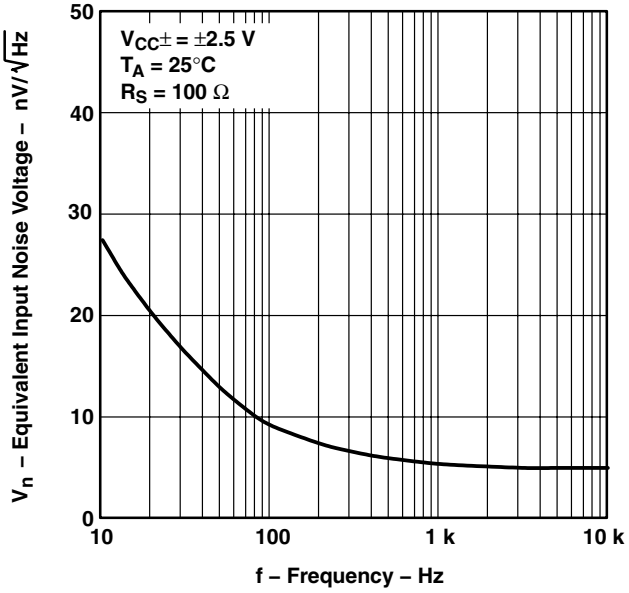


Figure 6

TOTAL HARMONIC DISTORTION vs FREQUENCY

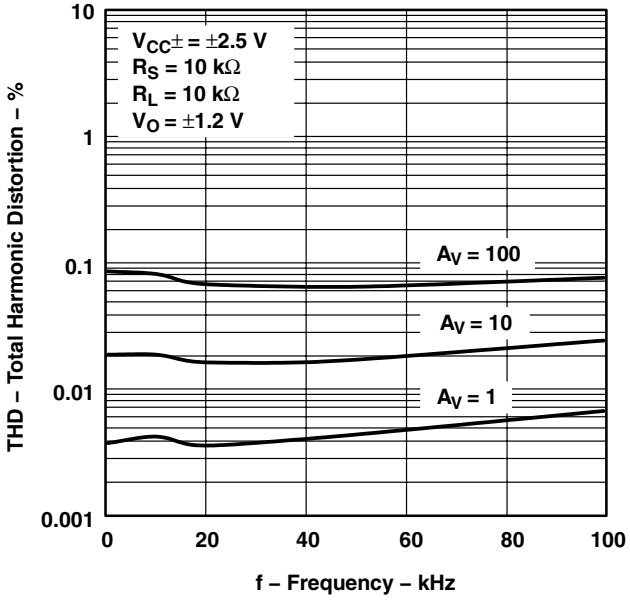


Figure 7

TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGE

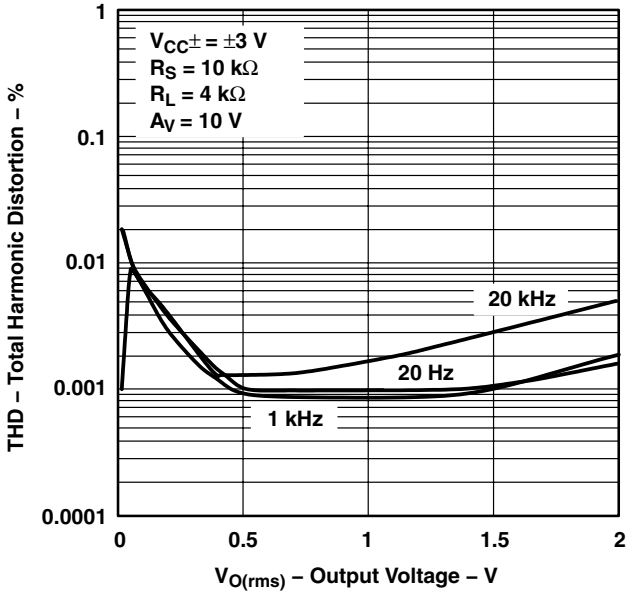


Figure 8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2361CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	(YC3B ~ YC3G ~ YC3L)	Samples
TLV2361CDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	(YC3B ~ YC3G ~ YC3L)	Samples
TLV2361IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	(YC4B ~ YC4G ~ YC4L)	Samples
TLV2361IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	(YC4B ~ YC4G ~ YC4L)	Samples
TLV2362ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2362I	Samples
TLV2362IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(YBL ~ YBS ~ YBU)	Samples
TLV2362IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(YBL ~ YBS ~ YBU)	Samples
TLV2362IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2362I	Samples
TLV2362IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2362I	Samples
TLV2362IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLV2362IP	Samples
TLV2362IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2362	Samples
TLV2362IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2362	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

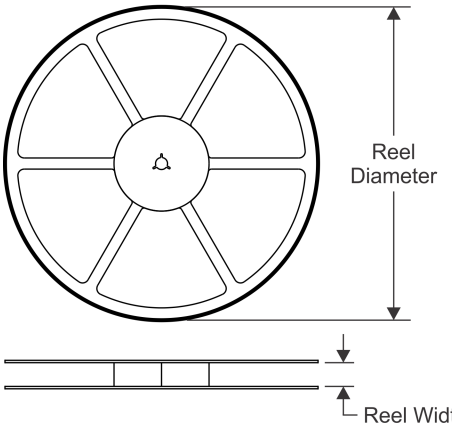
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

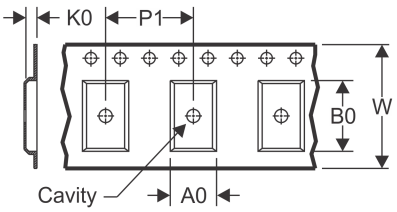
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

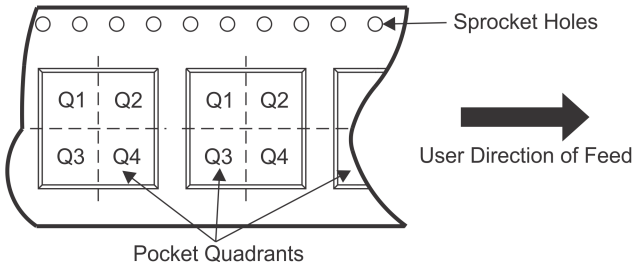


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

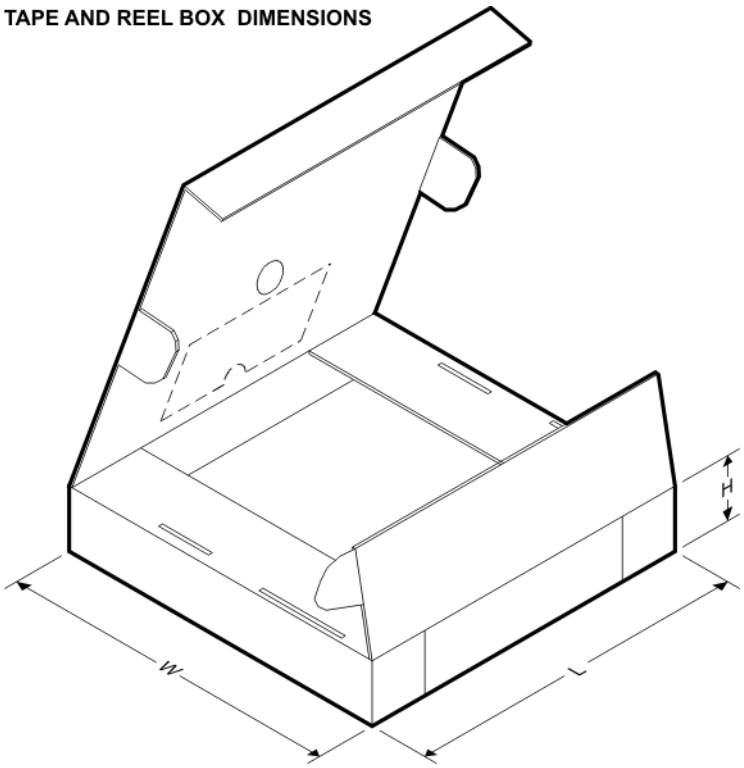
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2361CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV2361CDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV2361IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV2361IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV2362IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TLV2362IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2362IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

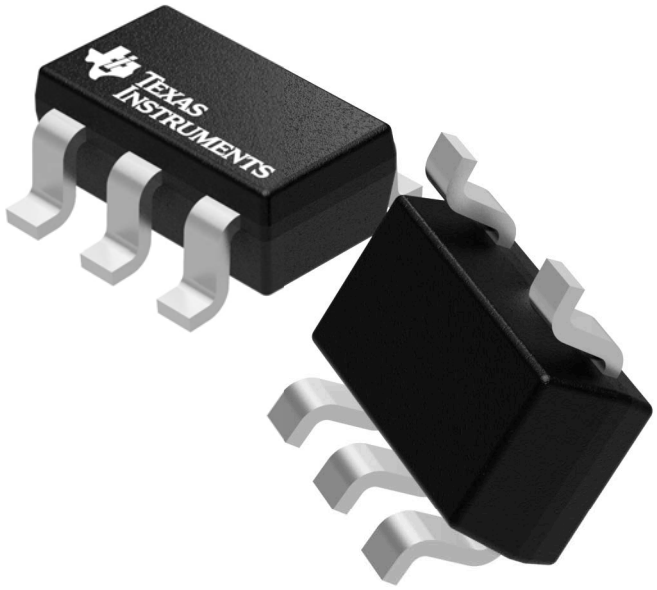


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2361CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV2361CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV2361IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV2361IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV2362IDGKR	VSSOP	DGK	8	2500	370.0	355.0	55.0
TLV2362IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2362IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



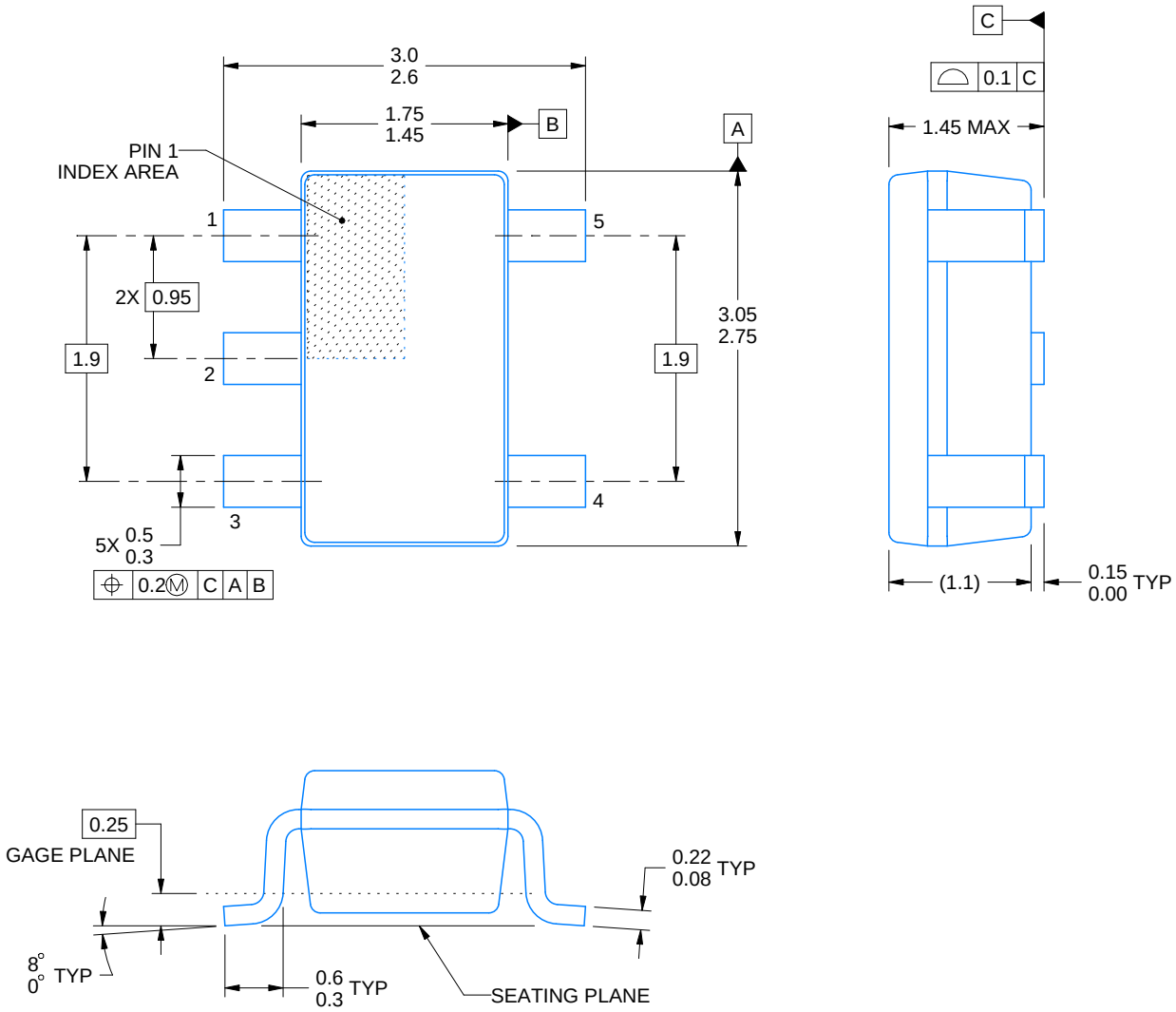
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

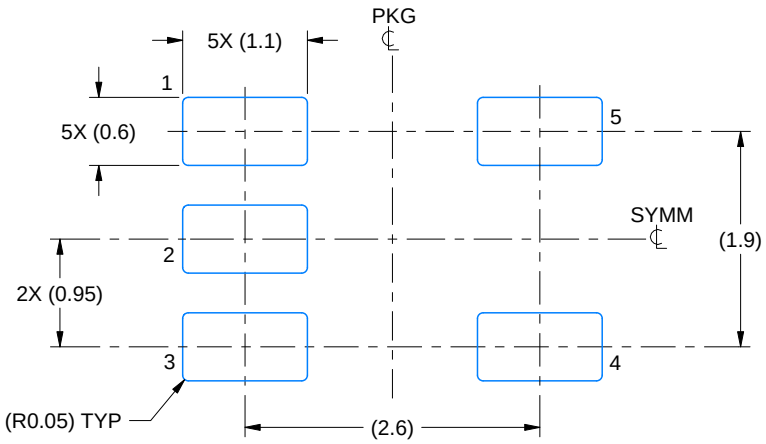
SMALL OUTLINE TRANSISTOR



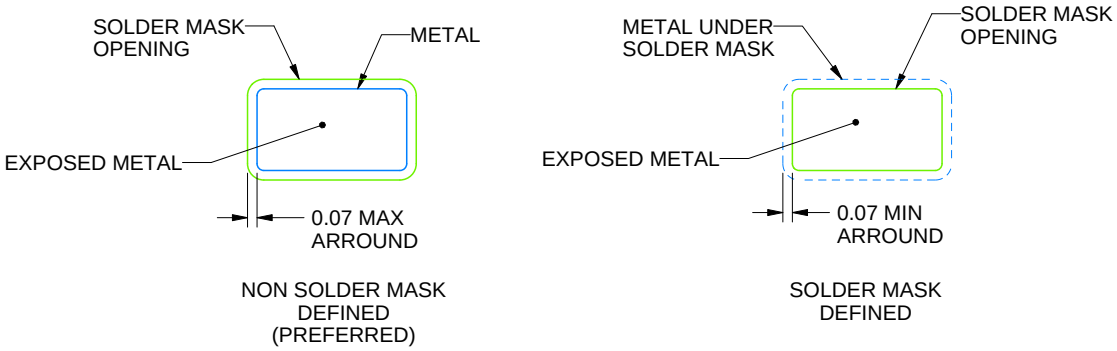
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

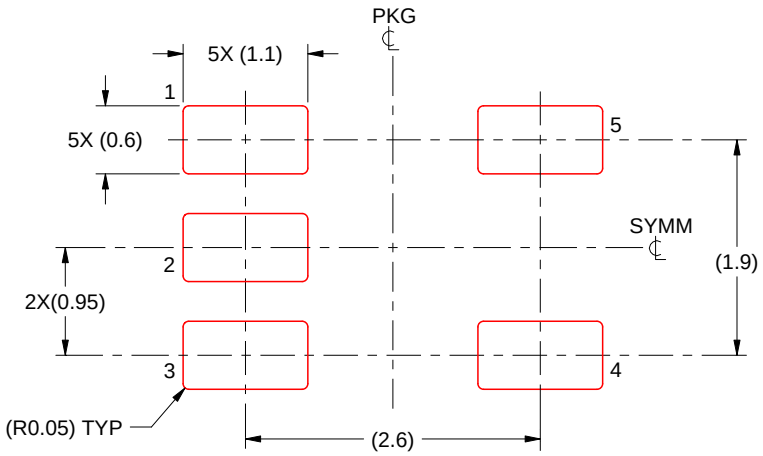


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



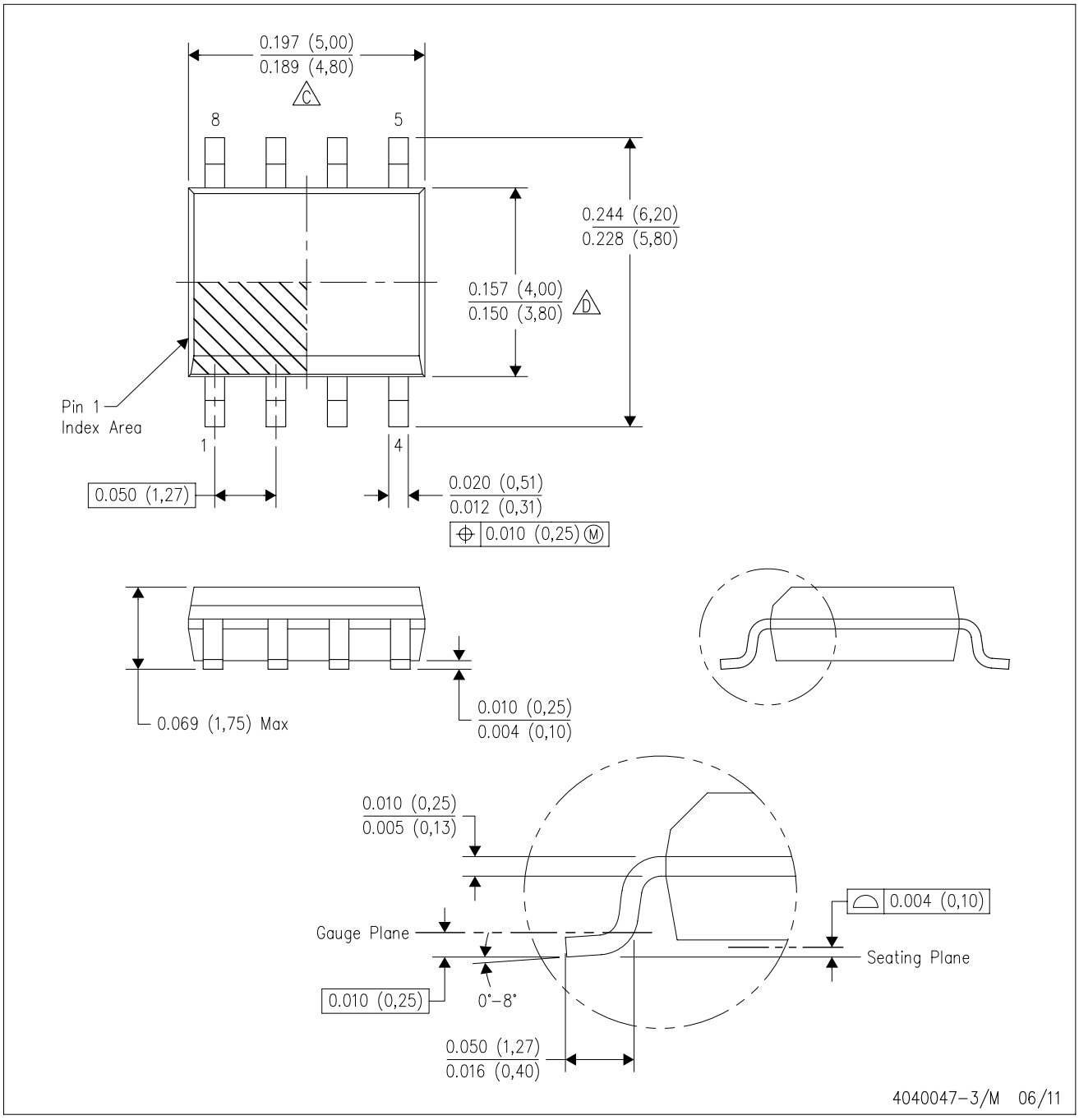
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

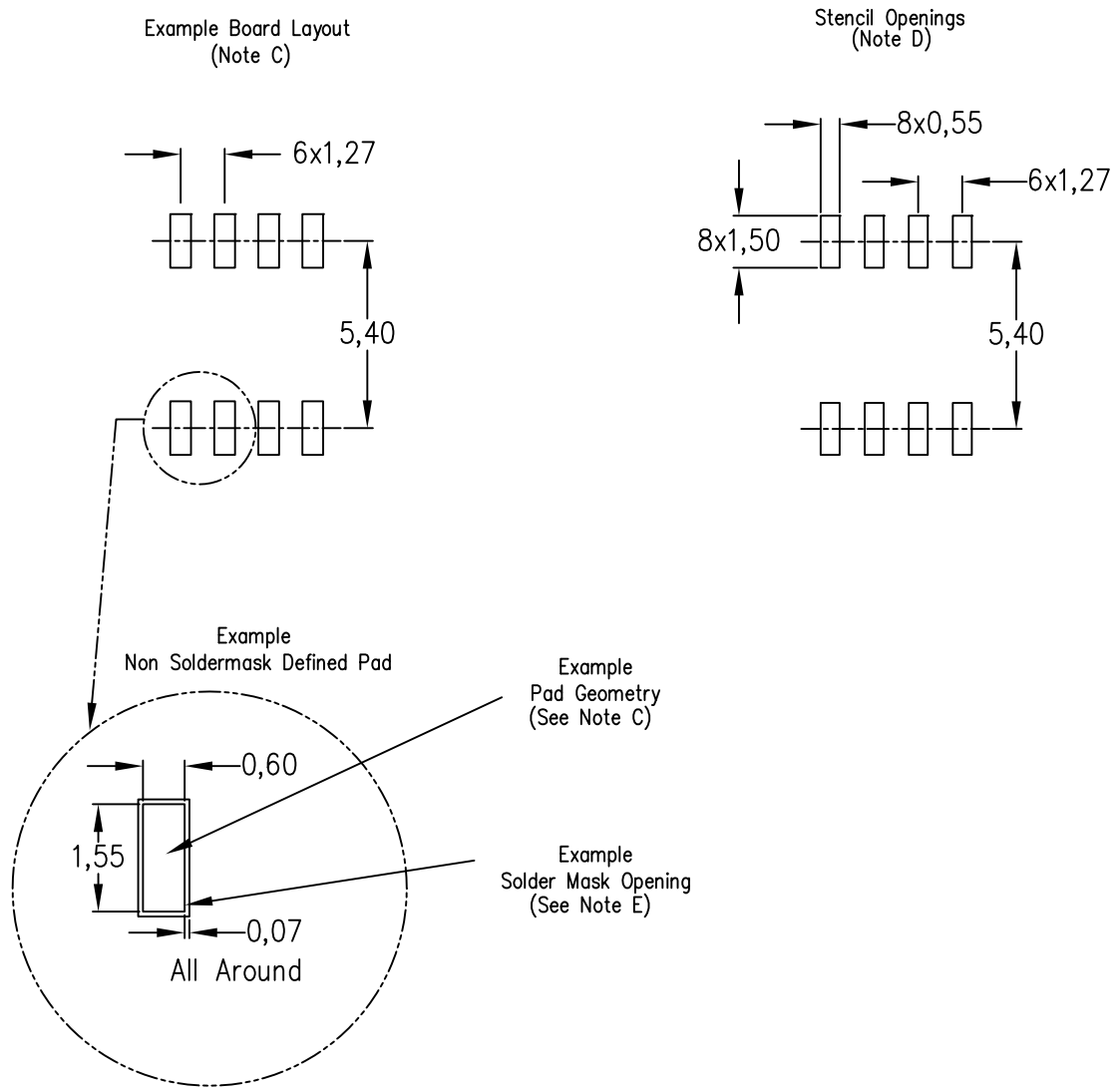
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



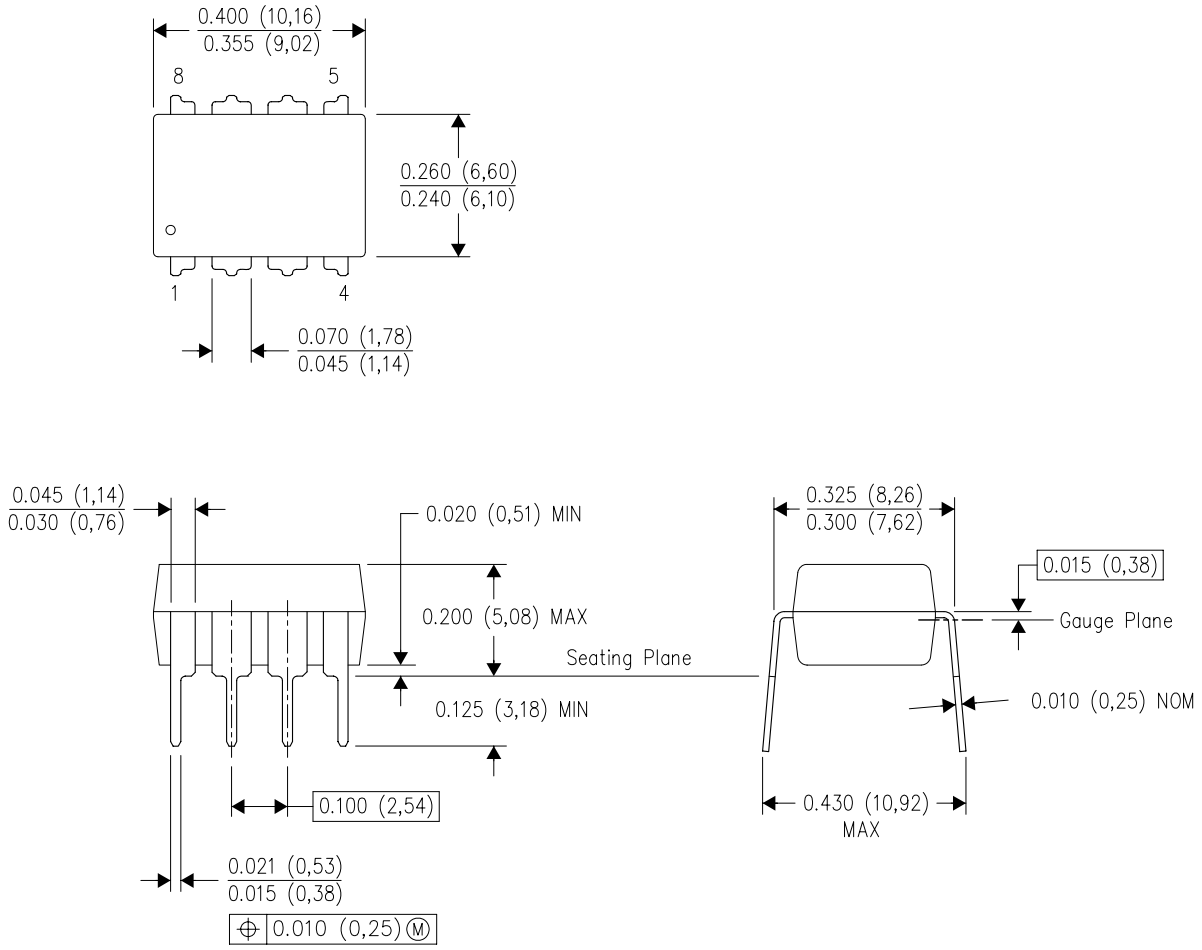
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



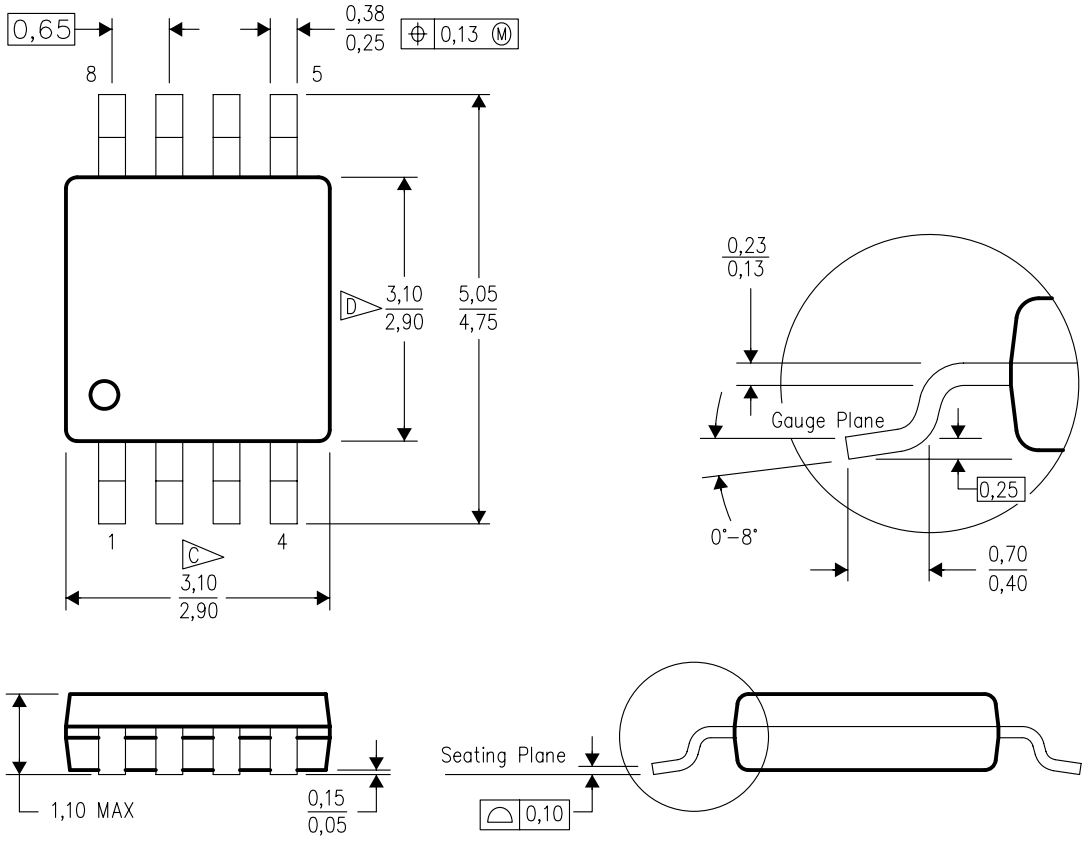
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

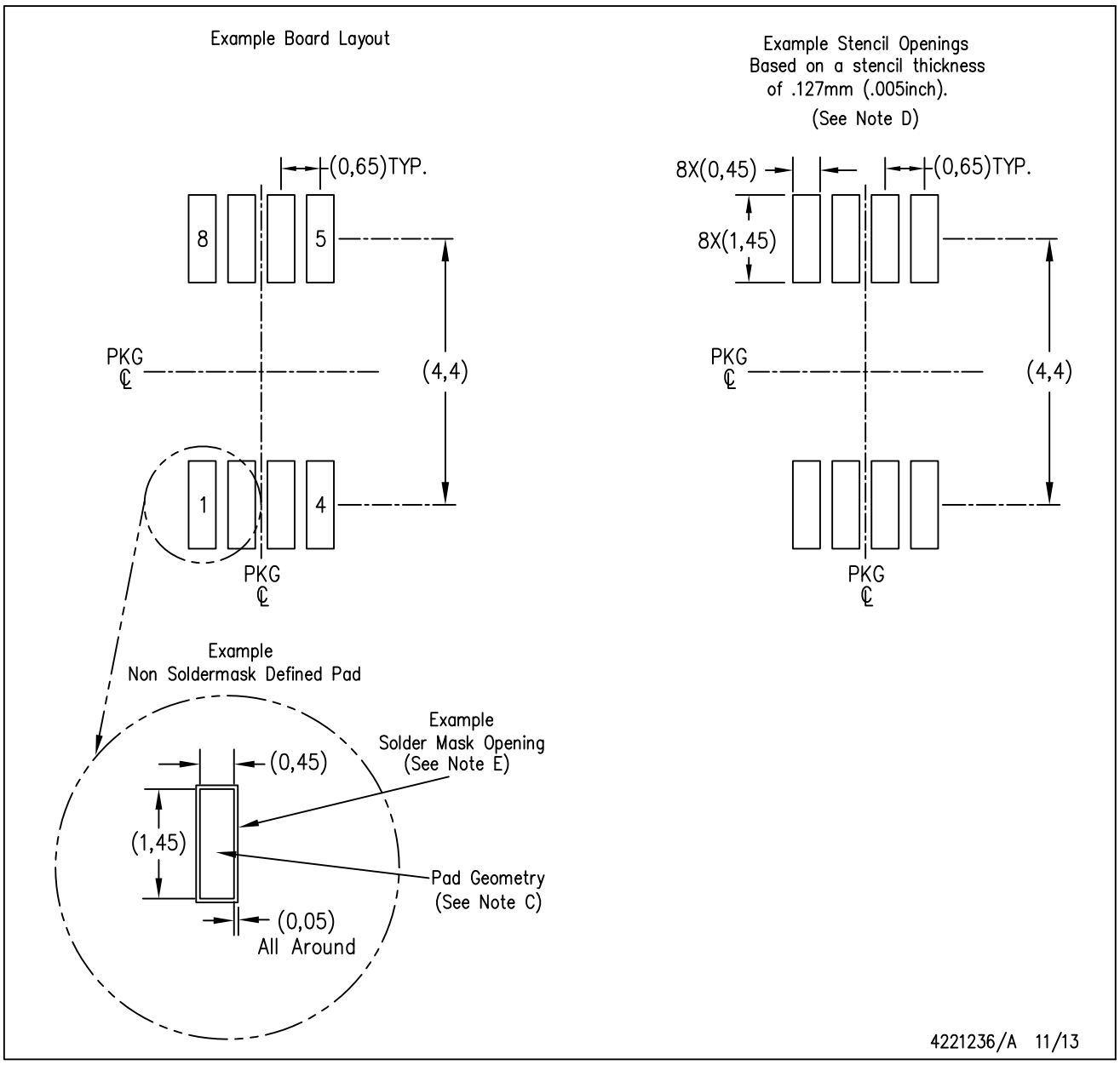
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



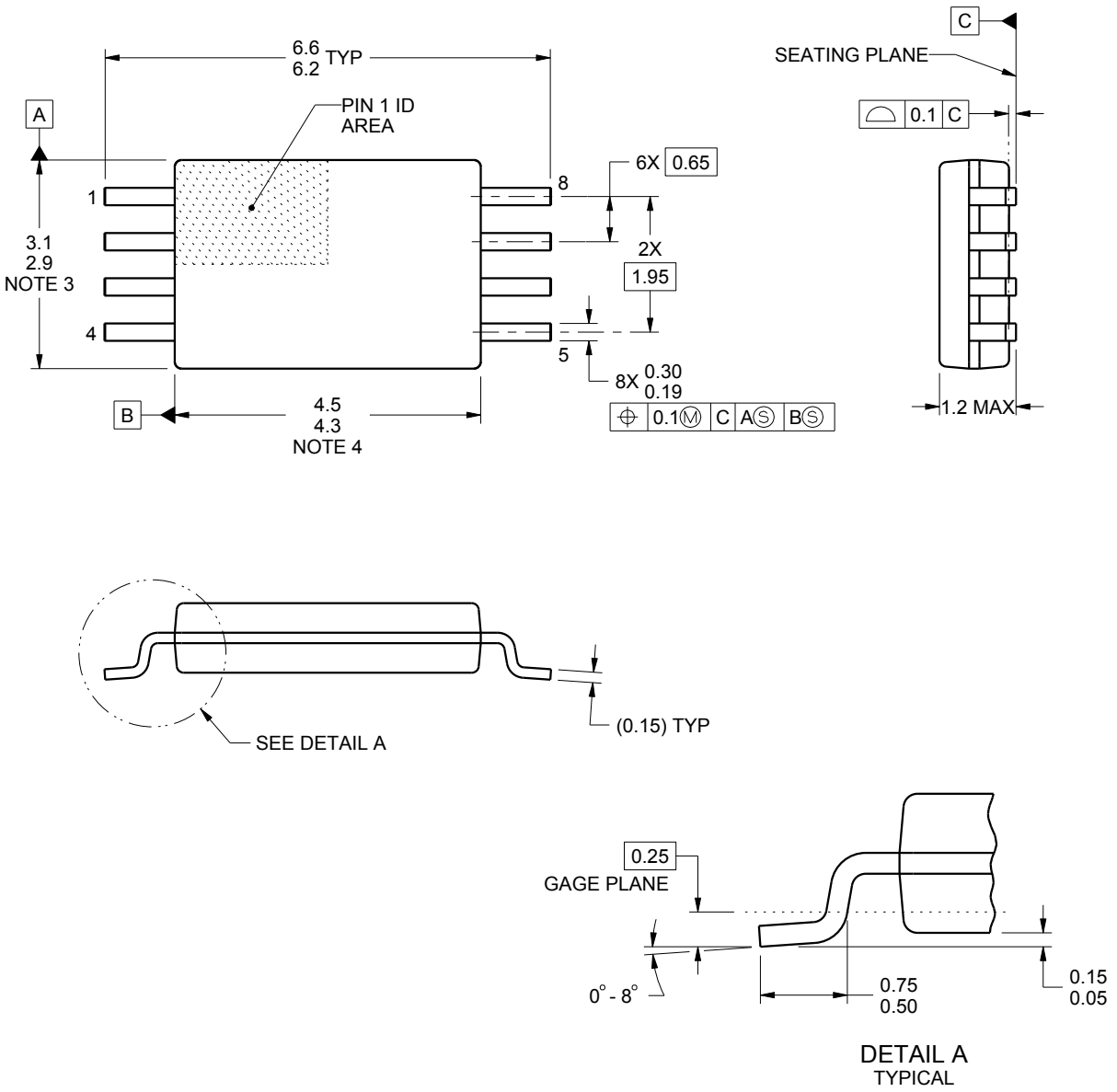
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0008A

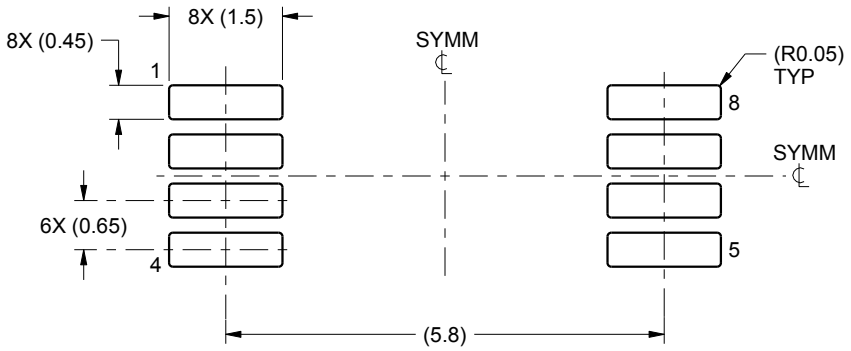
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

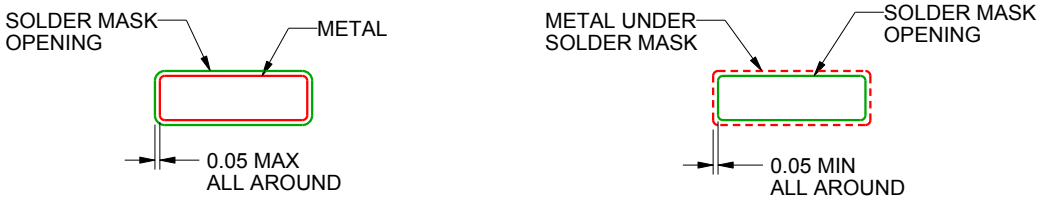


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

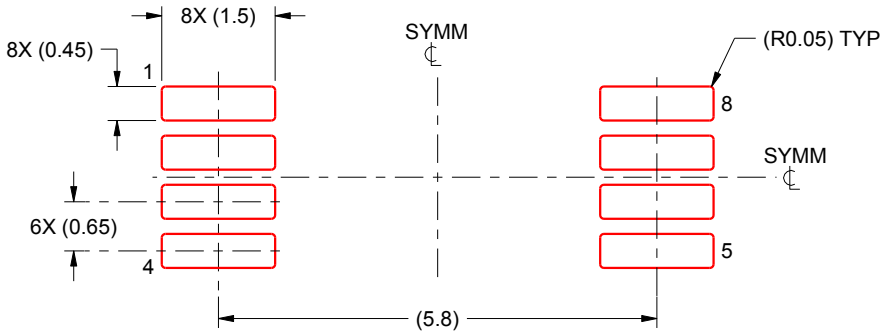


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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