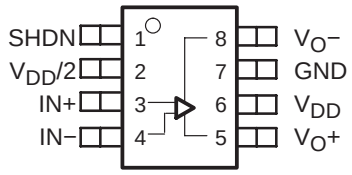
- **High Output Current Differential Drive . . . >200 mA**
- **Rail-To-Rail Output**
- **Unity-Gain Bandwidth . . . 2.4 MHz**
- **Slew Rate . . . 1.5 V/μs**
- **Supply Current . . . 1.4 mA**
- **Supply Voltage Range . . . 2.7 V to 5.5 V**
- **Specified Temperature Range:**
  − T_A = −40°C to 85°C . . . Industrial Grade

DGN PACKAGE
(TOP VIEW)



description

The TLV4120 single supply operational differential amplifier provides a differential output current in excess of 200 mA at 5 V. This enables the amplifier to be used as high current line drivers, buffers, or coil driver applications. The TLV4120 has a shutdown feature that reduces the supply current down to 6 μA when the amplifier is not active in the application.

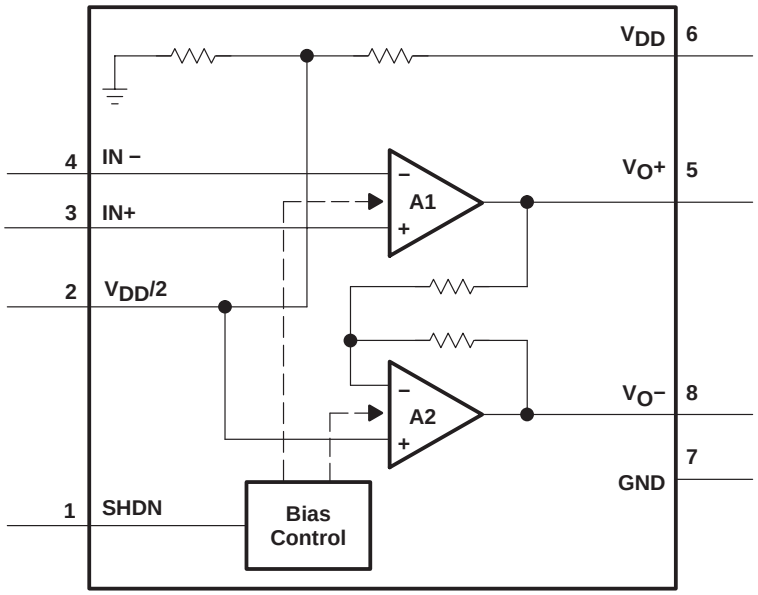
The TLV4120 is available in the ultrasmall MSOP PowerPAD™ package, which offers the exceptional thermal impedance required for amplifiers delivering high current levels.

AVAILABLE OPTIONS

T_A	DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES	SYMBOL	SHUTDOWN
			MSOP (DGN)†		
−40°C to 85°C	TLV4120	1	TLV4120IDGN	xxTIAHU	Yes

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV4120IDGNR).

functional block diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 6 V
Differential input voltage, V_{ID} . . . . . $\pm V_{DD}$
Input voltage range, V_I . . . . . $\pm V_{DD}$
Output current, I_O (see Note 2) . . . . . 800 mA
Continuous /RMS output current, I_O (each output of amplifier): $T_J \le 105°C$ . . . . . 350 mA
$T_J \le 150°C$ . . . . . 110 mA
Peak output current, I_O (each output of amplifier: $T_J \le 105°C$ . . . . . 500 mA
$T_J \le 150°C$ . . . . . 155 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: I suffix . . . . . −40°C to 85°C
Maximum junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to GND.
2. To prevent permanent damage the die temperature must not exceed the maximum junction temperature.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \le 25°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGN (8)‡	4.7	52.7	2.37 W	1.23 W

‡ See The Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2.7	5.5	V
Common-mode input voltage range, V_{ICR}		0.5	V_{DD}−0.5	V
Operating free-air temperature, T_A	I-suffix	−40	85	°C
Shutdown turn-on/off voltage level§	V(on)		$<V_{DD}/3$	V
	V(off)	$>V_{DD}\times 0.75$		

§ Relative to GND

electrical characteristics at recommend operating conditions, V_{DD} = 2.7 V and 5 V (unless otherwise noted)

dc performance

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNITS
V_{IO}	Input offset voltage	$V_{IC} = V_{DD}/2$,	$V_O = V_{DD}/2$, R_S = 50 Ω	25°C		100	3000	μV
				Full range			4000	
CMRR	Common-mode rejection ratio	V_{DD} = 2.7 V, R_S = 50 Ω	V_{IC} = 0.5 to 2.2 V,	25°C	69	95		dB
				Full range	66			
		V_{DD} = 5 V, R_S = 50 Ω	V_{IC} = 0.5 to 4.5 V,	25°C	71	95		
				Full range	68			
A_{VD}	Large-signal differential voltage amplification	V_{DD} = 2.7 V, $V_{O(PP)}$=1 V, $V_{IC} = V_{DD}/2$	R_L=100 Ω	25°C	80	85		dB
				Full range	70			
		V_{DD} = 5 V, $V_{O(PP)}$=3 V, $V_{IC} = V_{DD}/2$	R_L=100 Ω	25°C	90	95		
				Full range	80			

† Full range is −40°C to 85°C for I suffix.

input characteristics

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNITS
I_{IO}	Input offset current	$V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, R_S = 50 Ω	25°C		0.3	60	pA
			Full range			300	
I_{IB}	Input bias current		25°C		0.3	60	
			Full range			300	
$r_{i(d)}$	Differential input resistance		25°C		1000		GΩ
C_{IC}	Common-mode input capacitance	f = 100 Hz	25°C		5		pF
	$V_{DD}/2$ biasing resistors		25°C		500		kΩ
	Amplifier A2's gain resistors		25°C		20		kΩ

† Full range is −40°C to 85°C for I suffix.

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V and 5 V (unless otherwise noted) (continued)

output characteristics

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNITS
V_{OH}	High-level output voltage	V_{DD} = 2.7 V, V_{IC} = V_{DD}/2	I_{OH} = −10 mA	25°C	2.6	2.67		V
				Full range	2.58			
			I_{OH} =−100 mA	25°C	2.35	2.4		
				Full range	2.3			
		V_{DD} = 5 V, V_{IC} = V_{DD}/2	I_{OH} = −10 mA	25°C	4.9	4.96		
				Full range	4.88			
			I_{OH} = −100 mA	25°C	4.7	4.8		
				Full range	4.65			
			I_{OH} = −200 mA	25°C	4.45	4.55		
				Full range	4.38			
V_{OL}	Low−level output voltage	V_{DD} = 2.7 V , V_{IC} = V_{DD}/2	I_{OL} = 10 mA	25°C		0.03	0.1	V
				Full range			0.12	
			I_{OL} = 100 mA	25°C		0.3	0.4	
				Full range			0.5	
		V_{DD} = 5 V, V_{IC} = V_{DD}/2	I_{OL} = 10 mA	25°C		0.03	0.1	
				Full range			0.12	
			I_{OL} = 100 mA	25°C		0.2	0.3	
				Full range			0.35	
			I_{OL} = 200 mA	25°C		0.5	0.55	
				Full range			0.62	
I_O	Output current	Measured at 0.5 V from rail	V_{DD} = 2.7 V	25°C		320		mA
			V_{DD} = 5 V			200		

† Full range is− 40°C to 85°C for I suffix.

power supply

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNITS
I_{DD}	Supply current	V_O = V_{DD}/2, SHDN = <Vdd/3 V	25°C		1.4	1.7	mA
			Full range			2.3	
PSRR	Power supply rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} =2.7 to 3.3 V, V_{IC} = V_{DD}/2 V, No load	25°C	80	94		dB
			Full range	75			
		V_{DD} =2.7 to 5 V, V_{IC} = V_{DD}/2 V, No load	25°C	70	84		
			Full range	65			

† Full range is −40°C to 85°C for I suffix.

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V and 5 V (unless otherwise noted) (continued)

dynamic performance

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNITS
GBWP	Gain bandwidth product	R_L=100 Ω	C_L=10 pF	25°C		2.4		MHz
SR	Slew rate at unity gain	$V_{O(pp)}$ = $V_{DD/2}$, R_L = 100 Ω, C_L = 50 pF	V_{DD} = 2.7 V	25°C	0.75	1.48		V/μs
				Full range	0.5			
			V_{DD} = 5 V	25°C	0.9	1.57		
				Full range	0.65			
ϕM	Phase margin	R_L = 100 Ω,	C_L = 10 pF	25°C		60		
	Gain margin					20		dB
V_n	Input noise voltage	f = 10 kHz		25°C		10		nV/√Hz

† Full range is −40°C to 85°C for I suffix.

shutdown characteristics

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNITS
$I_{DD(SHDN)}$	Supply current in shutdown mode	SHDN > Vdd × 0.75	25°C		6	12	μA
			Full range			50	

† Full range is −40°C to 85°C for I suffix.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{OH}	High-level output voltage	vs High-level output current	1, 3
V_{OL}	Low-level output voltage	vs Low-level output current	2, 4
Z_O	Output impedance	vs Frequency	5
P_O	Output power	vs Load resistance	6
I_{DD}	Supply current	vs Supply voltage	7
PSRR	Power supply rejection ratio	vs Frequency	8
A_{vd}	Differential voltage amplification and phase	vs Frequency	9
	Phase margin	vs Capacitive load	10
	Slew rate	vs Free-air temperature	11
		vs Supply voltage	12
	Total harmonic distortion + noise	vs Frequency	13
	Inverting large-signal pulse response	vs Time	14
	Inverting small-signal pulse response	vs Time	15
$I_{DD(SHDN)}$	Shutdown supply current	vs Free-air temperature	16
$I_{DD(SHDN)}$	Shutdown supply current	vs Supply voltage	17
	Shutdown mode pulse response	vs Time	18

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

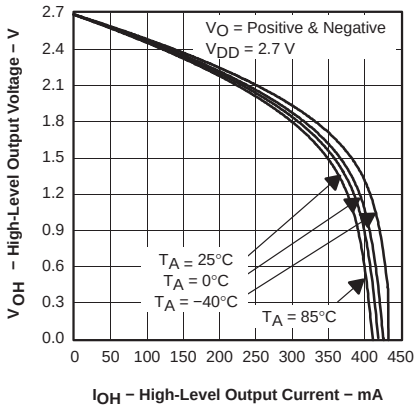


Figure 1

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

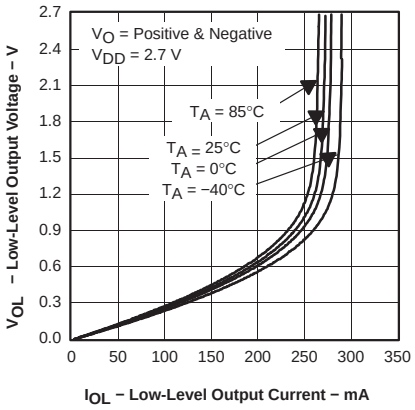


Figure 2

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

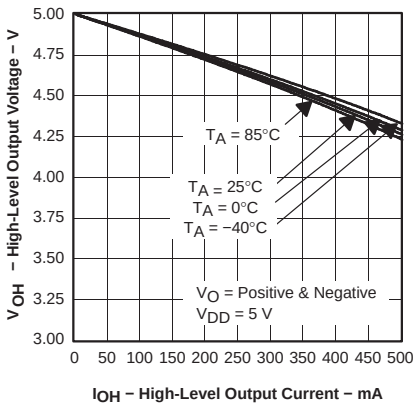


Figure 3

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

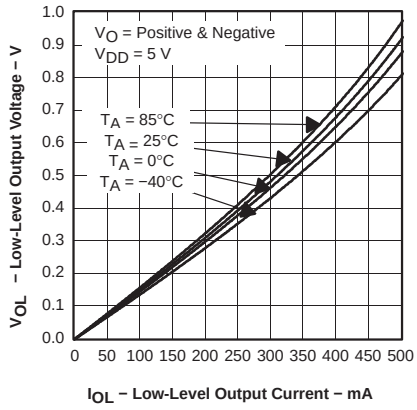


Figure 4

OUTPUT IMPEDANCE vs FREQUENCY

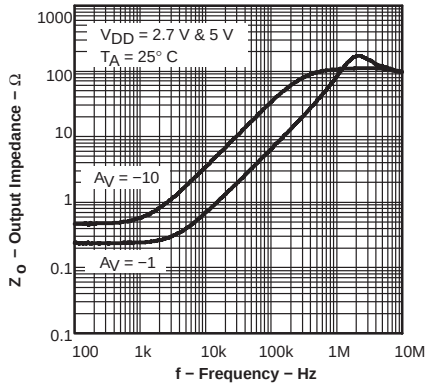


Figure 5

OUTPUT POWER vs LOAD RESISTANCE

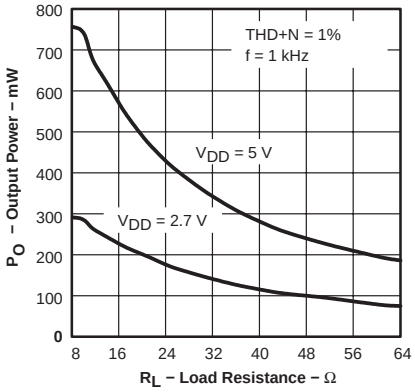


Figure 6

SUPPLY CURRENT vs SUPPLY VOLTAGE

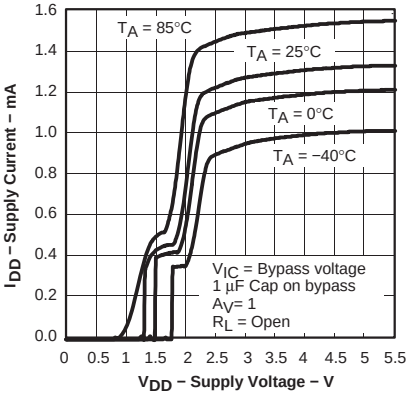


Figure 7

POWER SUPPLY REJECTION RATIO vs FREQUENCY

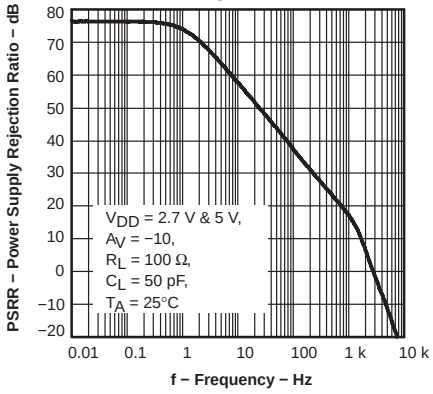


Figure 8

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE vs FREQUENCY

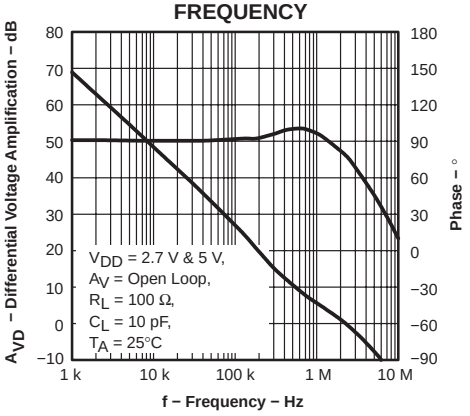


Figure 9

PHASE MARGIN vs CAPACITIVE LOAD

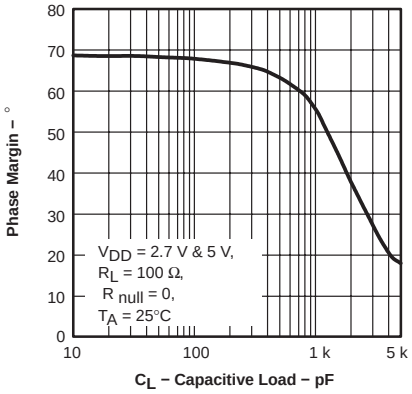


Figure 10

SLEW RATE vs FREE-AIR TEMPERATURE

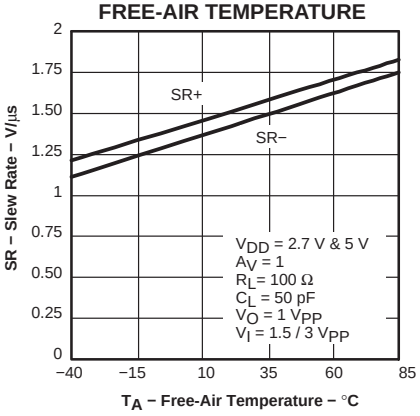


Figure 11

SLEW RATE vs SUPPLY VOLTAGE

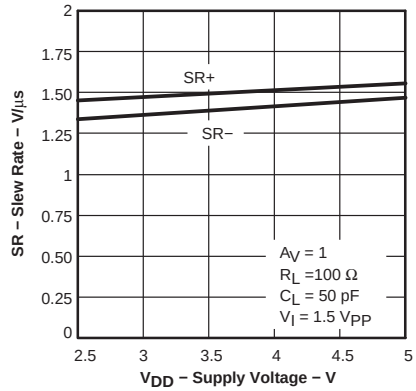


Figure 12

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

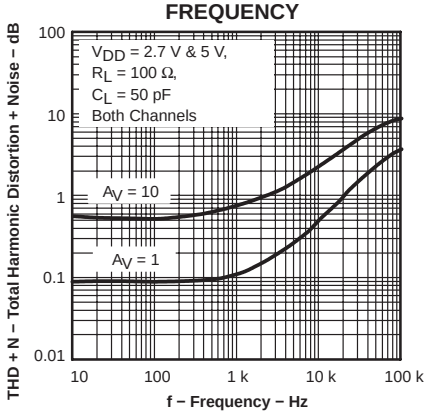


Figure 13

INVERTING LARGE-SIGNAL PULSE RESPONSE vs TIME

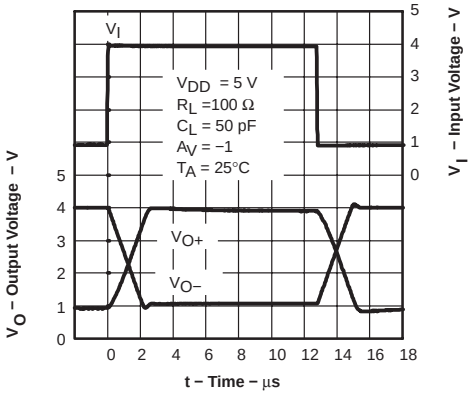


Figure 14

TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL PULSE RESPONSE vs TIME

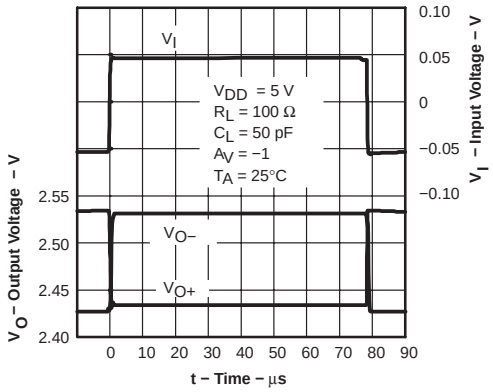


Figure 15

SHUTDOWN SUPPLY CURRENT vs FREE-AIR TEMPERATURE

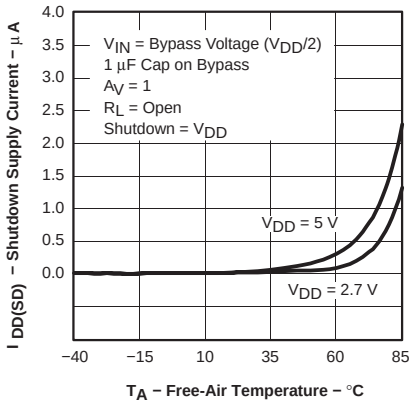


Figure 16

SHUTDOWN SUPPLY CURRENT vs SUPPLY VOLTAGE

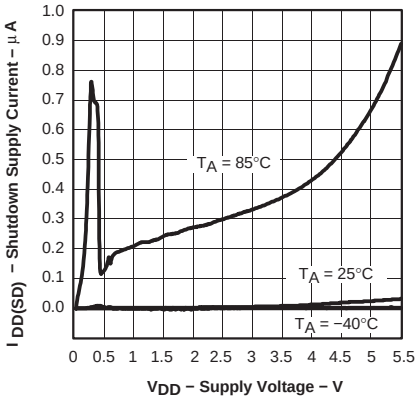


Figure 17

SHUTDOWN MODE PULSE RESPONSE vs TIME

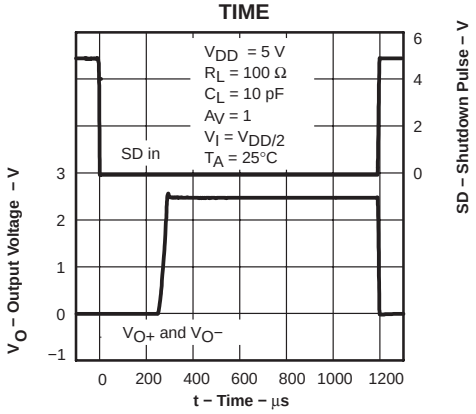


Figure 18

APPLICATION INFORMATION

differential output drive

The TLV4120 is two amplifiers arranged to produce high output current differential drive. The first amplifier, A1, is an operational amplifier, with both inputs uncommitted. This enables the first amplifier to be configured as an inverting amplifier, a noninverting amplifier, or even a difference amplifier. The second amplifier, A2, is internally configured as an inverting amplifier and biased about $V_{DD}/2$.

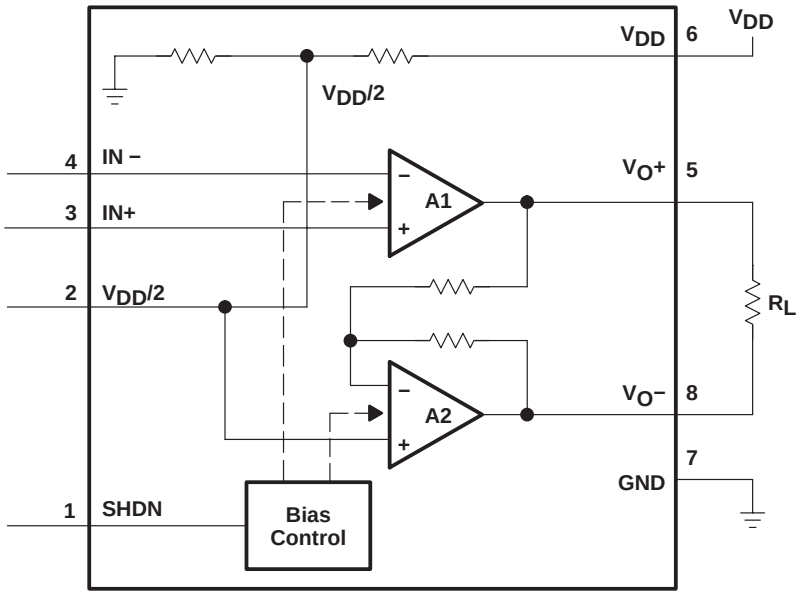


Figure 19

This approach makes a simple solution to single-ended to differential drive or even differential to differential drive.

When using the TLV4120 to drive heavy differential loads, care must be taken not to saturate the output of the first amplifier, as the second amplifier will produce a mirror image (about $V_{DD}/2$) of the first amplifier's output. This can lead to asymmetrical differential output swings.

This differential output drive configuration is ideal for low frequency high current drive applications, such as line drivers, driving LVDTs.

APPLICATION INFORMATION

Figure 20 shows the TLV4120 amplifier driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the load means that as one side is slewing up, the other side is slewing down, and vice versa. This doubles the voltage swing on the load as compared to a ground-referenced load, quadrupling the power delivered to the load.

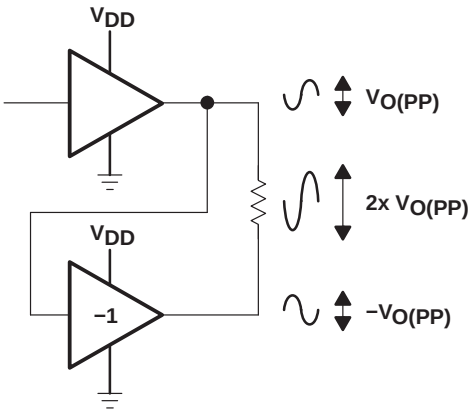


Figure 20. Bridge-Tied Load Configuration

component selection

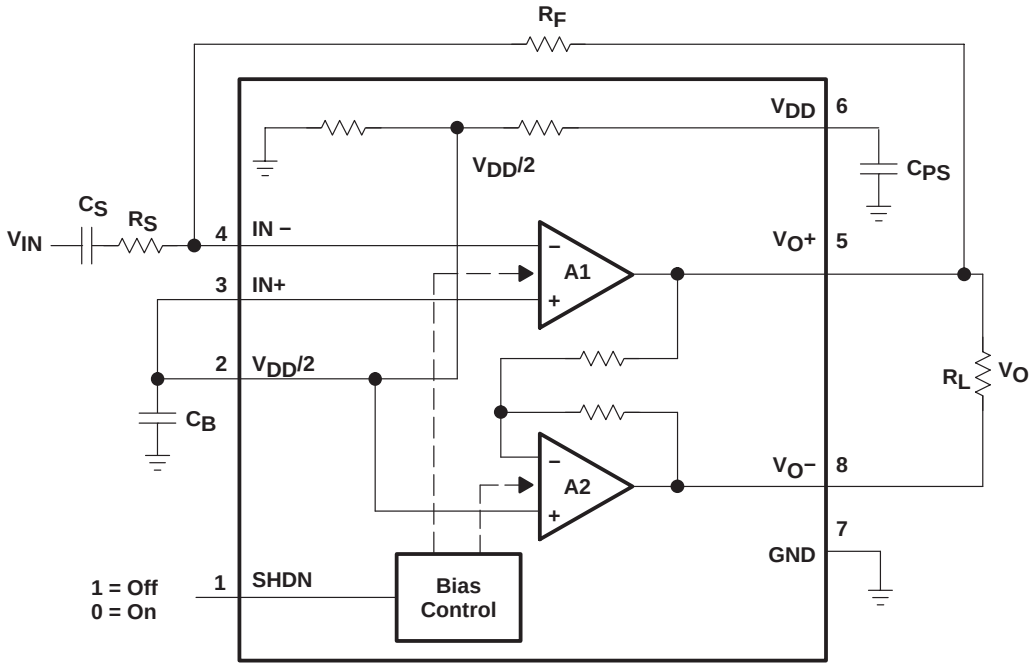


Figure 21. Driving a Capacitive Load

APPLICATION INFORMATION

gain setting resistors, R_F and R_S

The differential gain for the TLV4120, with A1 configured as an inverter, is set by resistors R_F and R_S using the following equation:

$$\text{DiffGain} = -2 \times \left(\frac{R_F}{R_S}\right)$$

The differential gain for the TLV4120, with A1 in a noninverting configuration, is set by resistors R_F and R_S using the following equation:

$$\text{DiffGain} = 2 \times \left(1 + \frac{R_F}{R_S}\right)$$

Differential drive operation brings about the factor 2 in the gain equation due to amplifier A2, configured as an inverter, mirroring the voltage swing across the load.

Given that the TLV4120 is a MOS amplifier, the input impedance is very high; consequently input bias currents in most cases will not generally be a concern (see offset voltage application section). However, the noise in the circuit will increase as R_F increases. Typical values for R_F will range between 5 kΩ and 20 kΩ.

Large values of feedback resistor, R_F, at low gains can cause instability due to the pole caused by the input capacitance. This can be alleviated by either reducing the size of R_F or by putting a small capacitor in parallel with R_F.

AC coupling capacitor, C_S

When the input to the TLV4120 will be AC coupled to the input source, a high pass filter is formed with a corner frequency equal to:

$$f_c = \frac{1}{2\pi R_S C_S}$$

The value of C_S is important to consider as it directly affects the low frequency operation of the circuit.

A further consideration for this capacitor is the leakage path from the input source through the input network (R_S, C_S) and the feedback resistor (R_F) to the load. This leakage current creates a dc-offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

power supply decoupling, C_{PS}

The TLV4120 is a high-performance CMOS amplifier that requires adequate power supply decoupling to ensure stability and low total harmonic distortion (THD). Optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the amplifier is recommended.

APPLICATION INFORMATION

$V_{DD}/2$ bypass capacitor, C_B

The $V_{DD}/2$ bypass capacitor, C_B, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the mid-rail generation circuit internal to the amplifier, which appears as degraded PSRR and THD + N. The capacitor is fed from two internal 500-kΩ potential-dividing resistors. To keep the start-up bounce as low as possible, the relationship shown in equation 4 should be maintained. This ensures the input capacitor is fully charged before the bypass capacitor is fully charged and the amplifier starts up.

$$\frac{10}{\left(C_B \times 250\ k\Omega\right)} \leq \frac{1}{\left(R_F + R_S\right) C_S}$$

As an example, consider a circuit where C_B is 2.2 µF, C_S is 0.47 µF, R_F is 50 kΩ, and R_S is 10 kΩ. Inserting these values into equation 4 produces the following:

$$18.2 \leq 35.5$$

which satisfies the rule. For bypass capacitor, C_B , 0.1-µF to 2.2-µF ceramic or tantalum low-ESR capacitors are recommended for the best stability and noise performance.

using low-ESR capacitors

Low-ESR capacitors are recommended. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

shutdown function

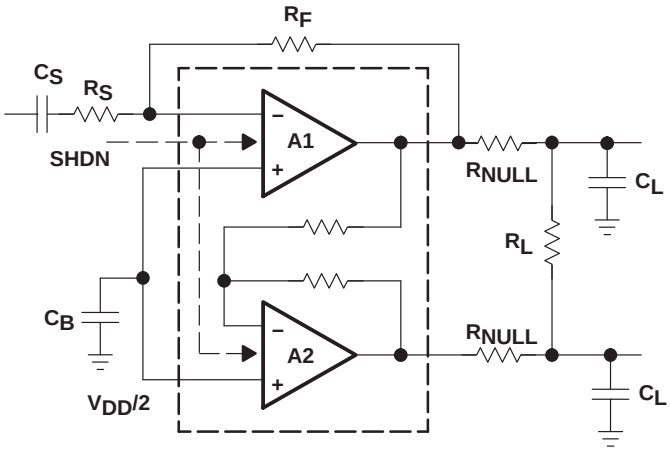
The TLV4120 has a shutdown terminal for conserving power in energy sensitive applications. When the shutdown terminal is pulled high the amplifier is disabled, placing the outputs into a high impedance state and reducing the supply current to the order of microamperes.

To enable the amplifier, the shutdown terminal must be pulled low. If open drain logic is used, pull-up resistors must be employed to ensure proper and known shutdown status. It is not recommended that the shutdown input is left to float, as the device could inadvertently shutdown.

APPLICATION INFORMATION

driving a capacitive load

When the amplifier is used to drive heavy capacitive loads, the device's phase margin will be reduced which could lead to high frequency ringing or oscillations. The TLV4120's high current drive capability reduces this possibility. However, for capacitive loads of greater than 1 nF, it is suggested that a resistor be placed in series (R_{NULL}) with the output of the amplifier as shown in Figure 22 which should help reduce the ringing.



NOTE: R_{NULL} will reduce the output drive capability of the TLV4120.

Figure 22. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of:

1. The input offset voltage (V_{IO}) multiplied by the noninverting gain
2. The noninverting input bias current (I_{IB}) multiplied by the resistance on this node multiplied by the noninverting gain
3. The inverting bias current multiplied by the feedback resistor.

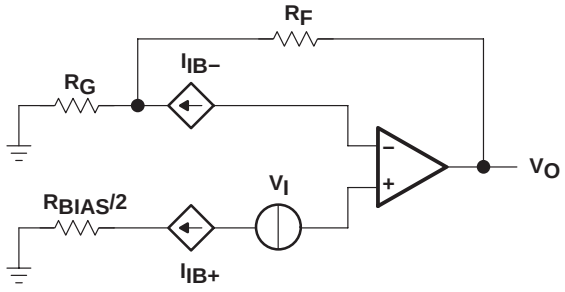


Figure 23. Output Offset Voltage Model

APPLICATION INFORMATION

offset voltage (continued)

The differential nature of the TLV4120 means that both amplifiers must be considered together to calculate the differential output offset voltage (V_{DOO}) (see Figure 24). The V_{OO} of amplifier A1 will be inverted by amplifier A2. This doubles A1's V_{OO} and has A2's V_{OO} added to it, yielding:

$$V_{DOO} = 2V_{IO1} \times \left(1 + \left(\frac{R_F}{R_S}\right)\right) \pm I_{IB+}\ 500k \times \left(1 + \left(\frac{R_F}{R_S}\right)\right) \pm 2I_{IB-}\ R_F - 2V_{IO2} \pm I_{IB+}\ 500k \pm I_{IB-}20k$$

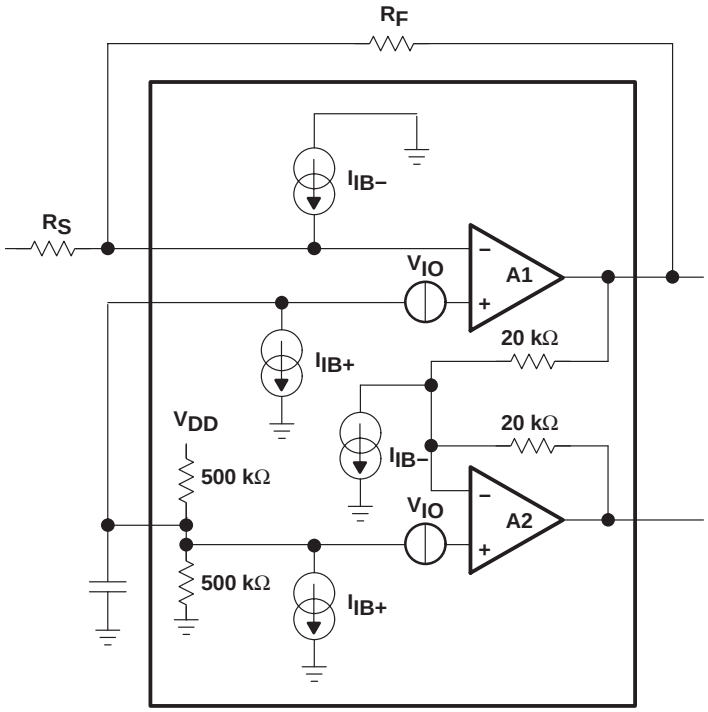


Figure 24. TLV4120 Offset Voltage Model

APPLICATION INFORMATION

general power design considerations

When driving heavy loads at high junction temperatures there is an increased probability of electromigration affecting the long term reliability of ICs. Therefore for this not to be an issue:

- The output current must be limited (at these high junction temperatures) or
- The junction temperature must be limited.

The maximum continuous output current at a die temperature of 150°C will be 1/3 of the current at 105°C.

The junction temperature will be dependent on the ambient temperature around the IC, thermal impedance from the die to the ambient, and power dissipated within the IC.

$$T_J = T_A + \theta_{JA} \times P_{DIS}$$

Where:

P_{DIS} is the IC power dissipation and is equal to the output current multiplied by the voltage dropped across the output of the IC.

θ_{JA} is the thermal impedance between the junction and the ambient temperature of the IC.

T_J is the junction temperature.

T_A is the ambient temperature.

Reducing one or more of these factors will result in a reduced die temperature.

The use of the MSOP PowerPAD dramatically reduces the thermal impedance from junction to case. And with correct mounting, the reduced thermal impedance will greatly increase the IC's permissible power dissipation and output current handling capability. For example, the power dissipation of the PowerPAD is increased to above 1 W. Sinusoidal and pulse-width modulated output signals will also increase the output current capability. The equivalent dc current is proportional to the square-root of the duty cycle:

$$I_{DC(EQ)} = I_{Cont} \times \sqrt{(\text{duty cycle})}$$

CURRENT DUTY CYCLE AT PEAK RATED CURRENT	EQUIVALENT DC CURRENT AS A PERCENTAGE OF PEAK CURRENT
100	100
70	84
50	71

Note that with an operational amplifier, a duty cycle of 70% will often result in the op-amp sourcing current 70% of the time and sinking current 30%; therefore, the equivalent dc current will still be 0.84 times the continuous current rating at a particular junction temperature.

The differential nature of the TLV4120 means that it will dissipate approximately four times the power of a single-ended amplifier driving a similar load referenced to mid rail. The TLV4120 will however be delivering four times the power to the load.

APPLICATION INFORMATION

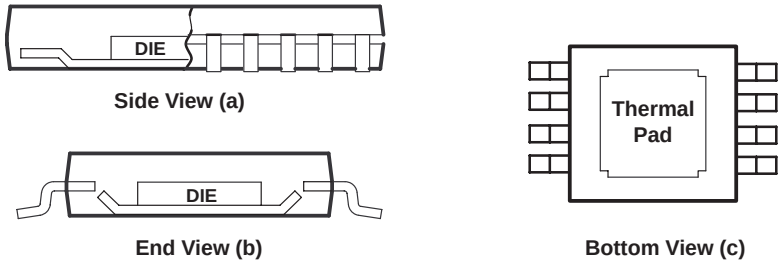
general PowerPAD design considerations

The TLV4120 is available in a thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 25(a) and Figure 25(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 25(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

Soldering the PowerPAD to the PCB is always recommended, even with applications that have low-power dissipation. This provides the necessary connection between the lead frame die pad and the PCB.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with mechanical heatsinking methods.



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Figure 25. Views of Thermally-Enhanced DGN Package

APPLICATION INFORMATION

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

general PowerPAD design considerations (continued)

1. The thermal pad must be connected to the same voltage potential as the device GND pin.
2. Prepare the PCB with a top side etch pattern as illustrated in the thermal land pattern mechanical drawing at the end of this document. There should be etch for the leads as well as etch for the thermal pad.
3. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
4. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the TLV4120 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
5. Connect all holes to the internal ground plane that is at the same voltage potential as the GND pin.
6. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the TLV4120 PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
7. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
8. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
9. With these preparatory steps in place, the TLV4120 IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For a given θ_{JA}, the maximum power dissipation is shown in Figure 26 and is calculated by the following formula:

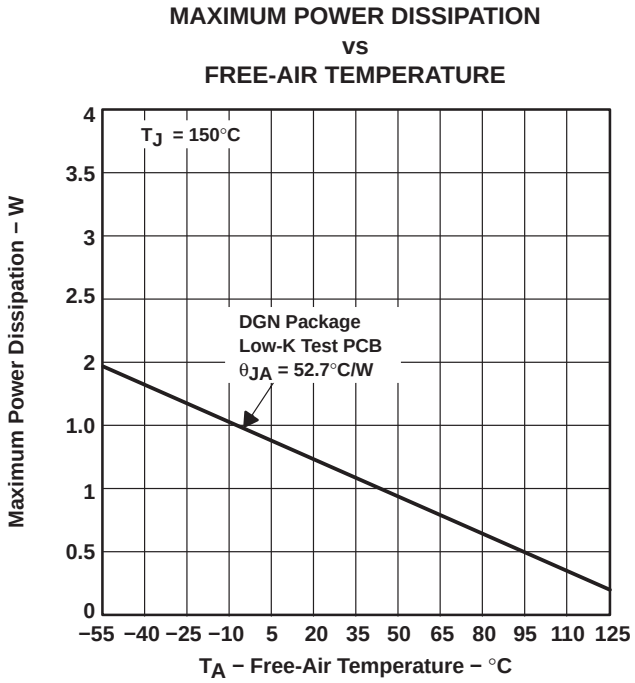
$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of TLV4120 IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

APPLICATION INFORMATION

general PowerPAD design considerations (continued)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 26. Maximum Power Dissipation vs Free-Air Temperature

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents.

The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV4120IDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHU	Samples
TLV4120IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

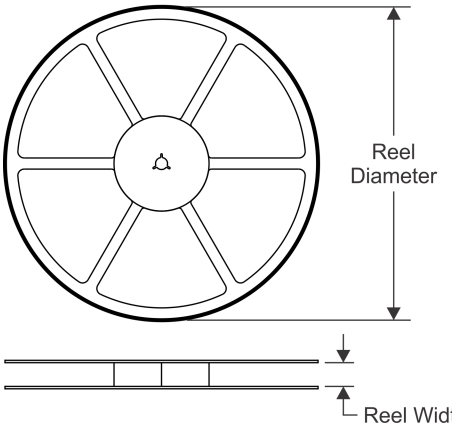
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

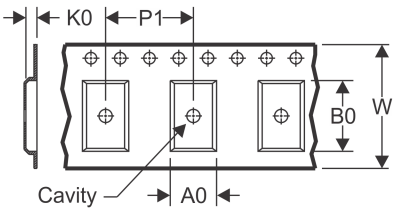
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

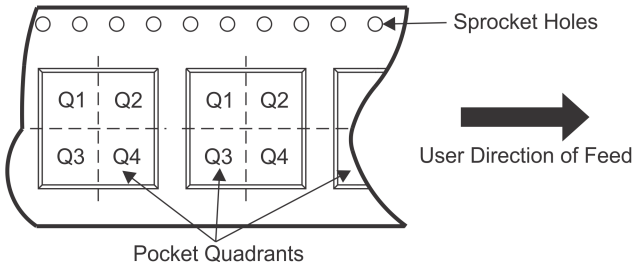


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

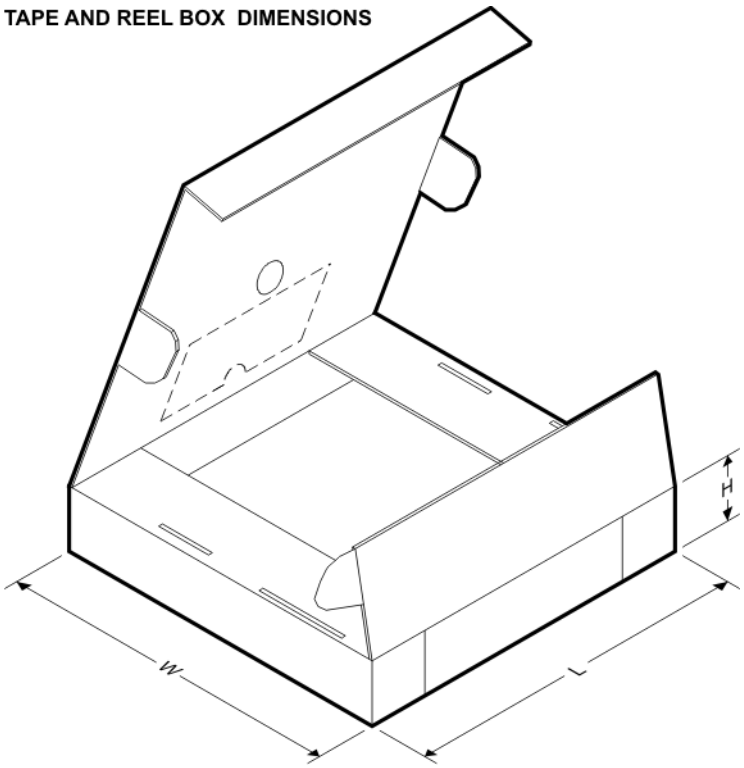
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV4120IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV4120IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0

GENERIC PACKAGE VIEW

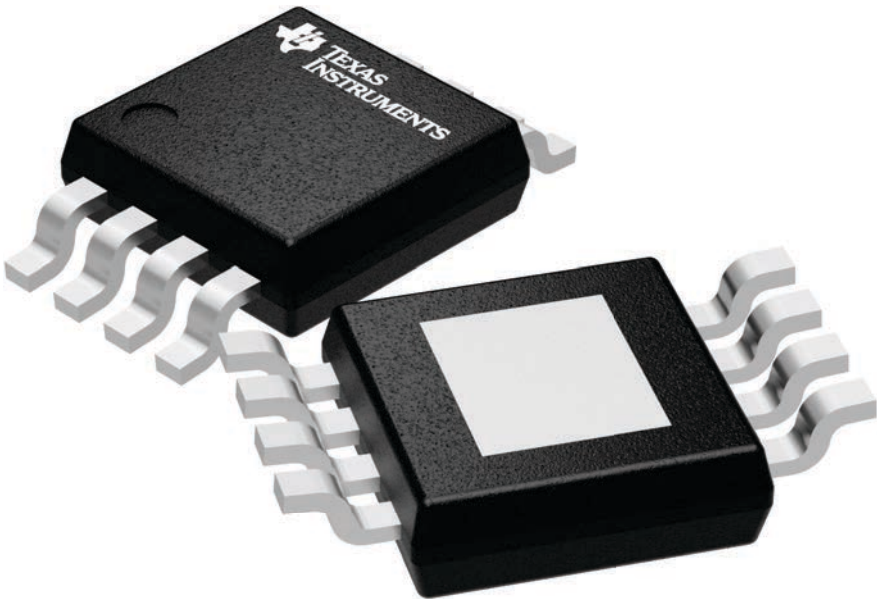
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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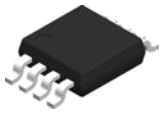
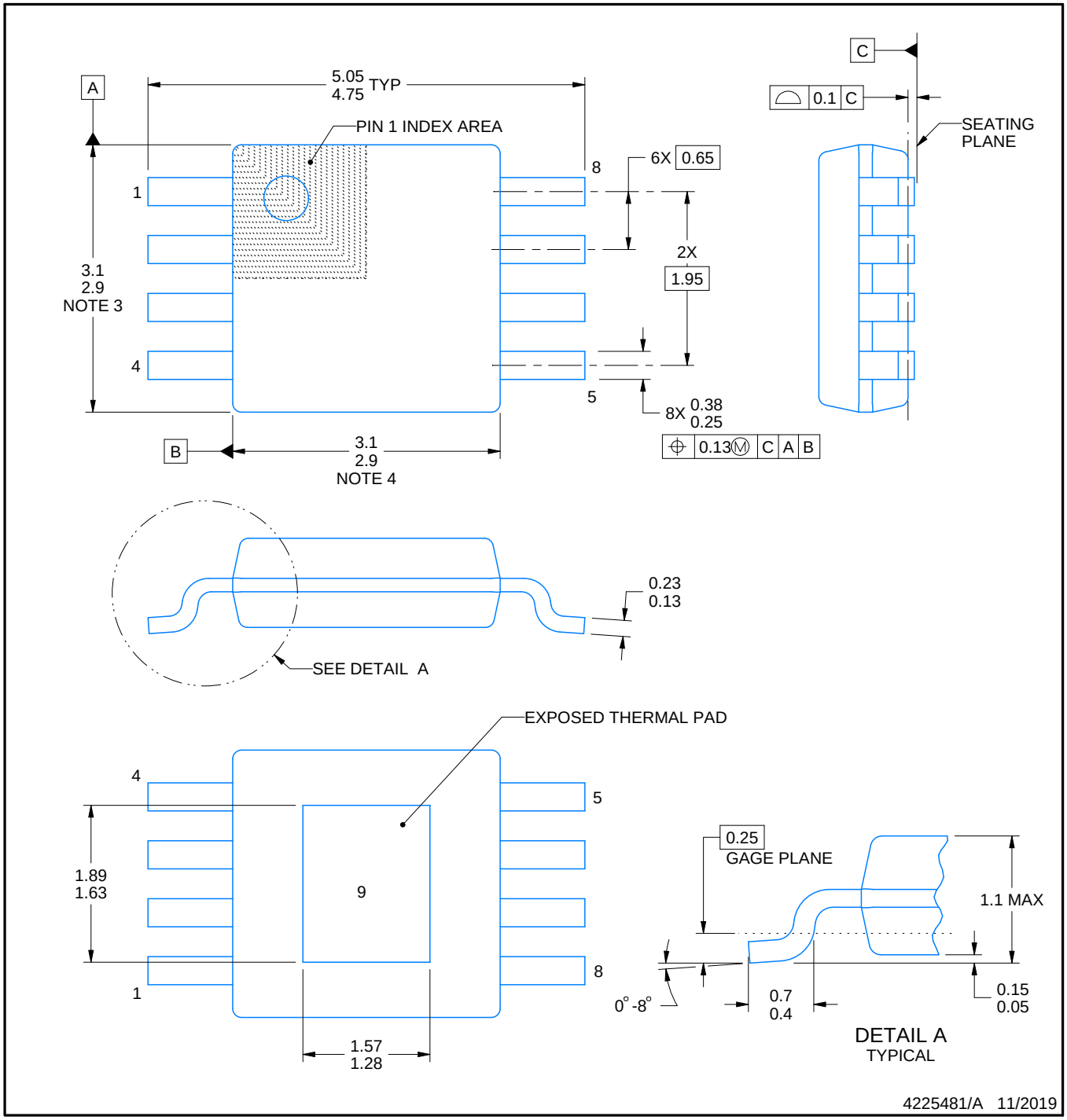
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

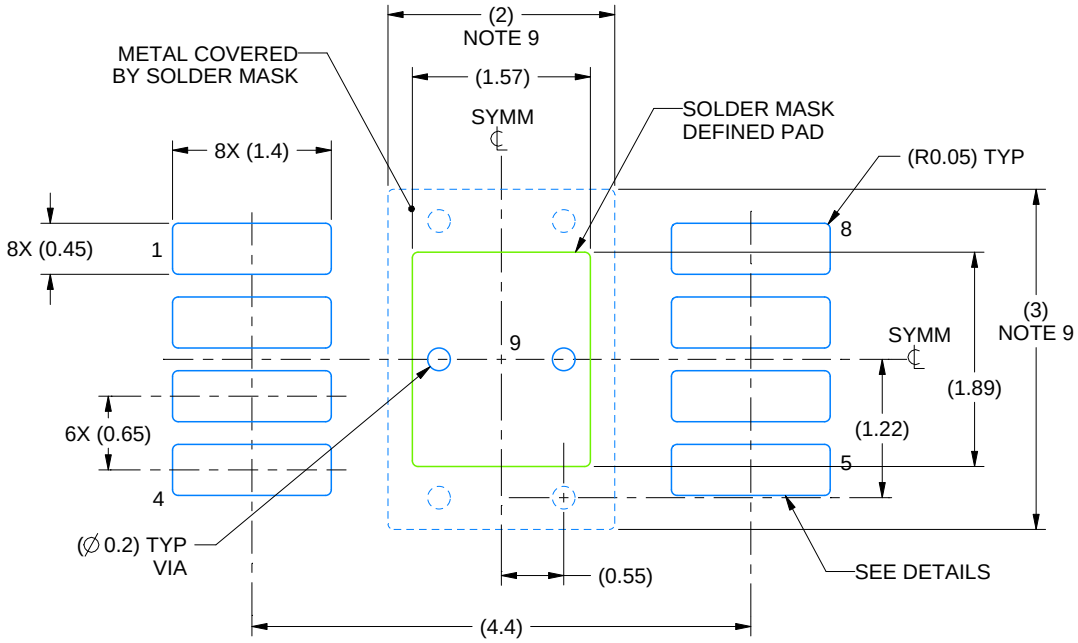
SMALL OUTLINE PACKAGE



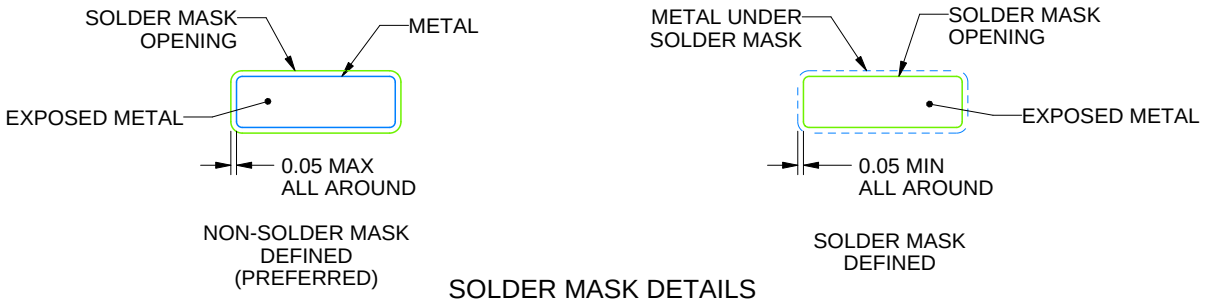
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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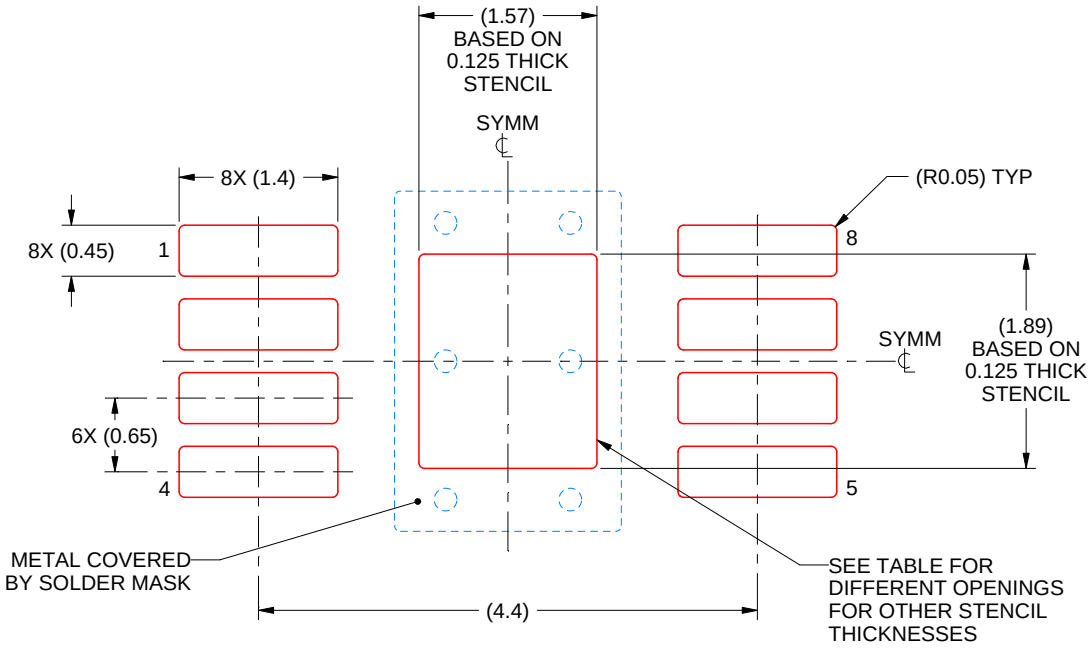
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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