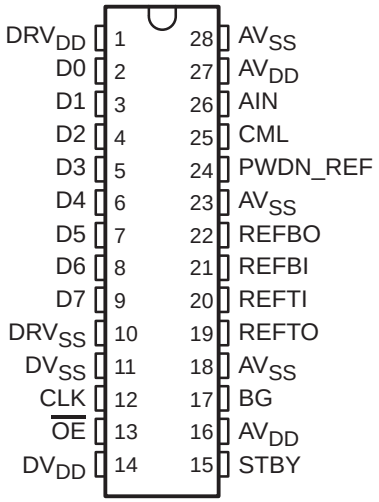
- **8-Bit Resolution 80 MSPS Sampling Analog-to-Digital Converter (ADC)**
- **Low Power Consumption: 165 mW Typ Using External references**
- **Wide Analog Input Bandwidth: 700 MHz Typ**
- **3.3 V Single-Supply Operation**
- **3.3 V TTL/CMOS-Compatible Digital I/O**
- **Internal Bottom and Top Reference Voltages**
- **Adjustable Reference Input Range**
- **Power Down (Standby) Mode**
- **Separate Power Down for Internal Voltage References**
- **Three-State Outputs**
- **28-Pin Small Outline IC (SOIC) and Thin Shrink SOP (TSSOP) Packages**
- **Applications**
  - **Digital Communications**
  - **Flat Panel Displays**
  - **High-Speed DSP Front-End (TMS320C6000)**
  - **Medical Imaging**
  - **Graphics Processing (Scan Rate/Format Conversion)**
  - **DVD Read Channel Digitization**

DW OR PW PACKAGE
(TOP VIEW)



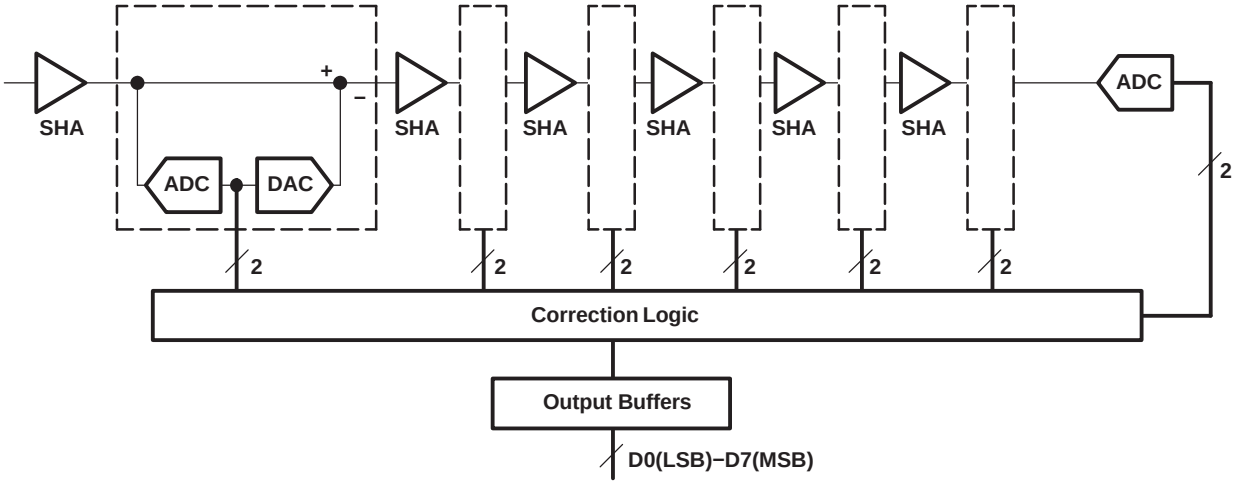
DESCRIPTION

The TLV5580 is an 8-bit 80 MSPS high-speed A/D converter. It converts the analog input signal into 8-bit binary-coded digital words up to a sampling rate of 80 MHz. All digital inputs and outputs are 3.3 V TTL/CMOS-compatible.

The device consumes very little power due to the 3.3 V supply and an innovative single-pipeline architecture implemented in a CMOS process. The user obtains maximum flexibility by setting both bottom and top voltage references from user-supplied voltages. If no external references are available, on-chip references are available for internal and external use. The full-scale range is 1 Vpp up to 1.6 Vpp, depending on the analog supply voltage. If external references are available, the internal references can be disabled independently from the rest of the chip, resulting in an even greater power saving.

While usable in a wide variety of applications, the device is specifically suited for the digitizing of high-speed graphics and for interfacing to LCD panels or LCD/DMD projection modules . Other applications include DVD read channel digitization, medical imaging and communications. This device is suitable for IF sampling of communication systems using sub-Nyquist sampling methods because of its high analog input bandwidth.

FUNCTIONAL BLOCK DIAGRAM



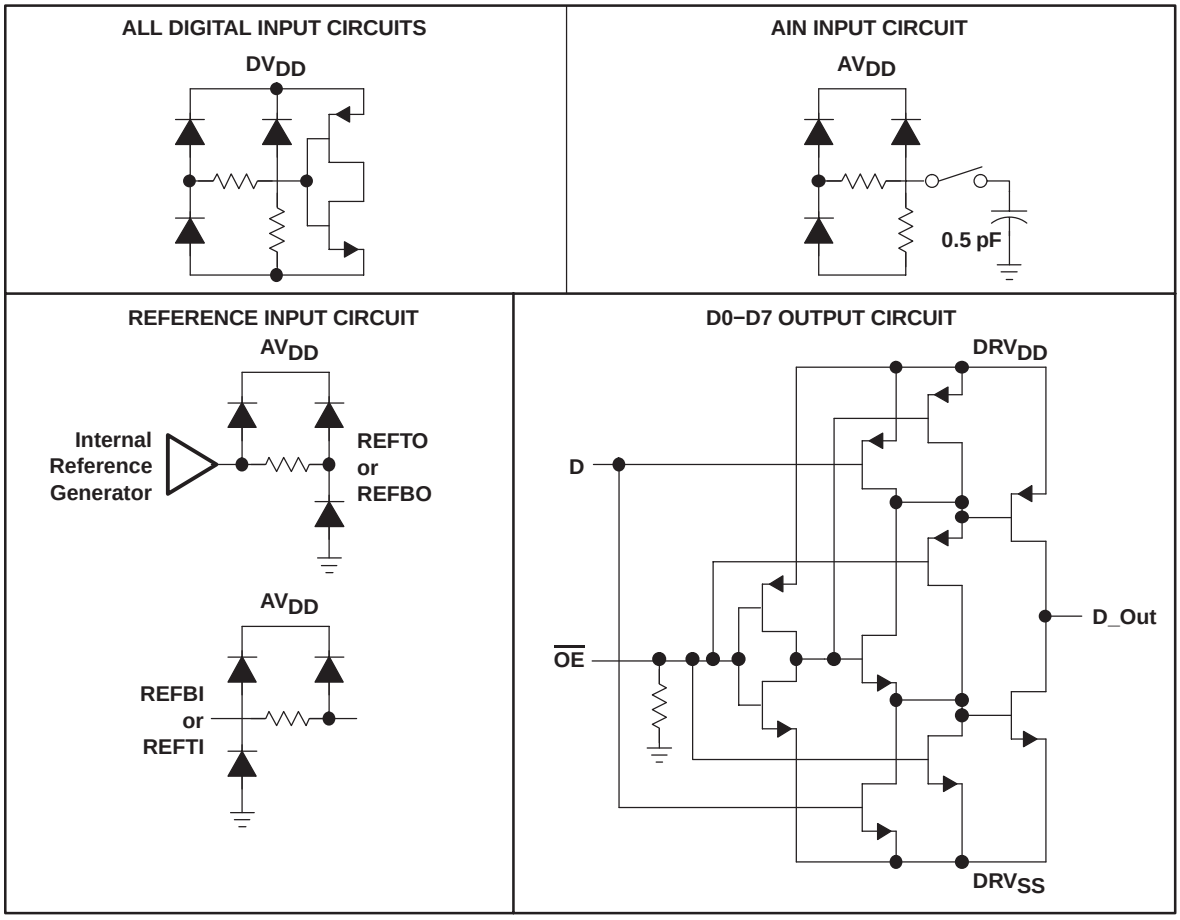
The single-pipeline architecture uses 6 ADC/DAC stages and one final flash ADC. Each stage produces a resolution of 2 bits. The correction logic generates its result using the 2-bit result from the first stage, 1 bit from each of the 5 succeeding stages, and 1 bit from the final stage in order to arrive at an 8-bit result. The correction logic ensures no missing codes over the full operating temperature range.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE−LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLV5580	SOIC, 28	DW	0°C to +70°C	TLV5580C	TLV5580CDW	Rails, 20
″	″	″	″	″	TLV5580CDWR	Tape and Reel, 1000
TLV5580	TSSOP. 28	PW	0°C to +70°C	TV5580	TLV5580CPW	Rails, 20
″	″	″	″	″	TLV5580CPWR	Tape and Reel, 2000
TLV5580	SOIC, 28	DW	−40°C to +85°C	TLV5580I	TLV5580IDW	Rails, 50
″	″	″	″	″	TLV5580IDWR	Tape and Reel, 1000
TLV5580	TSSOP, 28	PW	−40°C to +85°C	TY5580	TLV5580IPW	Rails, 50
″	″	″	″	″	TLV5580IPWR	Tape and Reel, 2000

(1) For the most current specifications and package information, refer to our web site at www.ti.com.

CIRCUIT DIAGRAMS OF INPUTS AND OUTPUTS



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AIN	26	I	Analog input
AV_{DD}	16, 27	I	Analog supply voltage
AV_{SS}	18, 23, 28	I	Analog ground
BG	17	O	Band gap reference voltage. A 1 μF capacitor (with an optional 0.1 μF capacitor in parallel) should be connected between this terminal and AV_{SS} for external filtering.
CLK	12	I	Clock input. The input is sampled on each rising edge of CLK.
CML	25	O	Common mode level. This voltage is equal to (AV_{DD} − AV_{SS}) ÷ 2. An external 0.1 μF capacitor should be connected between this terminal and AV_{SS}.
D0 − D7	2 − 9	O	Data outputs. D7 is the MSB
DRV_{DD}	1	I	Supply voltage for digital output drivers
DRV_{SS}	10	I	Ground for digital output drivers
DV_{DD}	14	I	Digital supply voltage
$\overline{OE}$	13	I	Output enable. When high the D0 − D7 outputs go in high-impedance mode.
DV_{SS}	11	I	Digital ground
PWDN_REF	24	I	Power down for internal reference voltages. A high on this terminal will disable the internal reference circuit.
REFBI	21	I	Reference voltage bottom input. The voltage at this terminal defines the bottom reference voltage for the ADC. It can be connected to REFBO or to an externally generated reference level. Sufficient filtering should be applied to this input. The use a 0.1 μF capacitor connected between REFBI and AV_{SS} is recommended. Additionally, a 0.1 μF capacitor can be connected between REFTI and REFBI.
REFBO	22	O	Reference voltage bottom output. An internally generated reference is available at this terminal. It can be connected to REFBI or left unconnected. A 1 μF capacitor between REFBO and AV_{SS} will provide sufficient decoupling required for this output.
REFTI	20	I	Reference voltage top input. The voltage at this terminal defines the top reference voltage for the ADC. It can be connected to REFTO or to an externally generated reference level. Sufficient filtering should be applied to this input. The use of a 0.1 μF capacitor between REFTI and AV_{SS} is recommended. Additionally, a 0.1 μF capacitor can be connected between REFTI and REFBI.
REFTO	19	O	Reference voltage top output. An internally generated reference is available at this terminal. It can be connected to REFTI or left unconnected. A 1 μF capacitor between REFTO and AV_{SS} will provide sufficient decoupling required for this output.
STBY	15	I	Standby input. A high level on this input enables a power-down mode.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE (unless otherwise noted)†

Supply voltage: AV_{DD} to AGND, DV_{DD} to DGND . . . . . −0.5 V to 4.5 V
Supply voltage: AV_{DD} to DV_{DD}, AGND to DGND . . . . . −0.5 V to 0.5 V
Digital input voltage range to DGND . . . . . −0.5 V to DV_{DD} + 0.5 V
Analog input voltage range to AGND . . . . . −0.5 V to AV_{DD} + 0.5 V
Digital output voltage applied from external source to DGND . . . . . −0.5 V to DV_{DD} + 0.5 V
Reference voltage input range to AGND: $V_{(REFTI)}$, $V_{(REFTO)}$, $V_{(REFBI)}$, $V_{(REFBO)}$ −0.5 V to AV_{DD} + 0.5 V
Operating free-air temperature range, T_A: TLV5580C . . . . . 0°C to 70°C
TLV5580I . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −55°C to 150°C

(1) †Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS OVER OPERATING FREE-TEMPERATURE RANGE

POWER SUPPLY

		MIN	NOM	MAX	UNIT
Supply voltage	AV_{DD}	3	3.3	3.6	V
	DV_{DD}				
	DRV_{DD}				

ANALOG AND REFERENCE INPUTS

	MIN	NOM	MAX	UNIT
Reference input voltage (top), $V_{(REFTI)}$	(NOM) − 0.2	2 + (AV_{DD} − 3)	(NOM) + 0.2	V
Reference input voltage (bottom), $V_{(REFBI)}$	0.8	1	1.2	V
Reference voltage differential, $V_{(REFTI)} - V_{(REFBI)}$			1 + (AV_{DD} − 3)	V
Analog input voltage, $V_{(AIN)}$	$V_{(REFBI)}$		$V_{(REFTI)}$	V

DIGITAL INPUTS

	MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	2.0		DV_{DD}	V
Low-level input voltage, V_{IL}	DGND		0.2xDV_{DD}	V
Clock period, t_c	12.5			ns
Pulse duration, clock high, $t_{w(CLKH)}$	5.25			ns
Pulse duration, clock low, $t_{w(CLKL)}$	5.25			ns

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS WITH F_{CLK} = 80 MSPS AND USE OF EXTERNAL VOLTAGE REFERENCES (unless otherwise noted)

POWER SUPPLY

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Operating supply current	AV_{DD}	AV_{DD} = DV_{DD} = 3.3 V, DRV_{DD} = 3 V, C_L = 15 pF, V_I = 1 MHz, −1 dBFS		57	71	mA
		DV_{DD}			3	3.6	
		DRV_{DD}			5	7.5	
P_D	Power dissipation		PWDN_REF = L		213	270	mW
			PWDN_REF = H		165	210	
$P_{D(STBY)}$	Standby power		STBY = H, CLK held high or low		11	15	

DIGITAL LOGIC INPUTS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current on CLK†	AV_{DD} = DV_{DD} = DRV_{DD} = CLK = 3.6 V			10	µA
I_{IL}	Low-level input current on digital inputs ($\overline{OE}$, STDBY, PWDN_REF, CLK)	AV_{DD} = DV_{DD} = DRV_{DD} = 3.6 V, Digital inputs at 0 V			10	µA
C_I	Input capacitance			5		pF

† I_{IH} leakage current on other digital inputs ($\overline{OE}$, STDBY, PWDN_REF) is not measured since these inputs have an internal pull-down resistor of 4 KΩ to DGND.

LOGIC OUTPUTS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	AV_{DD} = DV_{DD} = DRV_{DD} = 3 V at I_{OH} = 50 µA, Digital output forced high	2.8			V
V_{OL}	Low-level output voltage	AV_{DD} = DV_{DD} = DRV_{DD} = 3.6 V at I_{OL} = 50 µA, Digital output forced low			0.1	V
C_O	Output capacitance			5		pF
I_{OZH}	High-impedance state output current to high level	AV_{DD} = DV_{DD} = DRV_{DD} = 3.6 V			10	µA
I_{OZL}	High-impedance state output current to low level				10	µA

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS WITH F_{CLK} = 80 MSPS AND USE OF EXTERNAL VOLTAGE REFERENCES (unless otherwise noted)

DC ACCURACY

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Integral nonlinearity (INL), best-fit	Internal references (see Note 1)	T_A = −40°C to 85°C	−2.4	±1	2.4	LSB
Differential nonlinearity (DNL)	Internal references (see Note 2)	T_A = −40°C to 85°C	−1	±0.6	1.3	LSB
Zero error	AV_{DD} = DV_{DD} = 3.3 V, DRV_{DD} = 3 V See Note 3				5	%FS
Full scale error					5	%FS

1. Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full−scale point is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two endpoints.
2. An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore this measure indicates how uniform the transfer function step sizes are. The ideal step size is defined here as the step size for the device under test (i.e., (last transition level − first transition level) ÷ (2^n − 2)). Using this definition for DNL separates the effects of gain and offset error. A minimum DNL better than −1 LSB ensures no missing codes.
3. Zero error is defined as the difference in analog input voltage − between the ideal voltage and the actual voltage − that will switch the ADC output from code 0 to code 1. The ideal voltage level is determined by adding the voltage corresponding to 1/2 LSB to the bottom reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (256).

   Full-scale error is defined as the difference in analog input voltage – between the ideal voltage and the actual voltage – that will switch the ADC output from code 254 to code 255. The ideal voltage level is determined by subtracting the voltage corresponding to 1.5 LSB from the top reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (256).

ANALOG INPUT

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance			4		pF

REFERENCE INPUT (AV_{DD} = DV_{DD} = DRV_{DD} = 3.6 V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ref}	Reference input resistance			200		Ω
I_{ref}	Reference input current			5		mA

REFERENCE OUTPUTS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(REFTO)}$	Reference top offset voltage	Absolute min/max values valid and tested for AV_{DD} = 3.3 V	2.07	2 + [(AV_{DD} − 3) ÷ 2]	2.21	V
$V_{(REFBO)}$	Reference bottom offset voltage		1.09	1 + [(AV_{DD} − 3) ÷ 2]	1.21	V

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS WITH F_{CLK} = 80 MSPS AND USE OF EXTERNAL VOLTAGE REFERENCES (unless otherwise noted) (continued)

DYNAMIC PERFORMANCE†

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Effective number of bits, ENOB	f_{in} = 1 MHz	6.2	6.7		Bits
	f_{in} = 4.43 MHz	6.2	6.7		
	f_{in} = 15 MHz		6.4		
	f_{in} = 76 MHz		6.5		
Signal-to-total harmonic distortion + noise, S/(THD+N)	f_{in} = 1 MHz	39	42		dB
	f_{in} = 4.43 MHz	39	42		
	f_{in} = 15 MHz		40		
	f_{in} = 76 MHz		40		
Total harmonic distortion (THD)	f_{in} = 1 MHz	−46	−50		dB
	f_{in} = 4.43 MHz	−45.5	−49		
	f_{in} = 15 MHz		−44		
	f_{in} = 76 MHz		−45.5		
Spurious free dynamic range (SFDR)	f_{in} = 1 MHz	48	51		dB
	f_{in} = 4.43 MHz	48	51		
	f_{in} = 15 MHz		46		
	f_{in} = 76 MHz		48		
Analog input full-power bandwidth, BW	See Note 4		700		MHz
Differential phase, DP	f_{clk} = 40 MHz, f_{in} = 4.43 MHz, 20 IRE amplitude vs. full-scale of 140 IRE		0.8		°
Differential gain, DG			0.6		%

† Based on analog input voltage of −1 dBFS referenced to a 1.3 V_{pp} full-scale input range and using the external voltage references at f_{clk} = 80 MSPS with AV_{DD} = DV_{DD} = 3.3 V and DRV_{DD} = 3.0 V at 25°C.

4. The analog input bandwidth is defined as the maximum frequency of a −1 dBFS input sine that can be applied to the device for which an extra 3 dB attenuation is observed in the reconstructed output signal.

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS WITH F_{CLK} = 80 MSPS AND USE OF EXTERNAL VOLTAGE REFERENCES (unless otherwise noted) (continued)

TIMING REQUIREMENTS

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clk}	Maximum conversion rate			80			MHz
f_{clk}	Minimum conversion rate					10	kHz
$t_{d(o)}$	Output delay time (see Figure 1)	C_L = 10 pF,	See Notes 5 and 6		4.5	9	ns
$t_{h(o)}$	Output hold time	C_L = 2 pF,	See Note 5	2			ns
$t_{d(pipe)}$	Pipeline delay (latency)	See Note 6		4.5	4.5	4.5	CLK cycles
$t_{d(a)}$	Aperture delay time	See Note 5			3		ns
$t_{j(a)}$	Aperture jitter				1.5		ps, rms
t_{dis}	Disable time, $\overline{OE}$ rising to Hi-Z				5	8	ns
t_{en}	Enable, $\overline{OE}$ falling to valid data				5	8	ns

5. Output timing $t_{d(o)}$ is measured from the 1.5 V level of the CLK input falling edge to the 10%/90% level of the digital output. The digital output load is not higher than 10 pF.

   Output hold time $t_{h(o)}$ is measured from the 1.5 V level of the CLK input falling edge to the 10%/90% level of the digital output. The digital output is load is not less than 2 pF.

   Aperture delay $t_{d(A)}$ is measured from the 1.5 V level of the CLK input to the actual sampling instant.

   The OE signal is asynchronous.

   OE timing t_{dis} is measured from the $V_{IH(MIN)}$ level of OE to the high-impedance state of the output data. The digital output load is not higher than 10 pF.

   OE timing t_{en} is measured from the $V_{IL(MAX)}$ level of OE to the instant when the output data reaches $V_{OH(min)}$ or $V_{OL(max)}$ output levels. The digital output load is not higher than 10 pF.

6. The number of clock cycles between conversion initiation on an input sample and the corresponding output data being made available from the ADC pipeline. Once the data pipeline is full, new valid output data is provided on every clock cycle. In order to know when data is stable on the output pins, the output delay time $t_{d(o)}$ (i.e., the delay time through the digital output buffers) needs to be added to the pipeline latency. Note that since the max. $t_{d(o)}$ is more than 1/2 clock period at 80 MHz; data cannot be reliably clocked in on a rising edge of CLK at this speed. The falling edge should be used.

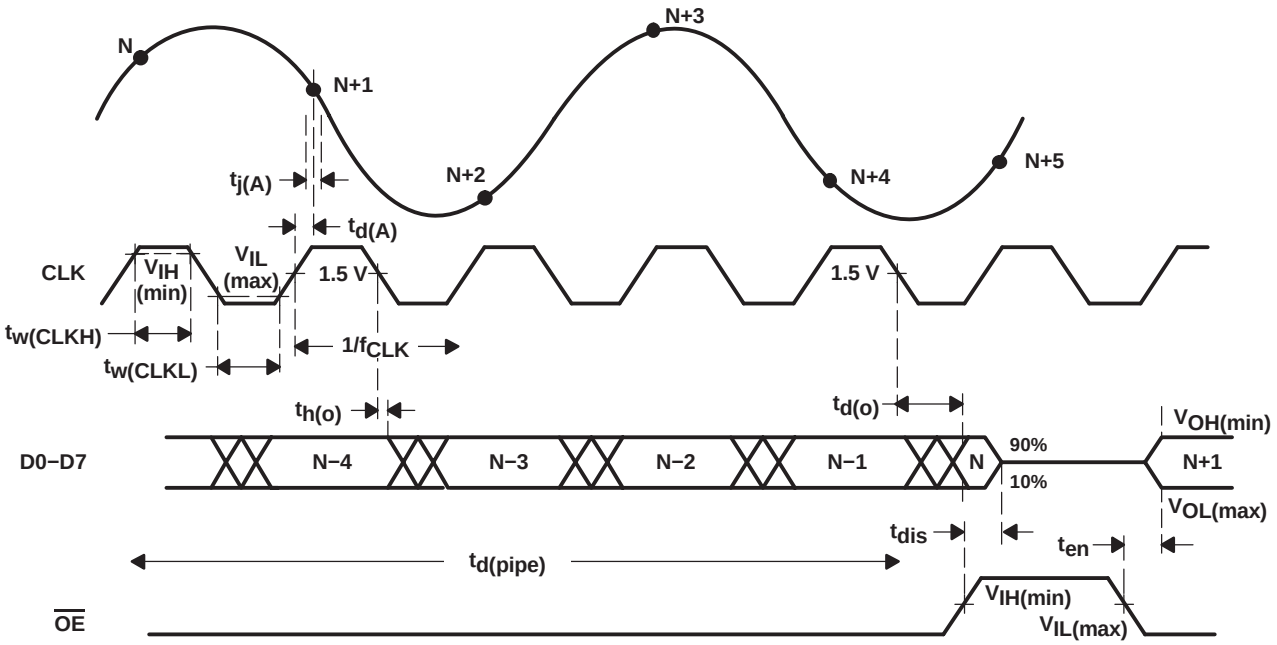


Figure 1. Timing Diagram

PERFORMANCE PLOTS AT 25°C

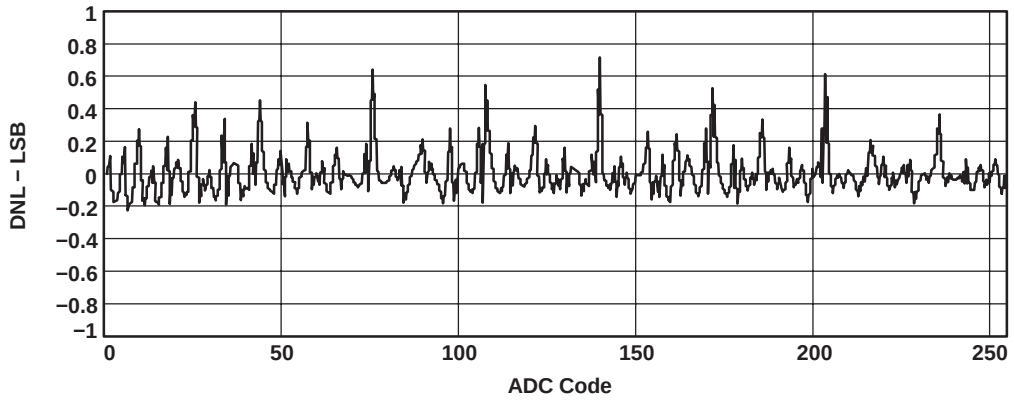


Figure 2. DNL vs Input Code At 80 MSPS (With External Reference, PW Package)

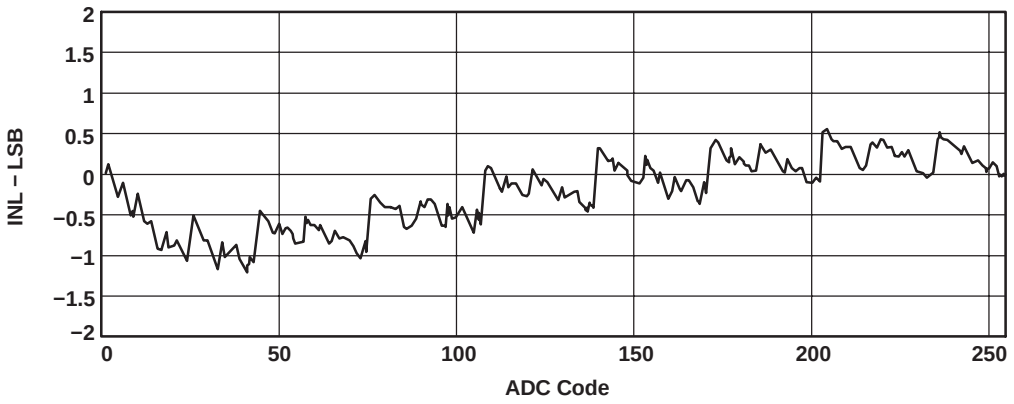


Figure 3. INL vs Input Code At 80 MSPS (With External Reference, PW Package)

PERFORMANCE PLOTS AT 25°C (Continued)

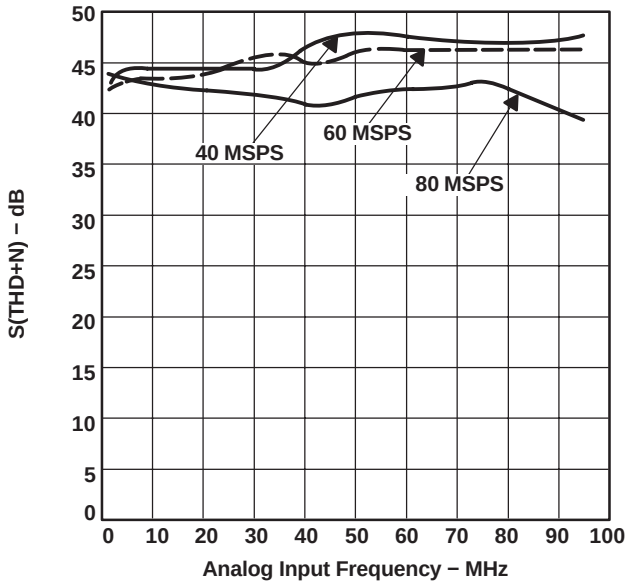


Figure 4. S/(THD+N) vs V_{IN} At 80 MSPS (Internal Reference), 60 MSPS (External Reference), 40 MSPS (External Reference)

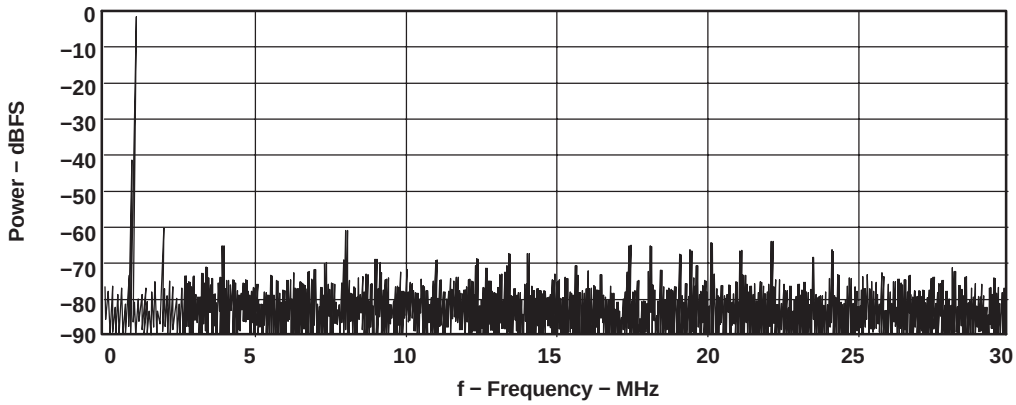


Figure 5. Spectral Plot f_{IN} = 1.011 MHz At 60 MSPS

PERFORMANCE PLOTS AT 25°C (Continued)

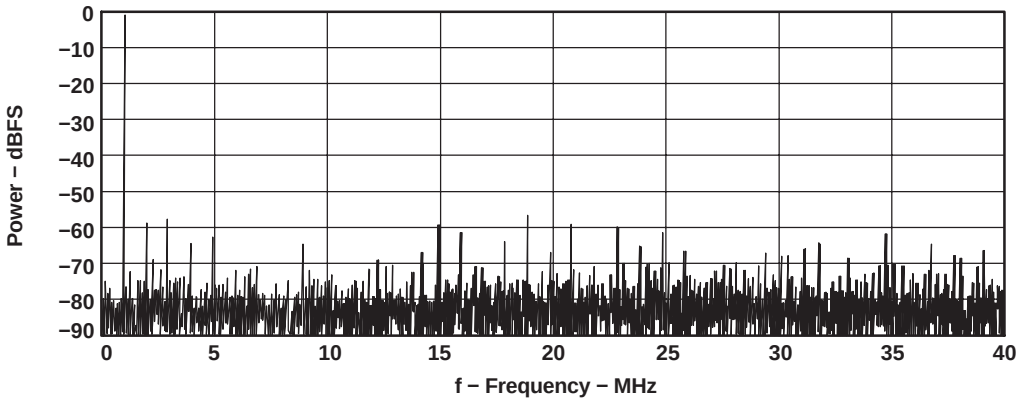


Figure 6. Spectral Plot f_{IN} = 0.996 MHz At 80MSPS

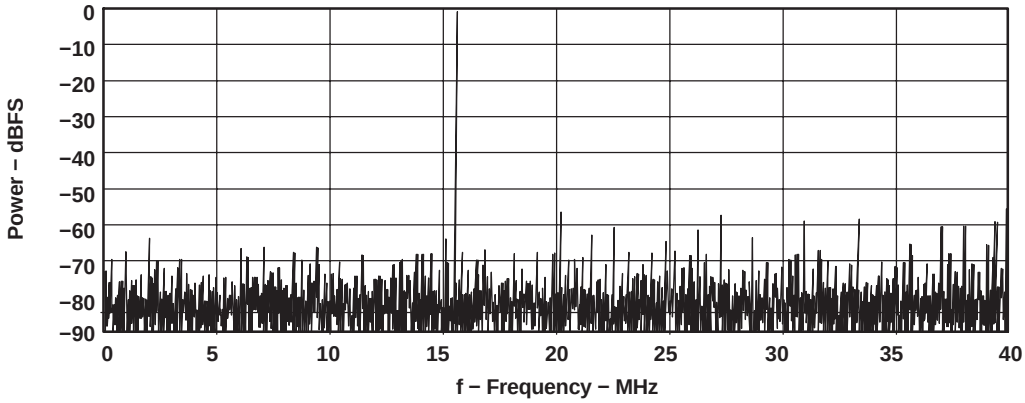


Figure 7. Spectral Plot f_{IN} = 15.527 MHz At 80 MSPS

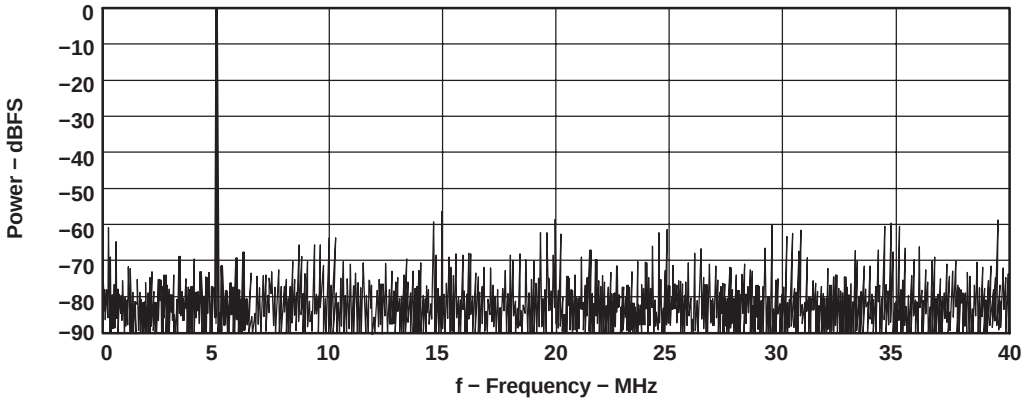


Figure 8. Spectral Plot f_{IN} = 75.02 MHz At 80MSPS
(Plot shows folded spectrum of undersampled input signal)

PERFORMANCE PLOTS AT 25°C (Continued)

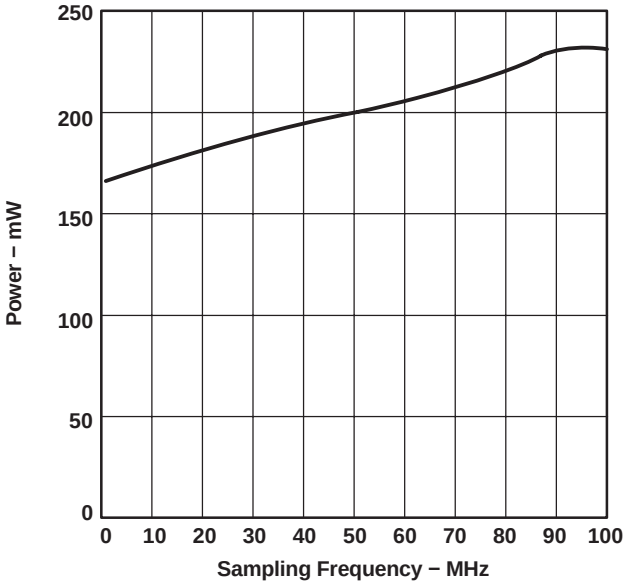


Figure 9. Power vs f_{CLK} At V_{IN} = 1 MHz, −1 dBFS

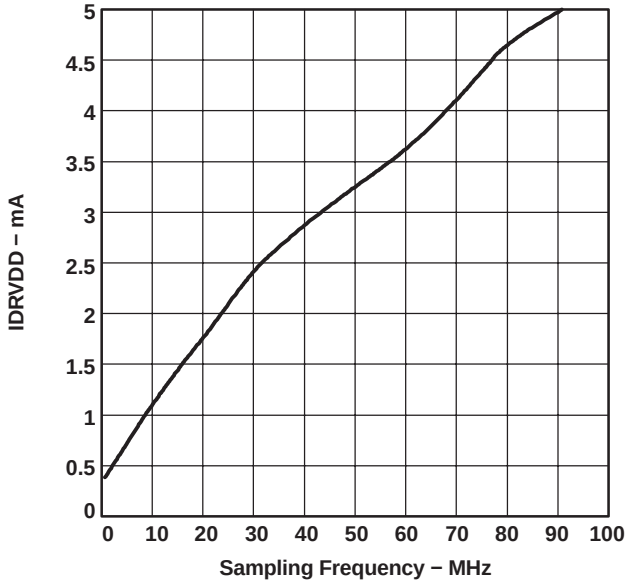


Figure 10. IDRVDD vs f_{CLK} At V_{IN} = 1 MHz, −1 dBFS

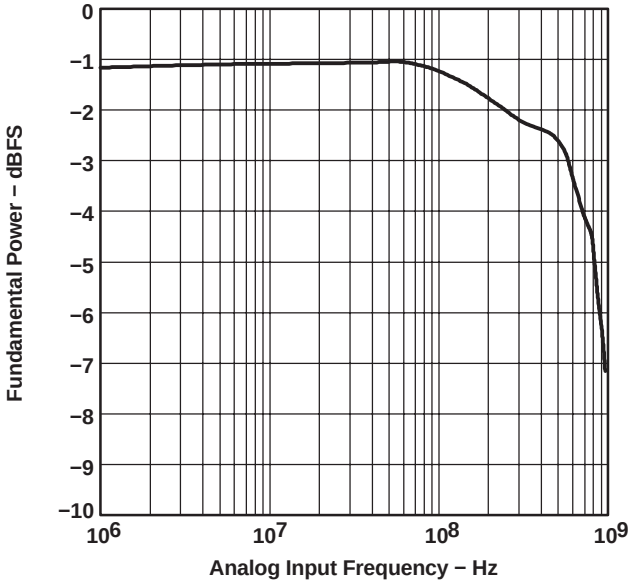


Figure 11. ADC Output Power With Respect To −1 dBFS V_{IN} (Internal Reference, DW Package)

PRINCIPLE OF OPERATION

The TLV5580 implements a high-speed 80 MSPS converter in a cost-effective CMOS process. Powered from 3.3 V, the single-pipeline design architecture ensures low-power operation and 8 bit accuracy. Signal input and clock signals are all single-ended. The digital inputs are 3.3 V TTL/CMOS compatible. Internal voltage references are included for both bottom and top voltages. Therefore the converter forms a self-contained solution. Alternatively the user may apply externally generated reference voltages. In doing so, both input offset and input range can be modified to suit the application.

A high-speed sampling-and-hold captures the analog input signal. Multiple stages will generate the output code with a pipeline delay of 4.5 CLK cycles. Correction logic combines the multistage data and aligns the 8-bit output word. All digital logic operates at the rising edge of CLK.

ANALOG INPUT

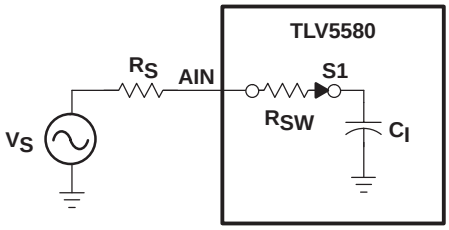


Figure 12. Simplified Equivalent Input Circuit

A first-order approximation for the equivalent analog input circuit of the TLV5580 is shown in Figure 12. The equivalent input capacitance C_I is 4 pF typical. The input must charge/discharge this capacitance within the sample period of one half clock cycle. When a full-scale voltage step is applied, the input source provides the charging current through the switch resistance R_{SW} (200 Ω) of S1 and quickly settles. In this case the input impedance is low. Alternatively, when the source voltage equals the value previously stored on C_I, the hold capacitor requires no input current and the equivalent input impedance is very high.

To maintain the frequency performance outlined in the specifications, the total source impedance should be limited to about 80 Ω, as follows from the equation with f_{CLK} = 80 MHz, C_I = 4 pF, R_{SW} = 200 Ω:

$$R_S < \left[1 \div \left(2f_{CLK} \times C_I \times \ln(256)\right) - R_{SW}\right]$$

So, for applications running at a lower f_{CLK}, the total source resistance can increase proportionally.

PRINCIPLE OF OPERATION

DC COUPLED INPUT

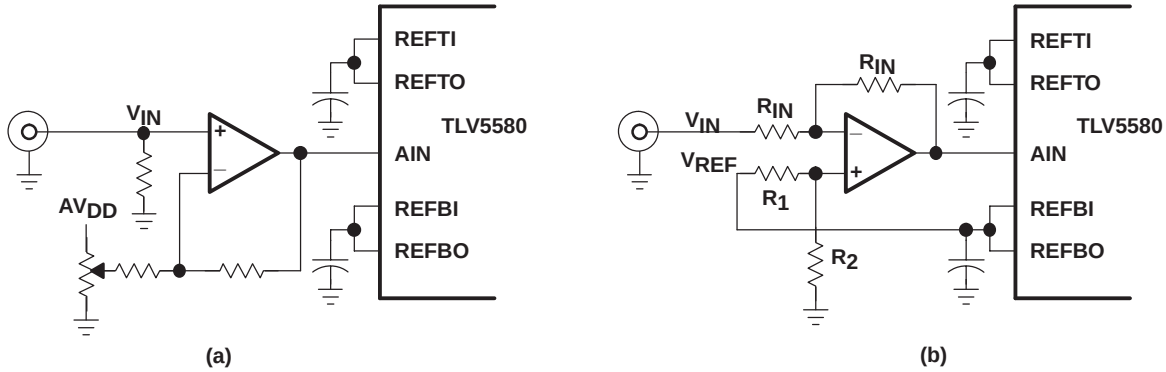


Figure 13. DC-Coupled Input Circuit

For dc-coupled systems an op amp can level-shift a ground-referenced input signal. A circuit as shown in Figure 13(a) is acceptable. Alternatively, the user might want a bipolar shift together with the bottom reference voltage as seen in Figure 13(b). In this case the AIN voltage is given by:

$$AIN = 2 \times R_2 \div \left(R_1 + R_2\right) \times V_{REF} - V_{IN}$$

AC COUPLED INPUT

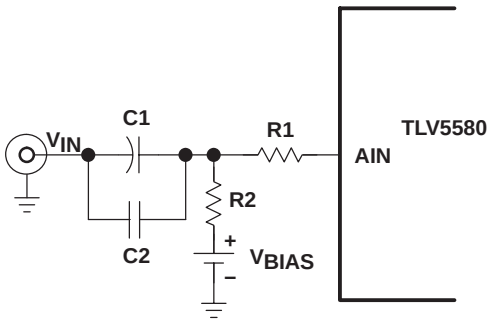


Figure 14. AC-Coupled Input Circuit

For many applications, especially in single supply operation, ac coupling offers a convenient way for biasing the analog input signal at the proper signal range. Figure 14 shows a typical configuration. To maintain the outlined specifications, the component values need to be carefully selected. The most important issue is the positioning of the 3 dB high-pass corner point $f_{-3\ dB}$, which is a function of R_2 and the parallel combination of C_1 and C_2, called C_{eq}. This is given by the following equation:

$$f_{-3\ dB} = 1 \div \left(2\pi \times R_2 \times C_{eq}\right)$$

where C_{eq} is the parallel combination of C_1 and C_2.

Since C1 is typically a large electrolytic or tantalum capacitor, the impedance becomes inductive at higher frequencies. Adding a small ceramic or polystyrene capacitor, C2 of approximately 0.01 μF, which is not inductive within the frequency range of interest, maintains low impedance. If the minimum expected input signal frequency is 20 kHz, and R2 equals 1 kΩ and R1 equals 50 Ω, the parallel capacitance of C1 and C2 must be a minimum of 8 nF to avoid attenuating signals close to 20 kHz.

PRINCIPLE OF OPERATION

REFERENCE TERMINALS

The voltages on terminals REFBI and REFTI determine the TLV5580's input range. Since the device has an internal voltage reference generator with outputs available on REFBO respectively REFTO, corresponding terminals can be directly connected externally to provide a contained ADC solution. Especially at higher sampling rates, it is advantageous to have a wider analog input range. The wider analog input range is achievable by using external voltage references (e.g., at AVDD = 3.3 V, the full scale range can be extended from 1 Vpp (internal reference) to 1.3 Vpp (external reference) as shown in Table 1). These voltages should not be derived via a voltage divider from a power supply source. Instead, use a bandgap-derived voltage reference to derive both references via an op amp circuit. Refer to the schematic of the TLV5580 evaluation module for an example circuit.

When using external references, the full-scale ADC input range and its dc position can be adjusted. The full-scale ADC range is always equal to $V_{REFT} - V_{REFB}$. The maximum full-scale range is dependent on AV_{DD} as shown in the specification section. In addition to the limitation on their difference, V_{REFT} and V_{REFB} each also have limits on their useful range. These limits are also dependent on AV_{DD}.
Table 3 summarizes these limits for 3 cases.

Table 1. Recommended Operating Modes

AV_{DD}	$V_{REFB(min)}$	$V_{REFB(max)}$	$V_{REFT(min)}$	$V_{REFT(max)}$	$[V_{REFT}-V_{REFB}]_{max}$
3 V	0.8 V	1.2 V	1.8 V	2.2 V	1 V
3.3 V	0.8 V	1.2 V	2.1 V	2.5 V	1.3 V
3.6 V	0.8 V	1.2 V	2.4 V	2.8 V	1.6 V

DIGITAL INPUTS

The digital inputs are CLK, STDBY, PWDN_REF, and $\overline{OE}$. All these signals, except CLK, have an internal pull-down resistor to connect to digital ground. This provides a default active operation mode using internal references when left unconnected.

The CLK signal at high frequencies should be considered as an analog input. Overshoot/undershoot should be minimized by proper termination of the signal close to the TLV5580. An important cause of performance degradation for a high-speed ADC is clock jitter. Clock jitter causes uncertainty in the sampling instant of the ADC, in addition to the inherent uncertainty on the sampling instant caused by the part itself, as specified by its aperture jitter. There is a theoretical relationship between the frequency (f) and resolution (2^N) of a signal that needs to be sampled and the maximum amount of aperture error dt_{max} that is tolerable. The following formula shows the relation:

$$dt_{max} = 1 \div \left[\pi \, f \, 2^{(N+1)}\right]$$

As an example, for an 8−bit converter with a 15-MHz input, the jitter needs to be kept <41 pF in order not to have changes in the LSB of the ADC output due to the total aperture error.

PRINCIPLE OF OPERATION

DIGITAL OUTPUTS

The output of TLV5580 is a standard binary code. Capacitive loading on the output should be kept as low as possible (a maximum loading of 10 pF is recommended) to provide best performance. Higher output loading causes higher dynamic output currents and can increase noise coupling into the device's analog front end. To drive higher loads, use an output buffer is recommended.

When clocking output data from TLV5580, it is important to observe its timing relation to CLK. Pipeline ADC delay is 4.5 clock cycles to which the maximum output propagation delay is added. See Note 6 in the specification section for more details.

LAYOUT, DECOUPLING AND GROUNDING RULES

It is necessary for any PCB using the TLV5580 to have proper grounding and layout to achieve the stated performance. Separate analog and digital ground planes that are spliced underneath the device are advisable. TLV5580 has digital and analog terminals on opposite sides of the package to make proper grounding easier. Since there is no internal connection between analog and digital grounds, they have to be joined on the PCB. Joining the digital and analog grounds at a point in close proximity to the TLV5580 is advised.

As for power supplies, separate analog and digital supply terminals are provided on the device (AV_{DD}/DV_{DD}). The supply to the digital output drivers is kept separate also (DRV_{DD}). Lowering the voltage on this supply from the nominal 3.3 V to 3 V improves performance because of the lower switching noise caused by the output buffers.

Due to the high sampling rate and switched-capacitor architecture, TLV5580 generates transients on the supply and reference lines. Proper decoupling of these lines is essential. Decoupling as shown in the schematic of the TLV5580 EVM is recommended.

TLV5580 EVALUATION MODULE

TLV5580 EVALUATION MODULE

TI provides an evaluation module (EVM) for TLV5580. The EVM also includes a 10-bit 80 MSPS DAC so that the user can convert the digitized signal back to the analog domain for functional testing. Performance measurements can be done by capturing the ADC's output data.

The EVM provides the following additional features:

- Provision of footprint for the connection of an onboard crystal oscillator, instead of using an external clock input.
- Use of TLV5580 internal or external voltage references. In the case of external references, an onboard circuit is used that derives adjustable bottom and top reference voltages from a bandgap reference. Two potentiometers allow for the independent adjustments of both references. The full scale ADC range can be adjusted to the input signal amplitude.
- All digital output, control signal I/O (output enable, standby, reference power-down) and clock I/O are provided on a single connector. The EVM can thus be part of a larger (DSP) system for prototyping.
- Onboard prototyping area with analog and digital supply and ground connections.

Figure 15 shows the EVM schematic.

The EVM is factory shipped for use in the following configuration:

- Use of external (onboard) voltage references
- External clock input

ANALOG INPUT

A signal in the range between $V_{(REFBI)}$ and $V_{(REFTI)}$ should be applied to avoid overflow/underflow on connector J10. This signal is onboard terminated with 50Ω. There is no onboard biasing of the signal. When using external (onboard) references, these levels can be adjusted with R7 ($V_{(REFTI)}$) and R6 ($V_{(REFBI)}$). Adjusting R7 causes both references to shift. R6 only impacts the bottom reference. The range of these signals for which the device is specified depends on AV_{DD} and is shown under the Recommended Operating Conditions.

Internally generated reference levels are also dependent on AV_{DD} as shown in the electrical characteristics section.

CLOCK INPUT

A clock signal should be applied with amplitudes ranging from 0 to AV_{DD} with a frequency equal to the desired sampling frequency on connector J9. This signal is onboard terminated with 50 Ω. Both ADC and DAC run off the same clock signal. Alternatively the clock can be applied from terminal 1 on connector J11. A third option is using a crystal oscillator. The EVM board provides the footprint for a crystal oscillator that can be populated by the end-user, depending on the desired frequency. The footprint is compatible with the Epson EG-8002DC series of programmable high-frequency crystal oscillators. Refer to the TLV5580 EVM Settings for selecting between the different clock modes.

TLV5580 EVALUATION MODULE

POWER SUPPLIES

The board provides seven power supply connectors (see Table 2). For optimum performance, analog and digital supplies should be kept separate. Using separate supplies for the digital logic portion of TLV5580 (DV_{DD}) and its output drivers (DRV_{DD}) benefits dynamic performance, especially when DRV_{DD} is put at the minimum required voltage (3 V), while DV_{DD} might be higher (up to 3.6 V). This lowers the switching noise on the die caused by the output drivers.

Table 2. Power Supplies

SIGNAL NAME	CONNECTOR	BOARD LABEL	DESCRIPTION
DRV3	J1	3DRV	3.3 V digital supply for TLV5580 (digital output drivers)
DV3	J2	3VD	3.3 V digital supply for TLV5580 (digital logic) and peripherals
DV5	J3	5VD	5 V digital supply for D/A converter and peripherals
AV3	J4	3VA	3.3 V analog supply for TLV5580
AV5	J5	5VA	5 V analog supply for onboard reference circuit and D/A converter. Can be left unconnected if internal references are used and no D/A conversion is required.
AV+12	J6	12VA	12 V analog supply for onboard reference circuit. Can be left unconnected if internal references are used.
AV−12	J7	−12VA	−12 V analog supply for onboard reference circuit. Can be left unconnected if internal references are used.

VOLTAGE REFERENCES

SW1 and SW2 switch between internal and external top and bottom references respectively. The external references are onboard generated from a stable bandgap-derived 3.3 V signal (using TI's TPS7133 and quad-op amp TLE2144). They can be adjusted via potentiometers R6 ($V_{(REFBI)}$) and R7 ($V_{(REFTI)}$). It is advised to power down the internal voltage references by asserting PWN_REF when onboard references are used.

The references are measured at test points TP3 ($V_{(REFB)}$) and TP4 ($V_{(REFT)}$).

DAC OUTPUT

The onboard DAC is a 10-bit 80 MSPS converter. It is connected back-to-back to the TLV5580. While the user could use its analog output for measurements, the DAC output is directly connected to connector J8 and does not pass through an analog reconstruction filter. So mirror spectra from aliased signal components feed through into the analog output.

For this reason and to separate ADC and DAC contributions, performance measurements should be made by capturing the ADC output data available on connector J11 and not by evaluating the DAC output.

TLV5580 EVALUATION MODULE

TLV5580 EVM SETTINGS

CLOCK INPUT SETTINGS

REFERENCE DESIGNATOR	FUNCTION
W1	Clock selection switch 1−2 J11: clock from pin1 on J11 connector 2−3 J9: clock from J9 SMA connector
W2	Clock source switch ■ XTL: clock from onboard crystal oscillator □ CLK: clock from pin 1 on J11 connector (if W1/1−2) or J9 SMA connector (if W1/2−3) NOTE: If set to XTL and a XTL oscillator is populated, no clock signal should be applied to J9 or J11, depending on the W1 setting.
W3	Clock output switch 1−2 Rising: clock output on J11 connector is the same phase as the clock to the digital output buffer. Data changes on rising CLK edge. 2−3 Falling: clock output on J11 connector is the opposite phase as the digital output buffer. Data changes on falling CLK edge.

REFERENCE SETTINGS

REFERENCE DESIGNATOR	FUNCTION
SW1	REFT external/internal switch ■□ REFT internal: REFT from TLV5580 internal reference □■ REFT external: REFT from onboard voltage reference circuit
SW2	REFB external/internal switch ■□ REFB internal: REFB from TLV5580 internal reference □■ REFB external: REFB from onboard voltage reference circuit

CONTROL SETTINGS

REFERENCE DESIGNATOR	FUNCTION
W4	TLV5580 and digital output buffer output enable control (1) ■ 5580-574 $\overline{OE}$-connected: Connects $\overline{OE}$s of TLV5580 and digital output buffer (574 buffer). Use this when no board-external $\overline{OE}$ is used. In addition, close W5 to have both $\overline{OE}$s permanently enabled. □ 5580-574 $\overline{OE}$-disconnected: Disconnects $\overline{OE}$s of TLV5580 and digital output buffer (574 buffer). The $\overline{OE}$ for the output buffer needs to be pulled low from pin 5 on J11 connector to enable. The $\overline{OE}$ for TLV5580 is independently controlled from pin 7 on J11 connector (W5 open) or is permanently enabled if W5 is closed.
W5	TLV5580 and digital output buffer output enable control (2) ■ 5580 $\overline{OE}$ to GND: Connects $\overline{OE}$s of TLV5580 to GND. Additionally connects $\overline{OE}$ of 74ALS574 to GND if W4 is 5580-574 $\overline{OE}$-connected. □ 5580 $\overline{OE}$ external: Enables control of $\overline{OE}$ of TLV5580 via pin 7 on J11 connector. When taken high (internal pulldown) the output can be disabled.
W6	TLV5580 STDBY control ■ Stdby: STDBY is active (high). □ Active: STDBY is low, via internal pulldown. STDBY can be taken high from pin 9 on J11 connector to enable standby mode.

TLV5580 EVALUATION MODULE

CONTROL SETTINGS (Continued)

REFERENCE DESIGNATOR	FUNCTION
W7	TLV5580 PWDN REF control ■ Pwdn_ref: PWDN_REF is active (high). □ Active: PWDN_REF is low, via internal pulldown. PWDN_REF can be taken high from pin 10 on J11 connector to enable pwdn_ref mode.
W8	DAC enable ■ Active: D/A on □ Standby: D/A off

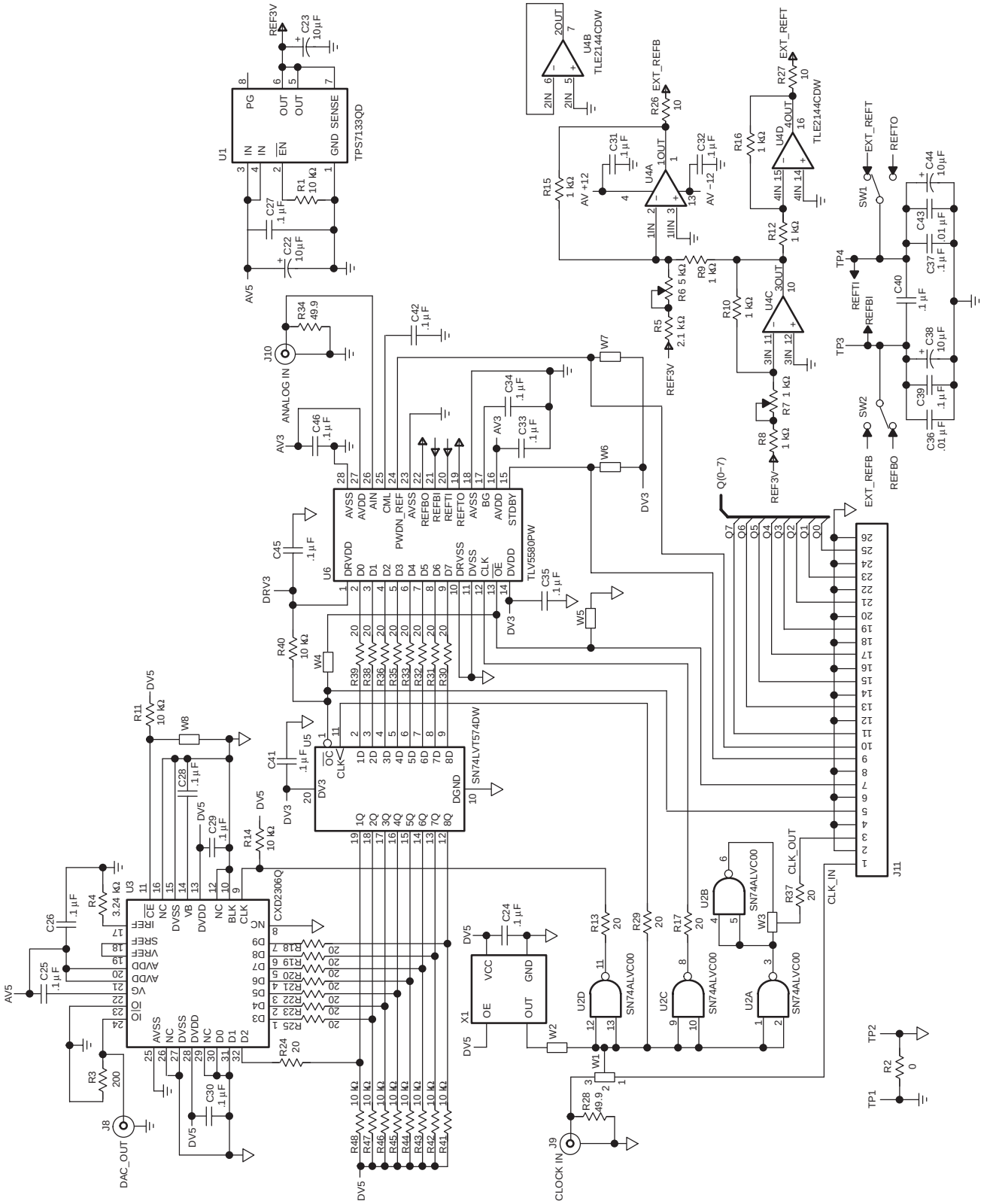


Figure 15. EVM Schematic

TLV5580 EVALUATION MODULE

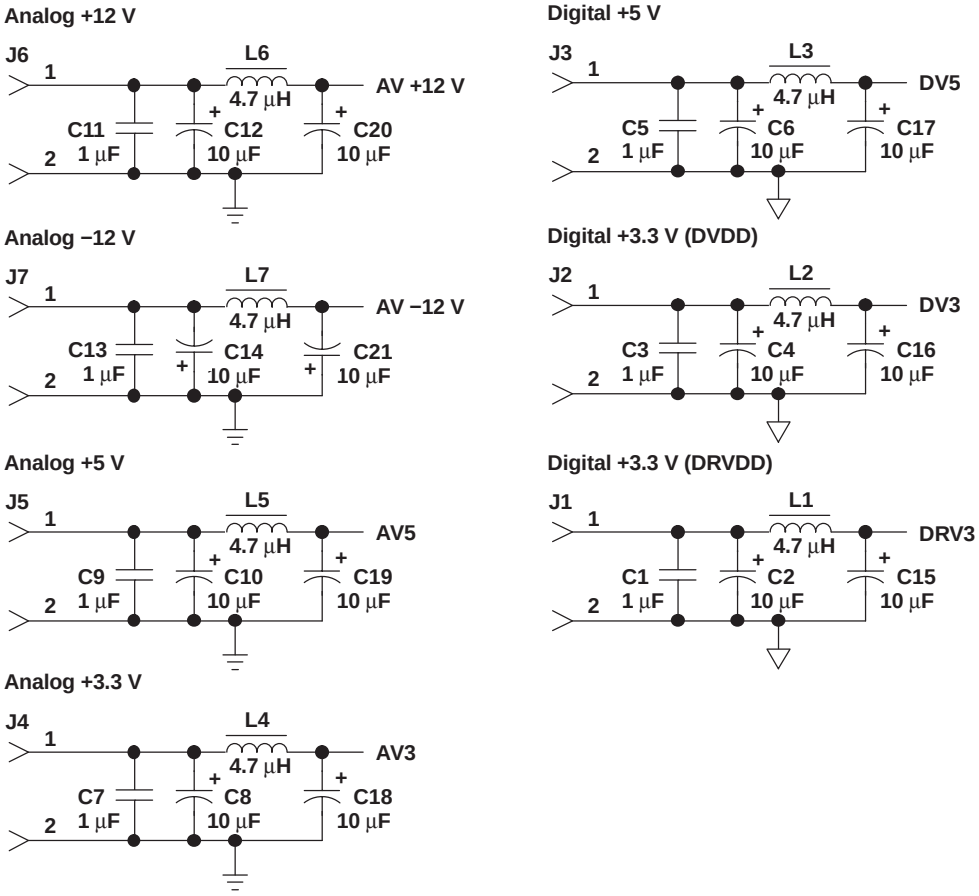
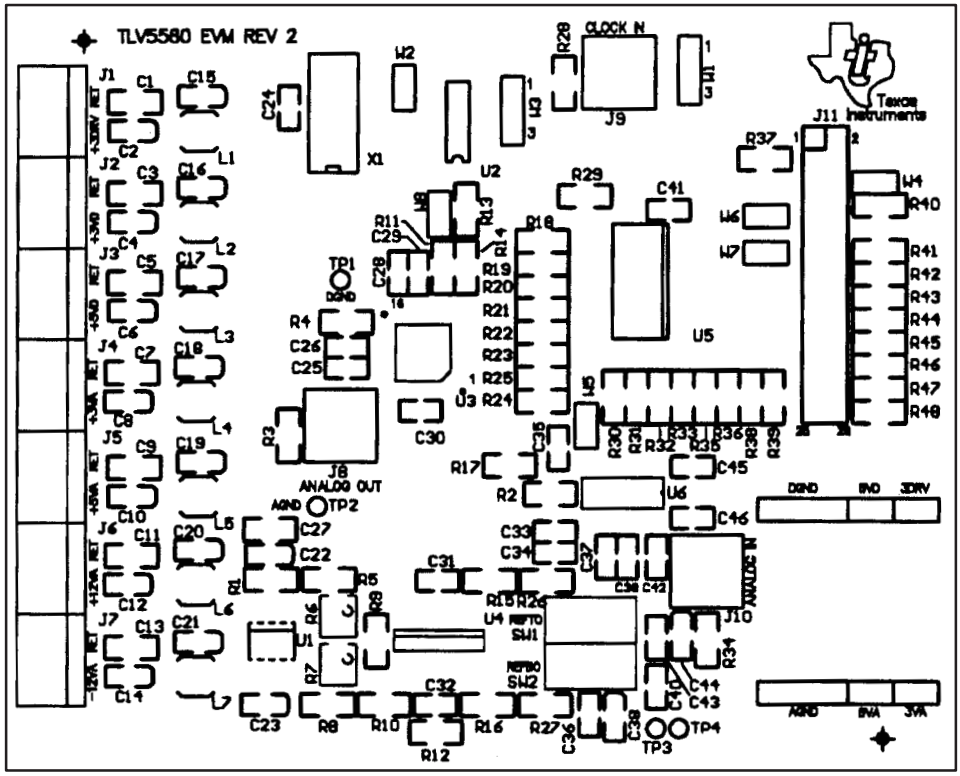


Figure 15. EVM Schematic (Continued)

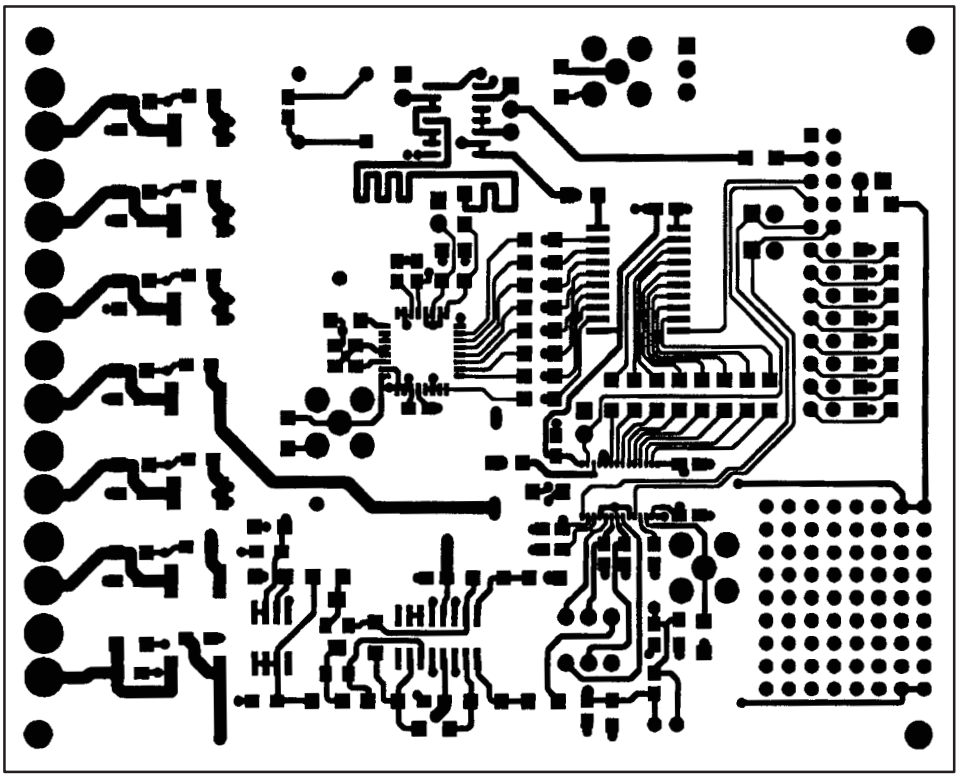
TLV5580 EVALUATION MODULE



Top Overlay

Figure 15. EVM Schematic (Continued)

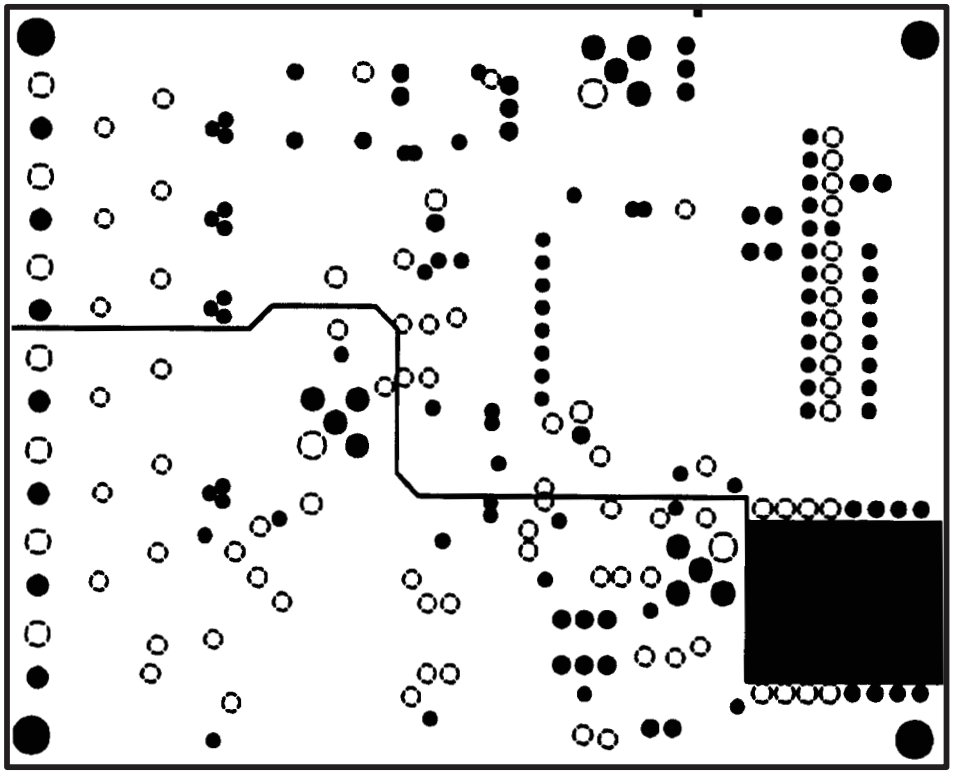
TLV5580 EVALUATION MODULE



Top Layer

Figure 15. EVM Schematic (Continued)

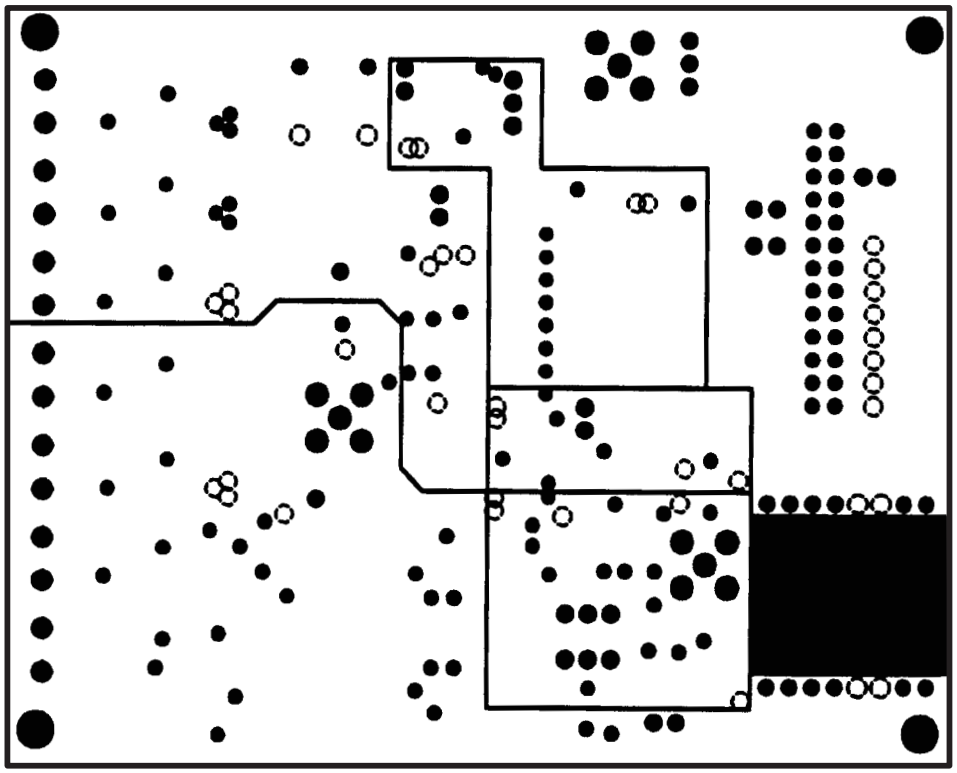
TLV5580 EVALUATION MODULE



Internal Plane 1

Figure 15. EVM Schematic (Continued)

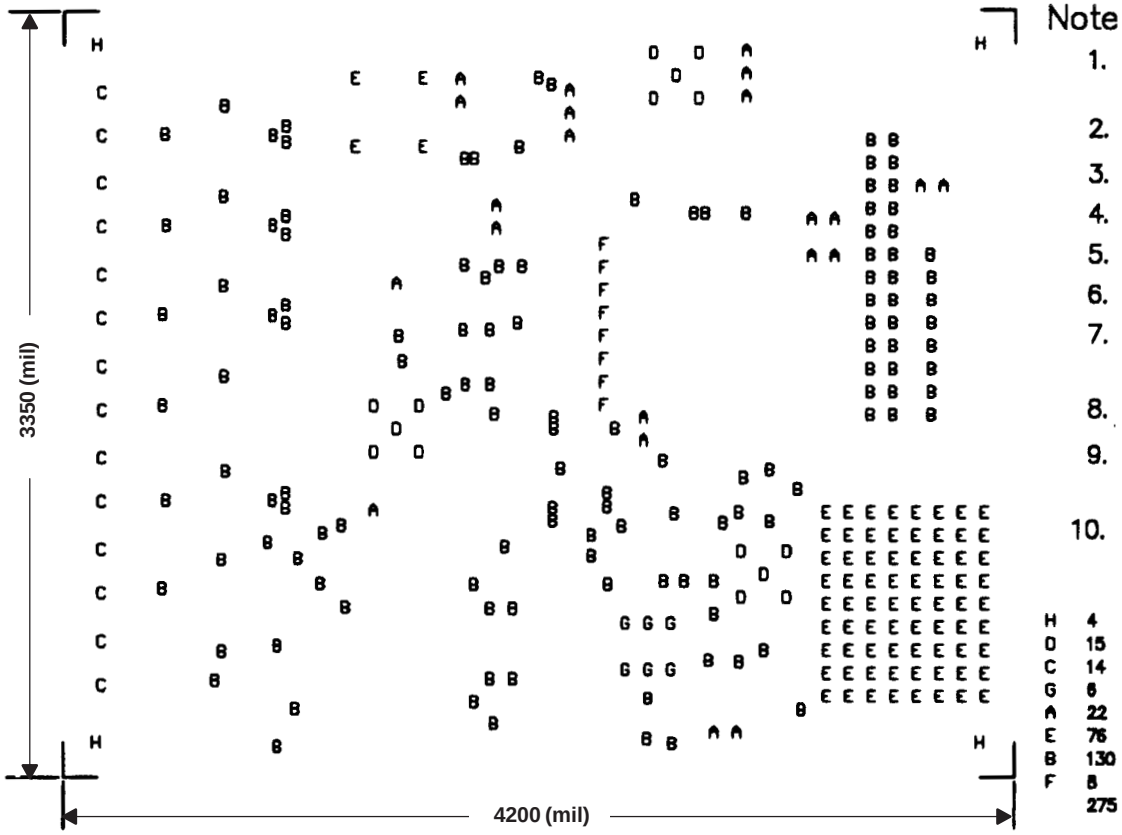
TLV5580 EVALUATION MODULE



Internal Plane 2

Figure 15. EVM Schematic (Continued)

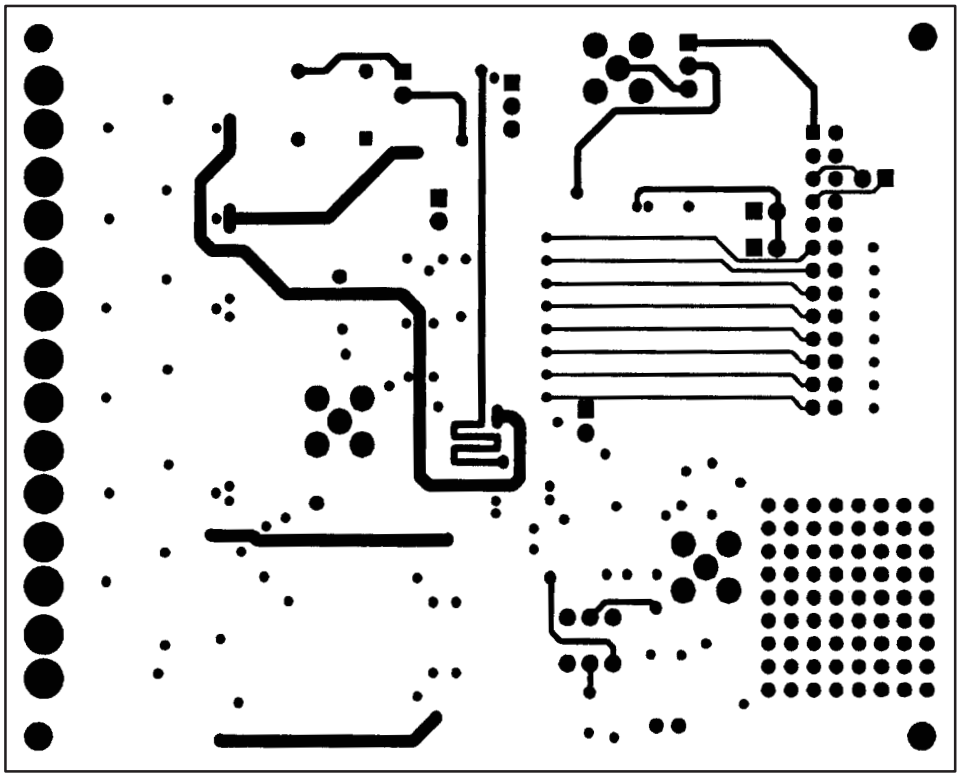
TLV5580 EVALUATION MODULE



Drill Drawing for Through Hole

Figure 15. EVM Schematic (Continued)

TLV5580 EVALUATION MODULE



Bottom Layer

Figure 15. EVM Schematic (Continued)

TLV5580 EVALUATION MODULE

Table 3. TLV5580EVM Bill of Material

QTY.	REFERENCE DESIGNATOR	VALUE	SIZE	DESCRIPTION	MANUFACTURER/ PART NUMBER†
7	C1, C11, C13, C3, C5, C7, C9	1 μF	1206	ceramic multi-layer capacitor	Any
18	C10, C12, C14, C15, C16, C17, C18, C19, C2, C20, C21, C22, C23, C4, C6, C8, C38, C44	10 μF	3216	16 V, 10 μF, tantalum capacitor	Any
2	C36, C43	0.01 μF	805	Ceramic multi-layer	Any
19	C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C37, C39, C40, C41, C42, C45, C46	0.1 μF	805	Ceramic multi-layer capacitor	Any
7	J1, J2, J3, J4, J5, J6, J7	Screw Con		2 terminal screw connector	Lumberg KRMZ2
3	J10, J8, J9	SMA		PCM mount, SMA Jack	Johnson Components 142-0701-206
1	J11	IDC26		13″ × 2.025″ square pin header	Samtec TSW-113-07-L-D
7	L1, L2, L3, L4, L5, L6, L7	4.7 μH		4.7 μH DO1608C-472-Coil Craft	Coil Craft DO1608-472
1	R2	0	1206	Chip resistor	Any
2	R26, R27	10	1206	Chip resistor	Any
12	R1, R11, R14, R40, R41, R42, R43, R44, R45, R46, R47, R48	10 K	1206	Chip resistor	Any
6	R10, R12, R15, R16, R8, R9	1 K	1206	Chip resistor	Any
1	R5	2.1 K	1206	Chip resistor	Any
20	R13, R17, R18, R19, R20, R21, R22, R23, R24, R25, R29, R30, R31, R32, R33, R35, R36, R37, R38, R39	20	1206	Chip resistor	Any
1	R3	200	1206	Chip resistor	Any
1	R4	3.24 K	1206	Chip resistor	Any
2	R28, R34	49.9	1206	Chip resistor	Any
1	R6	5 K		4 mm SM pot-top adjust	Bourns 3214W-5K
1	R7	1 K		4 mm SM pot-top adjust	Bourns 3214W-1K
2	SW1, SW2	SPDT		C&K tiny series−slide switch	C&K TS01CLE
4	TP1, TP2, TP3, TP4	TP		Test point, single 0.025″ pin	Samtec TSW-101-07-L-S or equivalent
1	U3	CXD2306Q			Sony CXD2306Q
1	U2	SN74ALVC00D	14-SOIC (D)	Quad 2-input positive NAND	Texas Instruments SN74ALVC00D
1	U5	SN74LVT574DW	20-SOP (DW)		Texas Instruments SN74LVT574DW

† Manufacturer and part number data for reference only. Equivalent parts might be substituted on the EVM.

TLV5580 EVALUATION MODULE

Table 3. TLV5580EVM Bill of Material (Continued)

QTY.	REFERENCE DESIGNATOR	VALUE	SIZE	DESCRIPTION	MANUFACTURER/ PART NUMBER†
1	U4	TLE2144CDW	16-SOP(D)	Quad op amp	Texas Instruments TLE2144CDW/ TLE2144IDW
1	U6	TLV5580PW	28-TSSOP (PW)		Texas Instruments TLV5580PW
1	U1	TPS7133	8-SOP(D)	Low-dropout voltage regulator	Texas Instruments TPS7133QD
6	W2, W4, W5, W6, W7, W8	SPST		2 position jumper, 0.1″ spacing	Samtec TSW-102-07-L-S or equivalent
2	W1, W3	DPFT		3 position jumper, 0.1″ spacing	Samtec TSW-103-07-L-S or equivalent
1	X1	NA		Crystal oscillator	Epson SG-8002DC series

† Manufacturer and part number data for reference only. Equivalent parts might be substituted on the EVM.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV5580CDW	NRND	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5580C	
TLV5580CPW	NRND	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5580	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

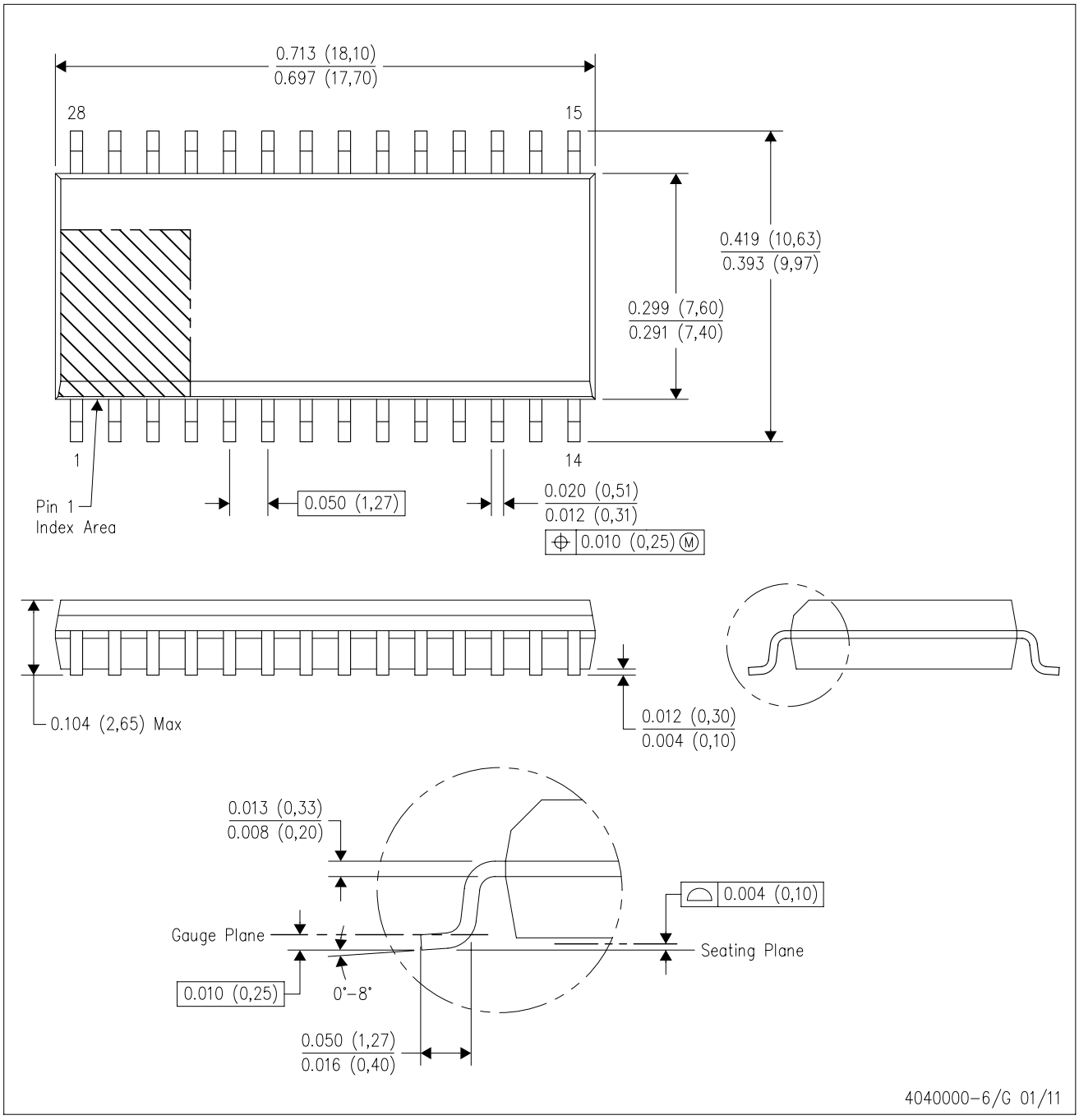
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

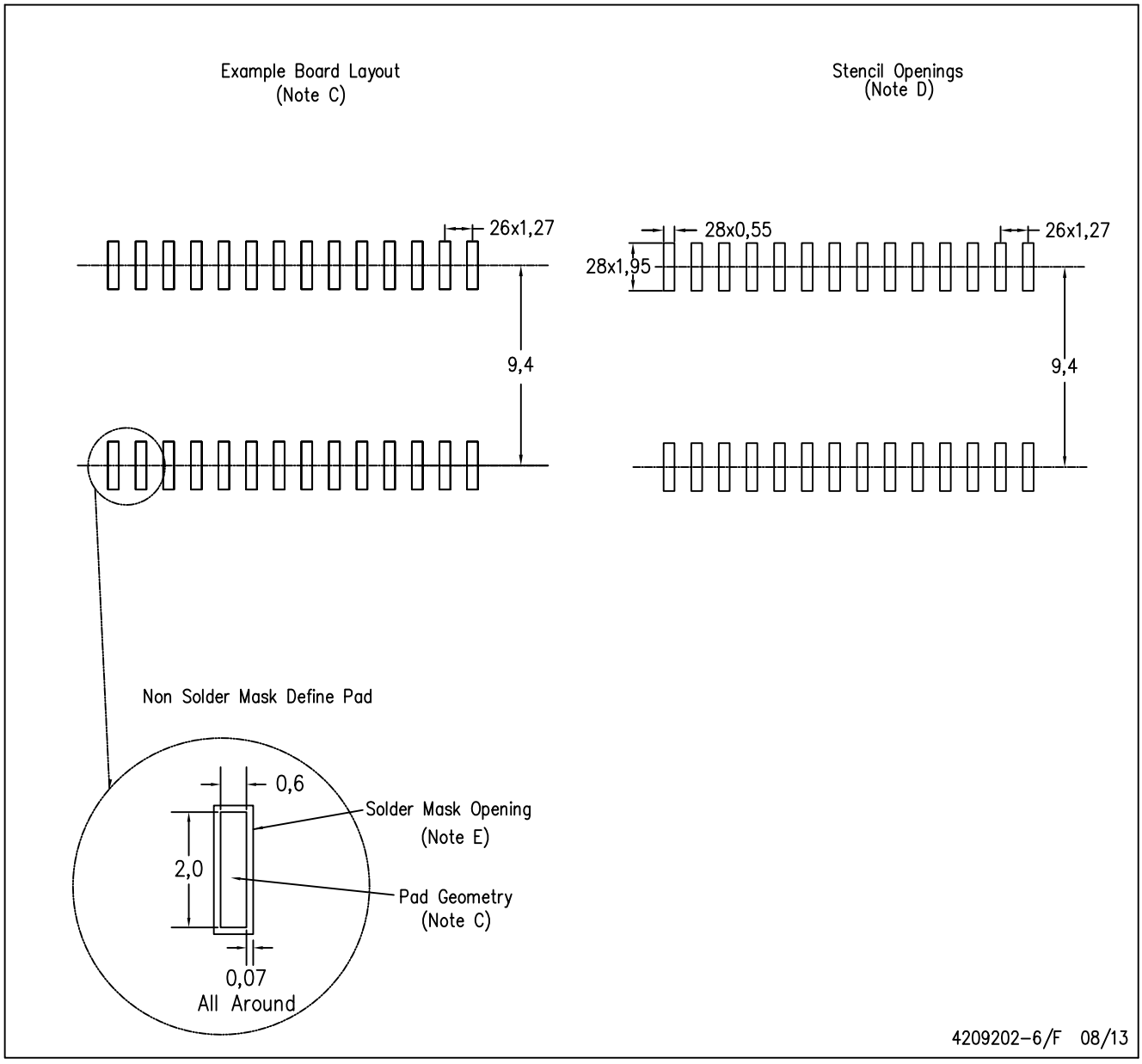
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



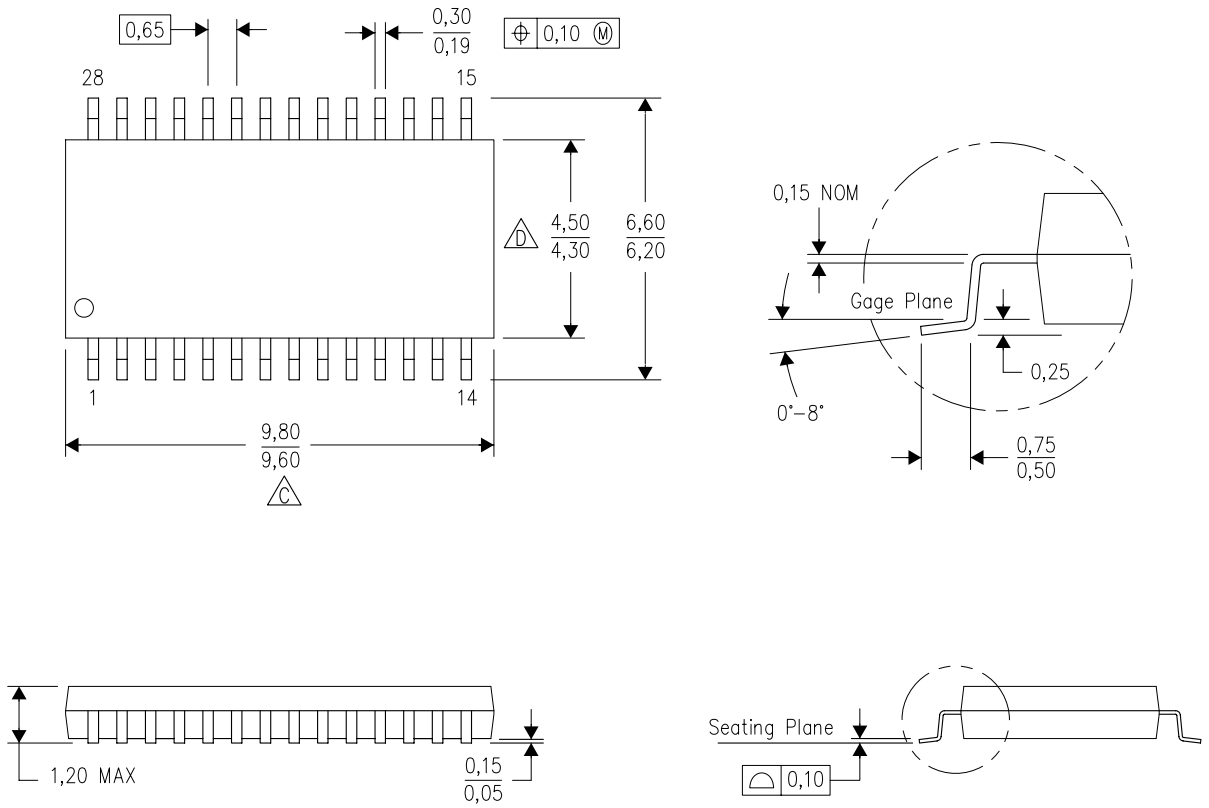
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

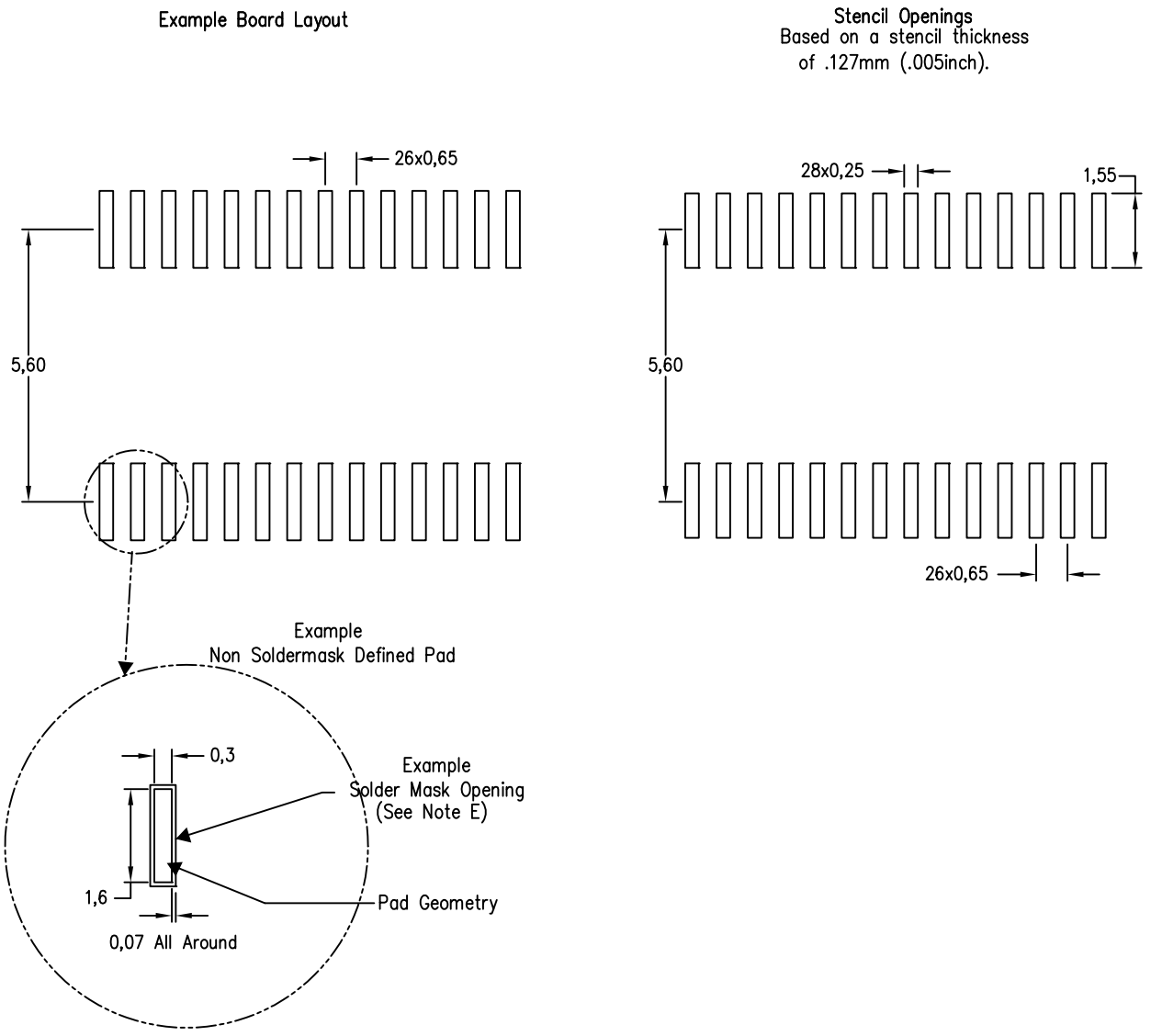
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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