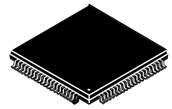


3-TO-1 DVI/HDMI SWITCH

FEATURES

- **Designed for Signaling Rates up to 1.65 Gbps in Support of UXGA Display**
- **Differential Interface Compatible with Transition Minimized Differential Signaling (TMDS) Electrical Specification**
- **Each Port Supports HDMI or DVI Inputs**
- **Isolated Digital Display Control (DDC) Bus for Unused Ports**
- **5-V Tolerance to all DDC and HPD_SINK Inputs**
- **Integrated Receiver Termination**
- **Inter-Pair Output Skew < 100 ps**
- **8-dB Receiver Equalization to Compensate for 5-m DVI Cable Losses**
- **High Impedance Outputs When Disabled**
- **HBM ESD Protection Exceeds 3 kV**
- **3.3-V Supply Operation**
- **80-Pin TQFP Package**
- **ROHS Compatible and 260°C Reflow Rated**

APPLICATIONS

- **Switching From Three Digital-Video (DVI) or Digital-Audio Visual (HDMI) Sources**
- **Digital TV**
- **Digital Projector**
- **Audio Video Receiver**

DESCRIPTION

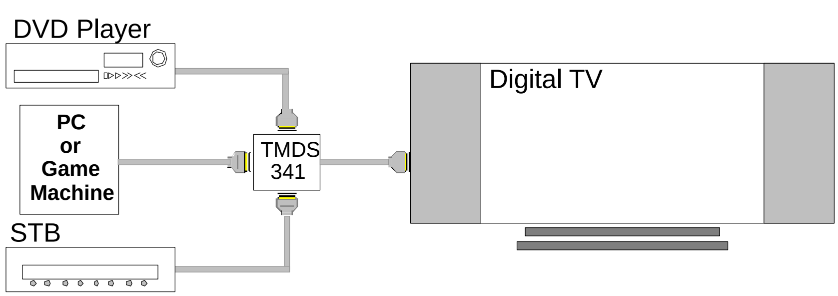
The TMDS341 is a 3-port digital video interface (DVI) or high-definition multimedia interface (HDMI) switch that allows up to 3 DVI or HDMI ports to be switched to a single display terminal. Four TMDS channels, one hot plug detector, and an I^2C interface are supported on each port. Each TMDS channel allows signaling rates up to 1.65 Gbps.

The active source is selected by configuring source selectors, S1, S2, and S3. The selected TMDS inputs from each port are switched through a 3-to-1 multiplexer. The I^2C interface of the selected input port is linked to the I^2C interface of the output port, and the hot plug detector (HPD) of the selected input port is output to HPD_SINK. For the unused ports, the I^2C interfaces are isolated, and the HPD pins are kept low.

Termination resistors (50-Ω), pulled up to V_{CC}, are integrated at each receiver input pin. External terminations are not required. A precision resistor is connected externally from the VSADJ pin to ground for setting the differential output voltage to be compliant with the TMDS standard. When the output is connected to a standard TMDS termination and $\overline{OE}$ is high, the output is high impedance.

The TMDS341 provides fixed 8-dB input equalization and selectable 3-dB output de-emphasis to optimize system performance through 5-meter or longer DVI compliant cables. The device is characterized for operation from 0°C to 70°C.

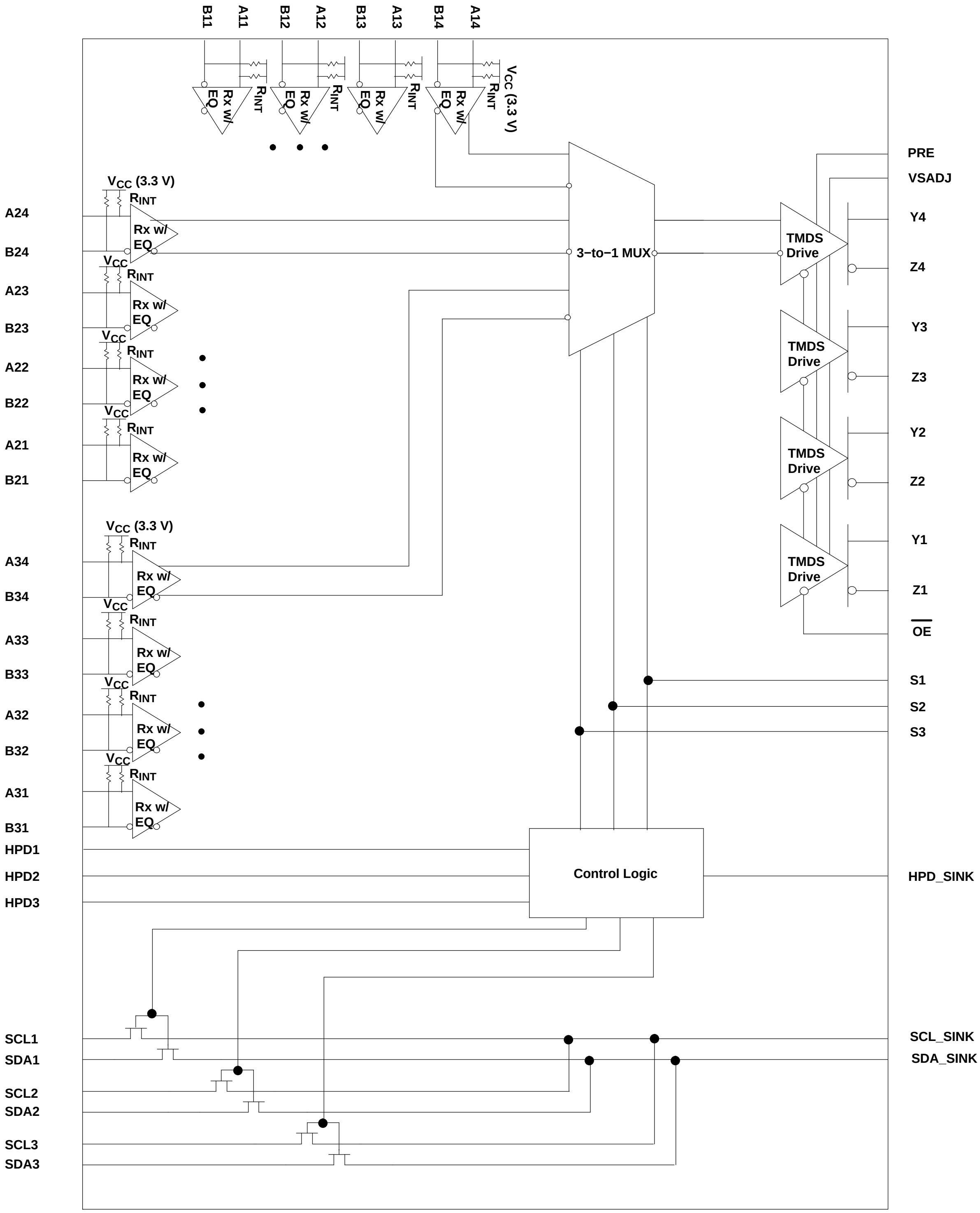
TYPICAL APPLICATION



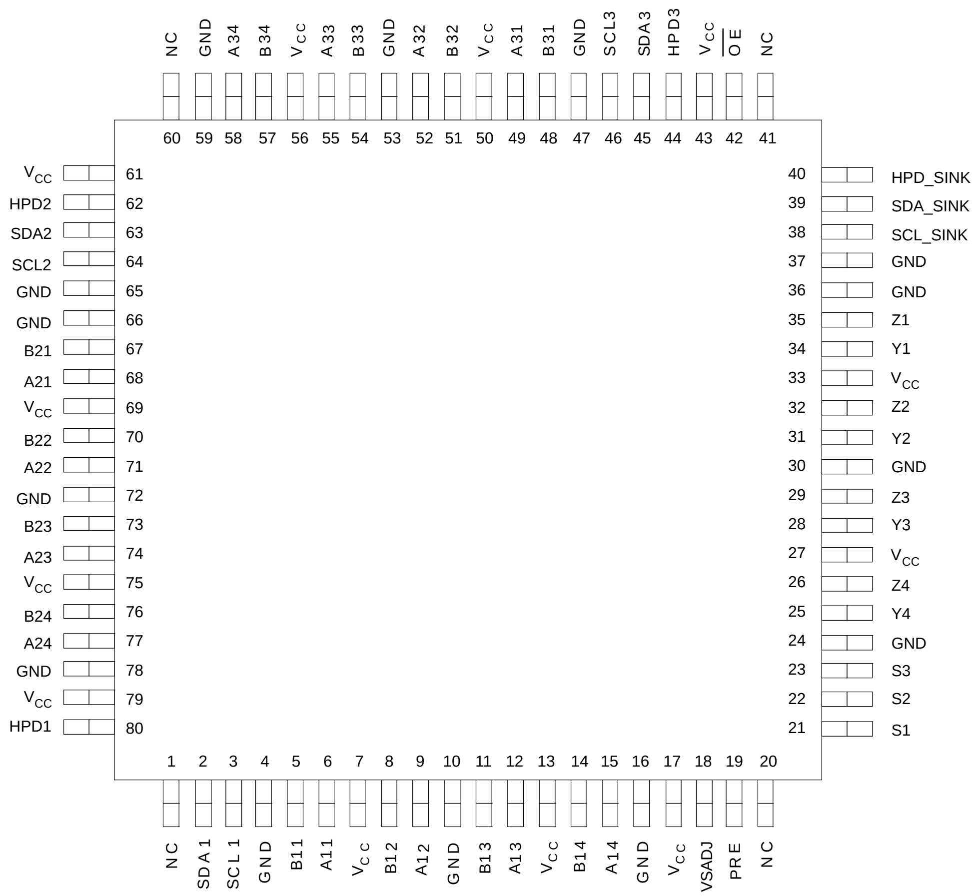
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



PFC PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
A11, A12, A13, A14	6, 9, 12, 15	I	Port 1 TMDS positive inputs
A21, A22, A23, A24	68, 71, 74, 77	I	Port 2 TMDS positive inputs
A31, A32, A33, A34	49, 52, 55, 58	I	Port 3 TMDS positive inputs
B11, B12, B13, B14	5, 8, 11, 14	I	Port 1 TMDS negative inputs
B21, B22, B23, B24	67, 70, 73, 76	I	Port 2 TMDS negative inputs
B31, B32, B33, B34	48, 51, 54, 57	I	Port 3 TMDS negative inputs
GND	4, 10, 16 24, 30, 36, 37, 47, 53, 59, 65, 66, 72, 78		Ground
HPD1	80	O	Port 1 hot plug detector output
HPD2	62	O	Port 2 hot plug detector output
HPD3	44	O	Port 3 hot plug detector output
HPD_SINK	40	I	Sink side hot plug detector input High: 5-V power signal asserted from source to sink and EDID is ready Low: No 5-V power signal asserted from source to sink, or EDID is not ready
NC	1, 20, 41,60		No connect
$\overline{\text{OE}}$	42	I	Output enable, active low
PRE	19	I	Output de-emphasis adjustment High: 3 dB Low: 0 dB
SCL1	3	I/O	Port 1 DDC bus clock line
SCL2	64	I/O	Port 2 DDC bus clock line
SCL3	46	I/O	Port 3 DDC bus clock line
SCL_SINK	38	I/O	Sink side DDC bus clock line
SDA1	2	I/O	Port 1 DDC bus data line
SDA2	63	I/O	Port 2 DDC bus data line
SDA3	45	I/O	Port 3 DDC bus data line
SDA_SINK	39	I/O	Sink side DDC bus data line
S1, S2, S3	21, 22, 23	I	Source selector input
V_{CC}	7, 13, 17 27, 33, 43, 50, 56 61, 69, 75, 79		Power supply
VSADJ	18	I	TMDS compliant voltage swing control
Y1, Y2, Y3, Y4	34, 31, 28, 25	O	TMDS positive outputs
Z1, Z2, Z3, Z4	35, 32, 29, 26	O	TMDS negative outputs

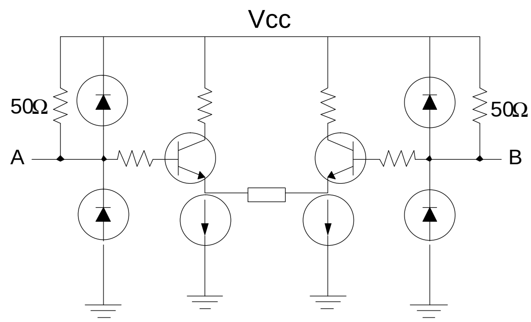
Table 1. Source Selection Lookup[(1)]

CONTROL PINS			I/O SELECTED		HOT PLUG DETECT STATUS		
S1	**S2**	**S3**	**Y/Z**	**SCL_SINK SDA_SINK**	**HPD1**	**HPD2**	**HPD3**
H	x	x	A1/B1	SCL1 SDA1	HPD_SINK	L	L
L	H	x	A2/B2	SCL2 SDA2	L	HPD_SINK	L
L	L	H	A3/B3	SCL3 SDA3	L	L	HPD_SINK
L	L	L	None (Z)	None (Z)	L	L	L

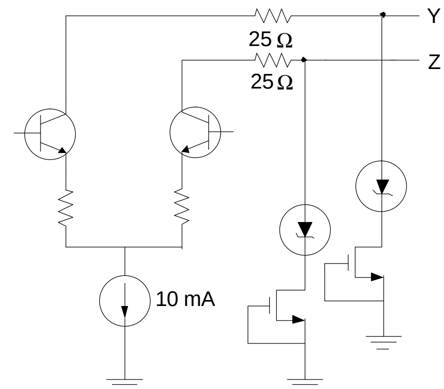
(1) H: Logic high; L: Logic low; X: Don't care; Z: High impedance

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

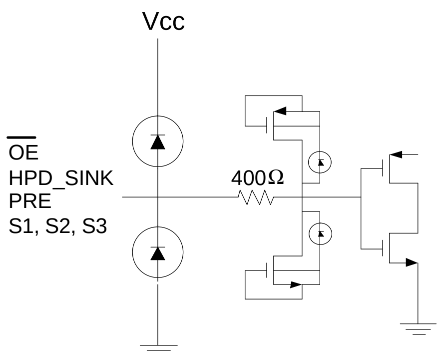
TMDS Input Stage



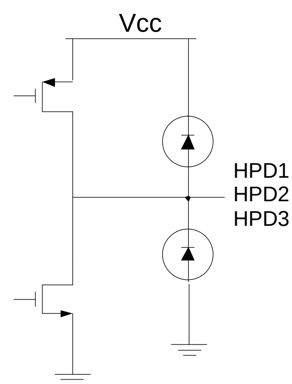
TMDS Output Stage



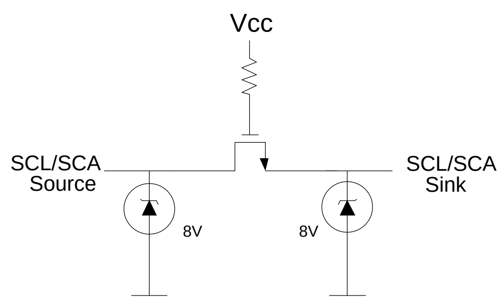
Control Input Stage



HPD output stage



DDC pass gate



ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
TMDS341PFC	TMDS341	80-PIN TQFP
TMDS341PFCR	TMDS341	80-PIN TQFP Tape/Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Supply voltage range, V_{CC} (2)		–0.5 V to 4 V
Voltage range	Anm(3), Bnm	1.7 V to 4 V
	Ym, Zm, VSADJ, PRE, Sn, $\overline{OE}$, HPDn	–0.5V to 4 V
	SCLn, SCL_SINK, SDAn, SDA_SINK, HPD_SINK	–0.5 V to 6 V
Electrostatic discharge	Human body model(4) (all pins)	±3 kV
	Charged-device model(5) (all pins)	±1500 V
	Machine model (6) (all pins)	± 200 V
Continuous power dissipation		See Dissipation Rating Table

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) n = 1, 2, 3; m = 1, 2, 3, 4
(4) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(5) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(6) Tested in accordance with JEDEC Standard 22, Test Method A115-A

DISSIPATION RATINGS

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR (1) ABOVE T_A = 25°C	T_A = 70°C POWER RATING
80-TQFP	1342 mW	13.42 mW/°C	738 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	0		70	°C
TMDS DIFFERENTIAL PINS (A/B)					
V_{ID}	Receiver peak-to-peak differential input voltage	150		1560	mVp-p
V_{IC}	Input common mode voltage	2		V_{CC}–0.04	V
R_{VSADJ}	Resistor for TMDS compliant voltage swing range	4.6	4.64	4.68	kΩ
AV_{CC}	TMDS output termination voltage, see Figure 1	3	3.3	3.6	V
R_T	Termination resistance, see Figure 1	45	50	55	Ω
	Signaling rate	0		1.65	Gbps
CONTROL PINS (PRE; S, $\overline{OE}$)					
V_{IH}	LVTTL High-level input voltage	2		V_{CC}	V
V_{IL}	LVTTL Low-level input voltage	GND		0.8	V
DDC I/O PINS (SCL, SCL_SINK, SDA, SDA_SINK)					
$V_{I(DDC)}$	Input voltage	GND		5.3	V
STATUS PINS (HPD_SINK)					
V_{IH}	LVTTL High-level input voltage	2		5.3	V
V_{IL}	LVTTL Low-level input voltage	GND		0.8	V

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	$V_{IH} = V_{CC}$, $V_{IL} = V_{CC} – 0.4$ V, $R_{VSADJ} = 4.64$ kΩ, $R_T = 50$ Ω, $AV_{CC} = 3.3$ V Am/Bm = 1.65 Gbps HDMI data pattern, m = 2, 3, 4 A1/B1 = 165 MHz clock		190	230	mA
P_D	Power dissipation	$V_{IH} = V_{CC}$, $V_{IL} = V_{CC} – 0.4$ V, $R_{VSADJ} = 4.64$ kΩ, $R_T = 50$ Ω, $AV_{CC} = 3.3$ V Am/Bm = 1.65 Gbps HDMI data pattern, m = 2, 3, 4 A1/B1 = 165 MHz clock		394	657	mW
TMDS DIFFERENTIAL PINS (A/B; Y/Z)						
V_{OH}	Single-ended high-level output voltage	See Figure 2, $AV_{CC} = 3.3$ V, $R_T = 50$ Ω, PRE = 0 V	AV_{CC}–10		AV_{CC}+10	mV
V_{OL}	Single-ended low-level output voltage		AV_{CC}–600		AV_{CC}–400	mV
V_{swing}	Single-ended output swing voltage		400		600	mV
$V_{OD(O)}$	Overshoot of output differential voltage			6%	15%	2× V_{swing}
$V_{OD(U)}$	Undershoot of output differential voltage			12%	25%	2× V_{swing}
$ΔV_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			0.5	5	mV
$I_{(O)OFF}$	Single-ended standby output current	0 V ≤ V_{CC} ≤ 1.5 V, $AV_{CC} = 3.3$ V, $R_T = 50$ Ω	–10		10	µA
$\|I_{(OS)}\|$	Short circuit output current	See Figure 3			12	mA
$V_{ODE(SS)}$	Steady state output differential voltage with de-emphasis	See Figure 4, PRE = V_{CC}, Am/Bm = 250 Mbps HDMI data pattern, m = 2, 3, 4 A1/B1 = 25 MHz clock	560		840	mVp-p
$V_{ODE(pp)}$	Peak-to-peak output differential voltage		800		1200	mVp-p
$V_{I(open)}$	Single-ended input voltage under high impedance input or open input	$I_I = 10$ µA	V_{CC}–10		V_{CC}+10	mV
R_{INT}	Input termination resistance	$V_{IN} = 2.9$ V	45	50	55	Ω
DDC I/O PINS (SCL, SCL_SINK, SDA, SDA_SINK)						
$\|I_{lkg}\|$	Input leakage current	$V_I = 0.1$ V_{CC} to 0.9 V_{CC} to isolated DDC ports		0.1	2	µA
C_{IO}	Input/output capacitance	$V_I = 0$ V		7.5		pF
R_{ON}	Switch resistance	$I_O = 3$ mA, $V_O = 0.4$ V		25	50	Ω
V_{PASS}	Switch output voltage	$V_I = 3.3$ V, $I_O = 100$ µA	1.5(2)	2.0	2.5(3)	V
STATUS PINS (HPD)						
$V_{OH(TTL)}$	TTL High-level output voltage	$I_{OH} = –8$ mA	2.4			V
$V_{OL(TTL)}$	TTL Low-level output voltage	$I_{OL} = 8$ mA			0.4	V
CONTROL PINS (PRE, S, $\overline{OE}$)						
$\|I_{IH}\|$	High-level digital input current	$V_{IH} = 2$ V or V_{CC}		0.1	2	µA
$\|I_{IL}\|$	Low-level digital input current	V_{IL} = GND or 0.8 V		0.1	2	µA
STATUS PINS (HPD_SINK)						
$\|I_{IH}\|$	High-level digital input current	$V_{IH} = 5.3$ V		23	100	µA
		$V_{IH} = 2$ V or V_{CC}		0.1	2	
$\|I_{IL}\|$	Low-level digital input current	V_{IL} = GND or 0.8 V		0.1	2	µA

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) The value is tested in full temperature range at 3.0 V.
(3) The value is tested in full temperature range at 3.6 V.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
TMDS DIFFERENTIAL PINS (Y/Z)						
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2, AV_{CC} = 3.3 V, R_T = 50 Ω, PRE = 0 V	250		800	ps
t_{PHL}	Propagation delay time, high-to-low-level output		250		800	ps
t_r	Differential output signal rise time (20% - 80%)		75		240	ps
t_f	Differential output signal fall time (20% - 80%)		75		240	ps
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)			7	50	ps
$t_{sk(D)}$	Intra-pair differential skew, see Figure 5			23	50	ps
$t_{sk(o)}$	Inter-pair channel-to-channel output skew(2)				100	ps
$t_{sk(pp)}$	Part-to-part skew (3)				200	ps
$t_{jit(pp)}$	Peak-to-peak output jitter from Y/Z(1) residual jitter	See Figure 8, PRE = 0 V Am/Bm = 1.65 Gbps HDMI data pattern, m = 2, 3, 4 A1/B1 = 165 MHz clock		15	30	ps
$t_{jit(pp)}$	Peak-to-peak output jitter from Y/Z(2:4) residual jitter			18	50	ps
t_{PRE}	De-emphasis duration	See Figure 4, PRE = V_{CC} Am/Bm = 250 Mbps HDMI data pattern, m = 2, 3, 4 A1/B1 = 25 MHz clock		240(4)		ps
t_{SX}	Select to switch output	See Figure 6		6	10	ns
t_{en}	Enable time			6	10	ns
t_{dis}	Disable time			6	10	ns
DDC I/O PINS (SCL, SCL_SINK, SDA, SDA_SINK)						
$t_{pd(DDC)}$	Propagation delay from SCLn to SCL_SINK or SDAn to SDA_SINK or SDA_SINK to SDAn	See Figure 7, C_L = 10 pF		0.4	2.5	ns
CONTROL AND STATUS PINS (S, HPD_SINK, HPD)						
$t_{pd(HPD)}$	Propagation delay (from HPD_SINK to the active port of HPD)	See Figure 7, C_L = 10 pF		2	6.0	ns
$t_{sx(HPD)}$	Switch time (from port select to the latest valid status of HPD)			3	6.5	ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(o)}$ is the magnitude of the difference in propagation delay times between any specified terminals of channel 2 to 4 of a device when inputs are tied together.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of channel 2 to 4 of two devices, or between channel 1 of two devices, when both devices operate with the same source, the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) The typical value is ensured by simulation.

PARAMETER MEASUREMENT INFORMATION

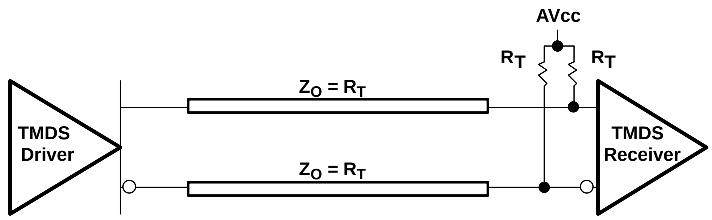
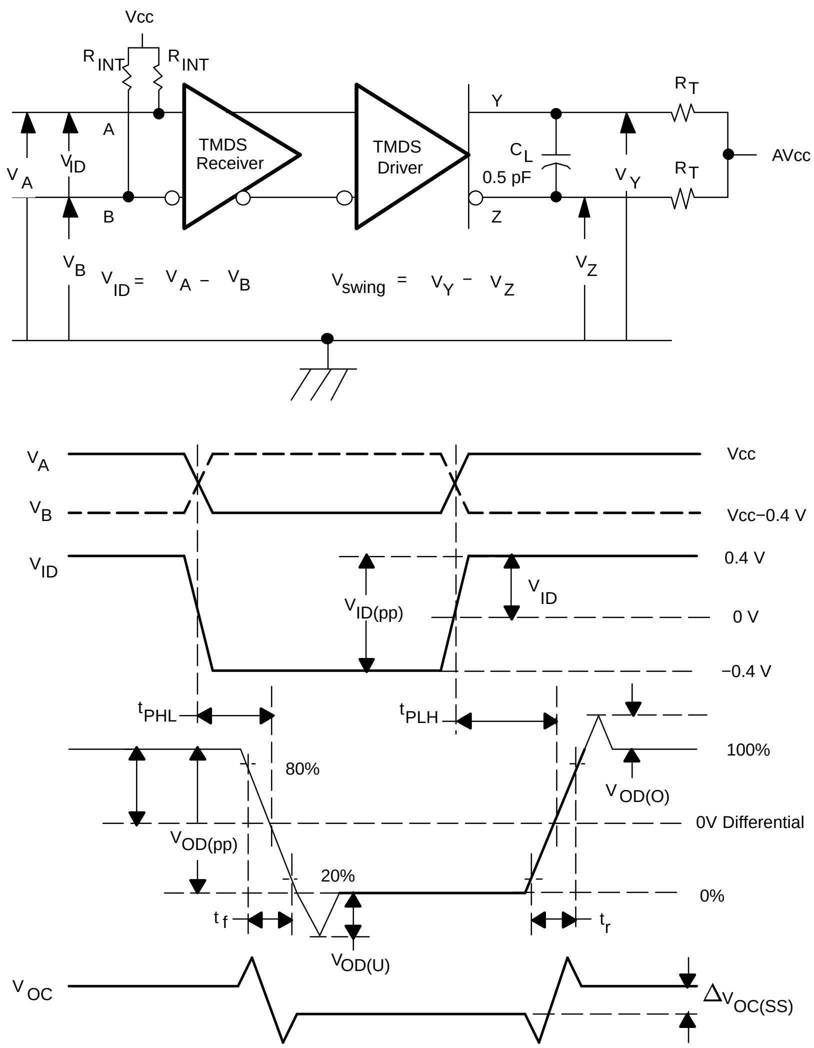


Figure 1. Termination for TMDS Output Driver



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f < 100 ps, 100 MHz from Agilent 81250. C_L includes instrumentation and fixture capacitance within 0.06 m of the D.U.T. Measurement equipment provides a bandwidth of 20 GHz minimum.

Figure 2. Timing Test Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

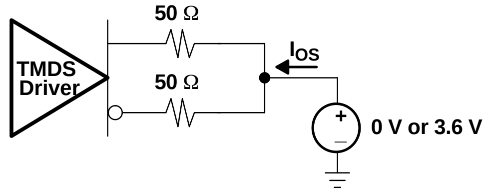


Figure 3. Short Circuit Output Current Test Circuit

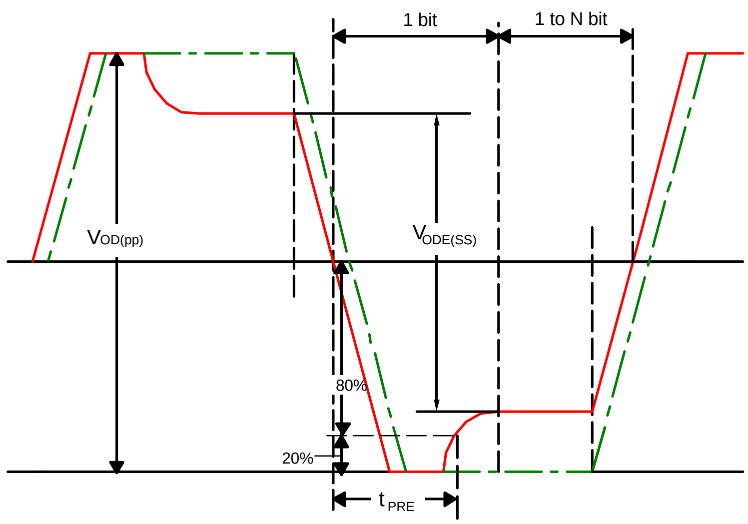


Figure 4. De-Emphasis Output Voltage Waveforms and Duration Measurement Definitions

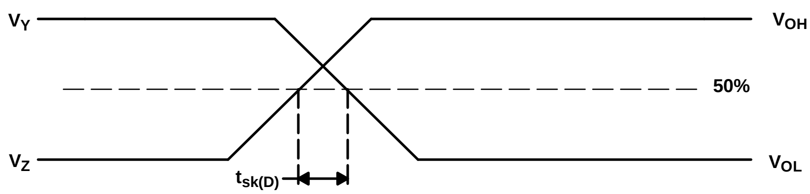


Figure 5. Definition of Intra-Pair Differential Skew

PARAMETER MEASUREMENT INFORMATION (continued)

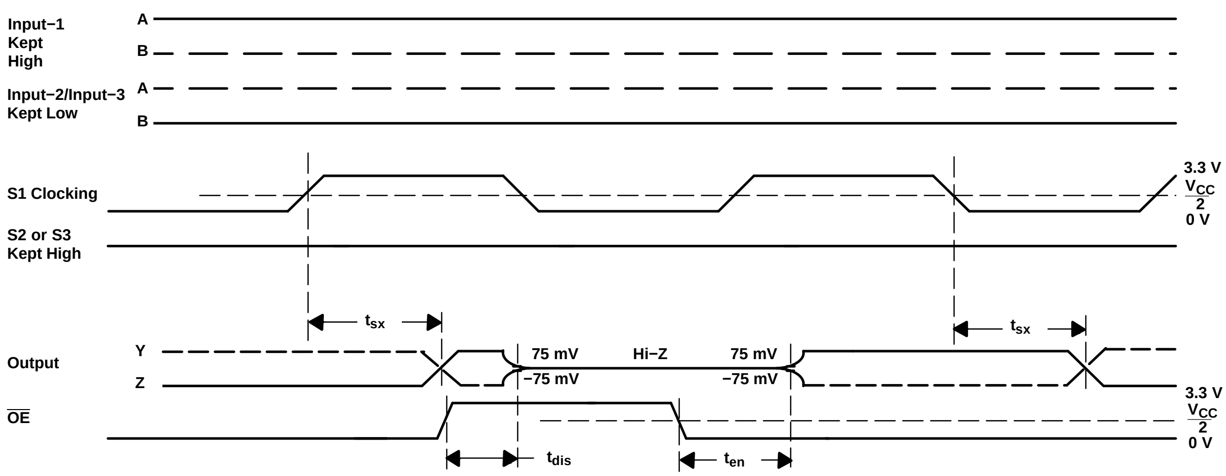


Figure 6. TMDS Outputs Control Timing Definitions

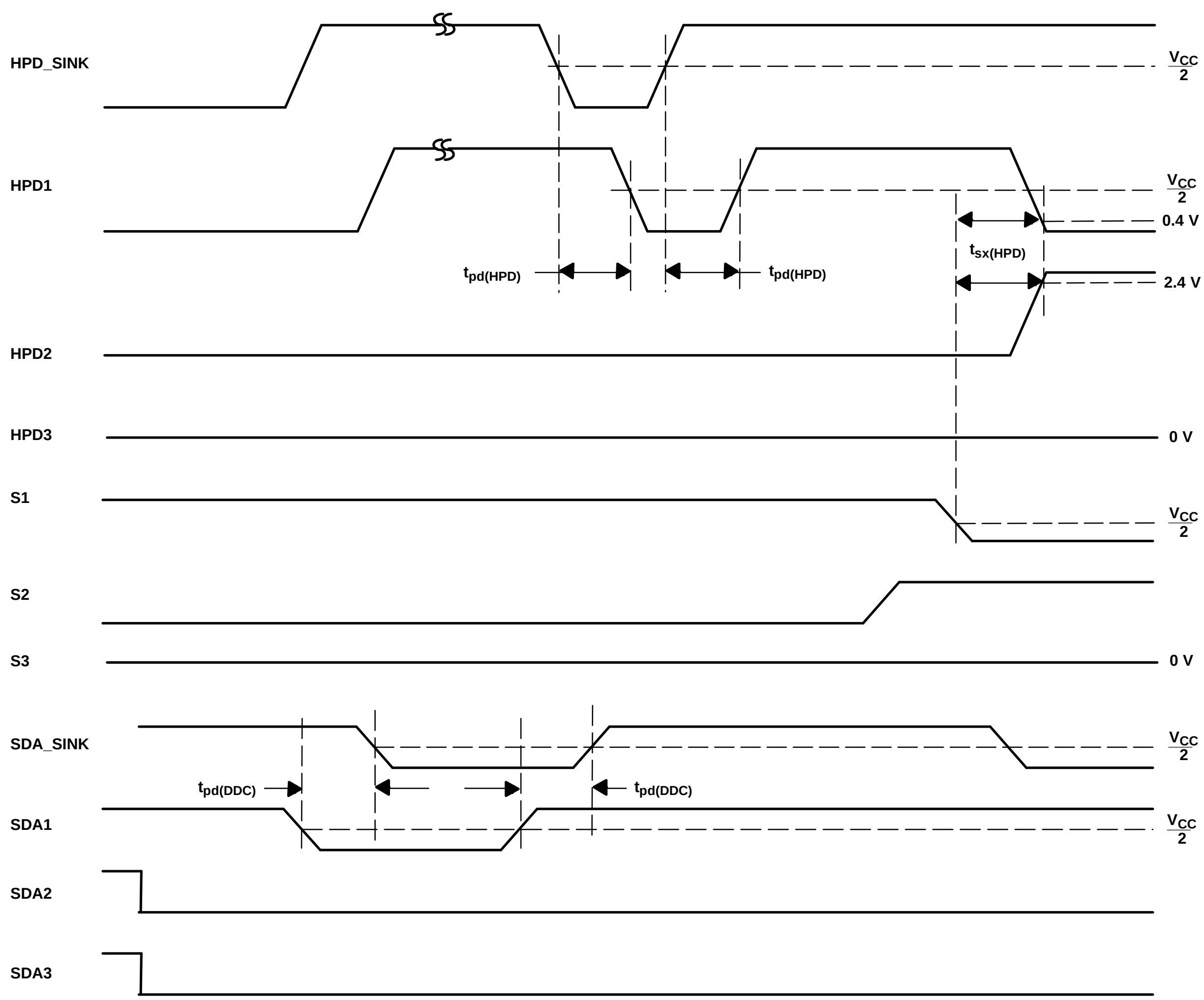
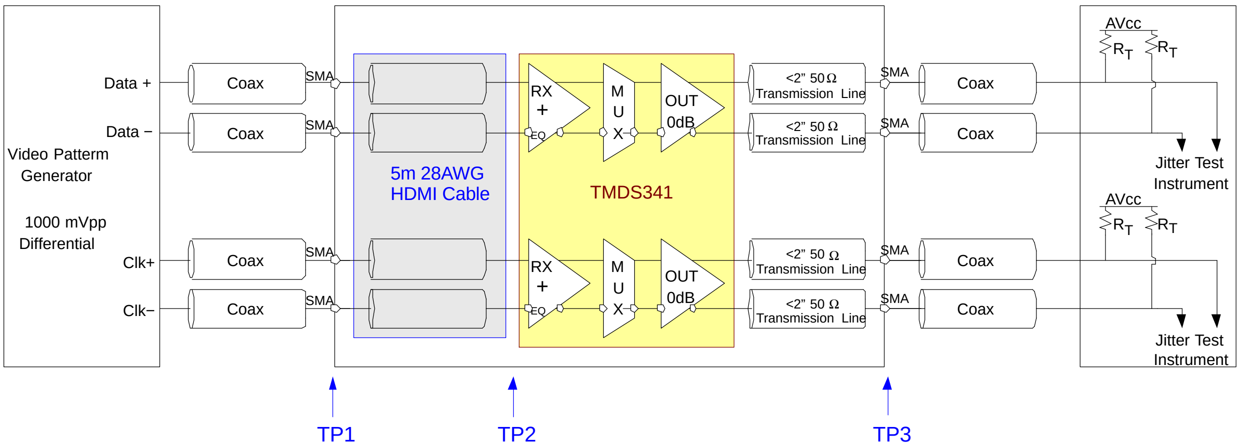


Figure 7. HPD Timing Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



A. All jitters are measured in BER of 10^{-12}

B. The residual jitter reflects the total jitter measured at the TMDS341 output, TP3, subtract the total jitter from the signal generator, TP1

Figure 8. Jitter Test Circuit

Figure 9 shows the frequency loss response from a 5m 28AWG HDMI cable and a 5m 28AWG DVI cable. The TMDS341 built-in passive input equalizer compensates for ISI. For an 8-dB loss HDMI cable, the TMDS341 typically reduces jitter by 60 ps from the device input to the device output.

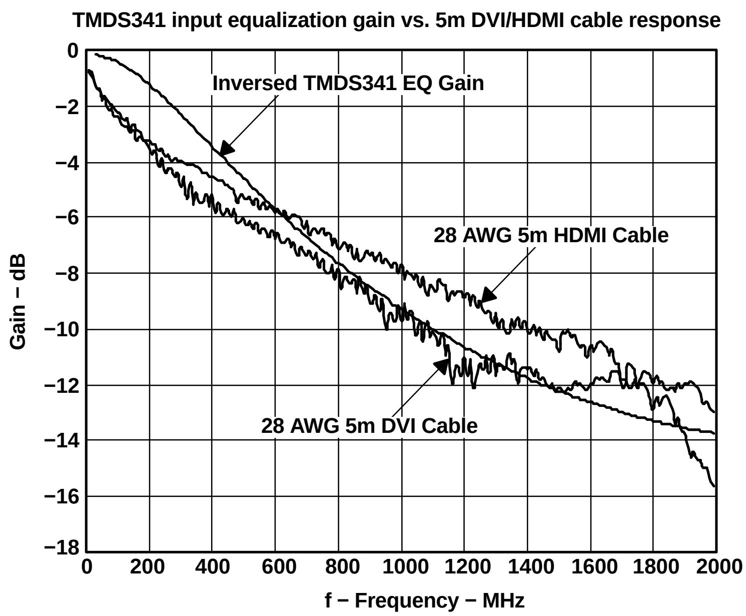


Figure 9. S-Parameter Plots of 5-m DVI and HDMI Cables

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

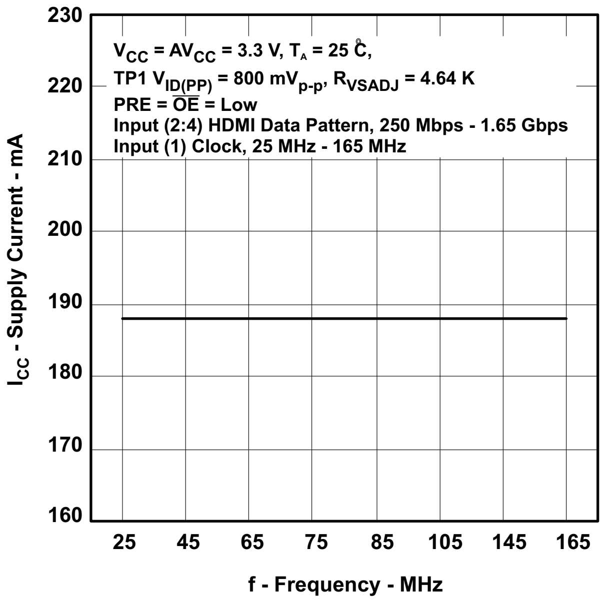


Figure 10.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

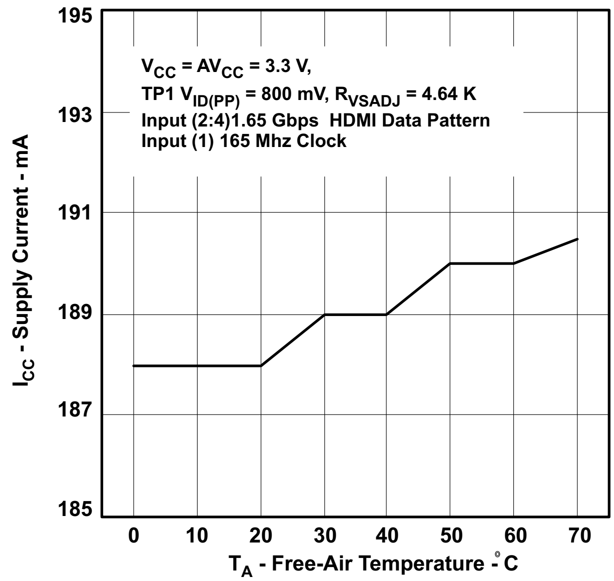


Figure 11.

RESIDUAL DETERMINISTIC JITTER vs DATA RATE

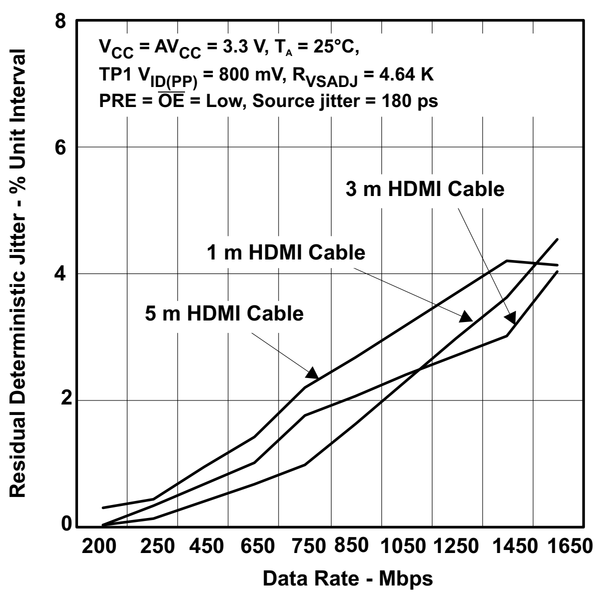


Figure 12.

RESIDUAL PEAK-TO-PEAK JITTER vs CLOCK FREQUENCY

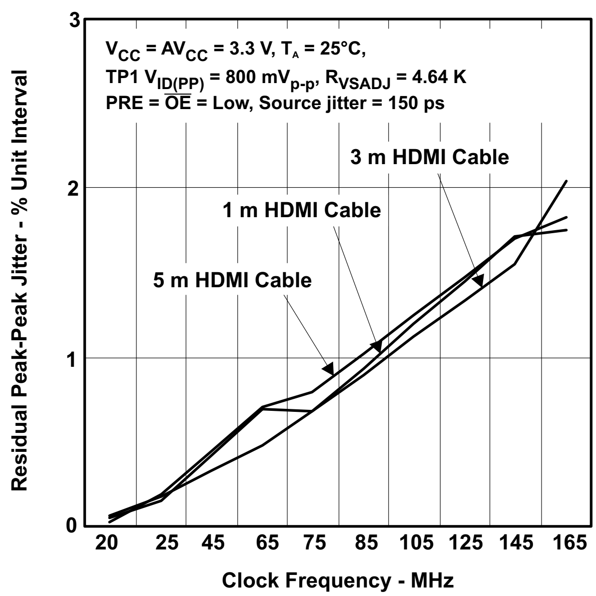


Figure 13.

TYPICAL CHARACTERISTICS (continued)

RESIDUAL DETERMINISTIC JITTER
vs
DIFFERENTIAL INPUT VOLTAGE

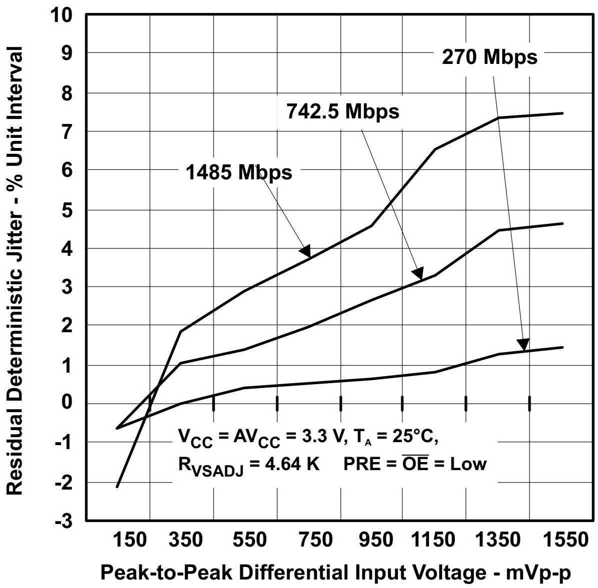


Figure 14.

RESIDUAL PEAK-TO-PEAK JITTER
vs
DIFFERENTIAL INPUT VOLTAGE

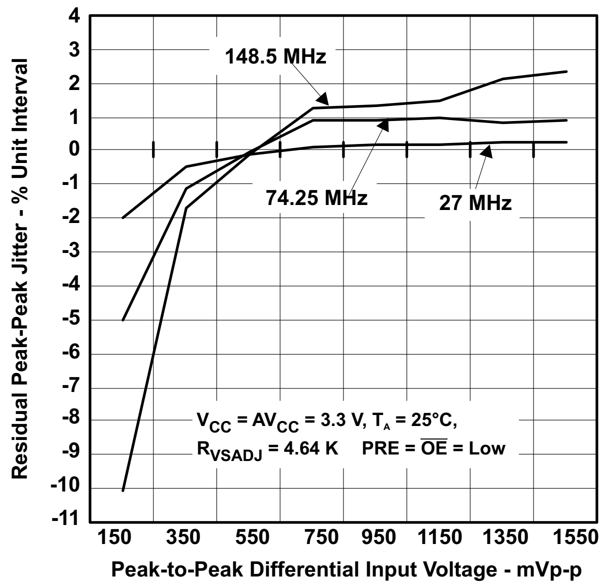


Figure 15.

RESIDUAL DETERMINISTIC JITTER
vs
FR4 PCB TRACE (at 3dB Pre-Emphasis)

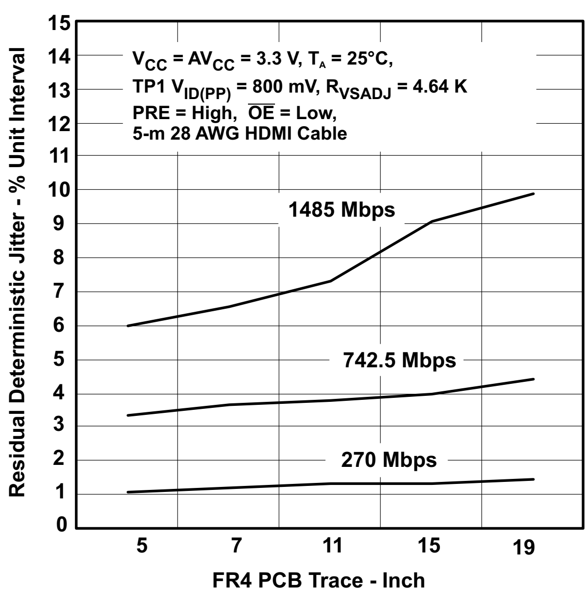


Figure 16.

RESIDUAL PEAK-TO-PEAK JITTER
vs
FR4 PCB TRACE (at 3dB Pre-Emphasis)

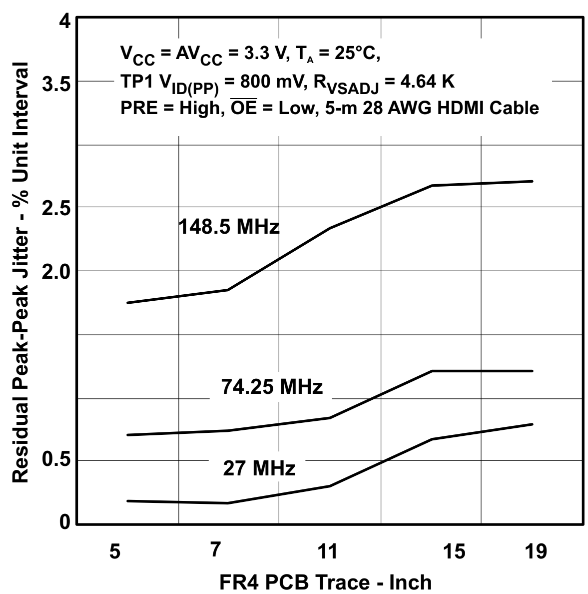


Figure 17.

TYPICAL CHARACTERISTICS (continued)

HDMI Cables Running at 165-MHz Pixel Clock

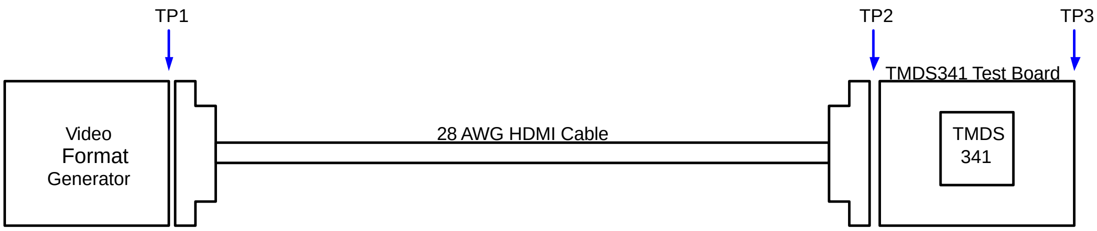


Figure 18. 1-m and 5-m HDMI Cable Test Point Configuration

1-m Cable Length Eye Patterns

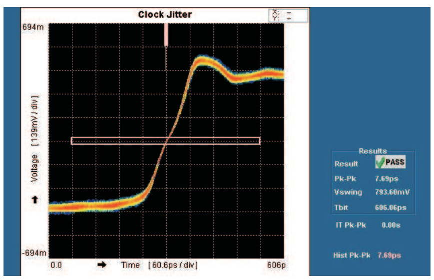


Figure 19. Clock at TP1

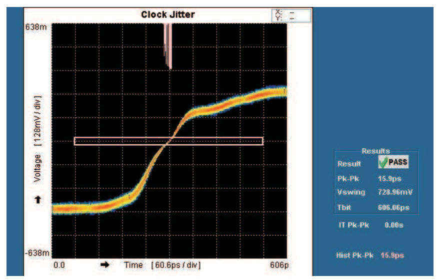


Figure 20. Clock at TP2

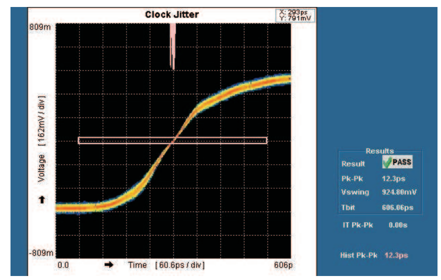


Figure 21. Clock at TP3

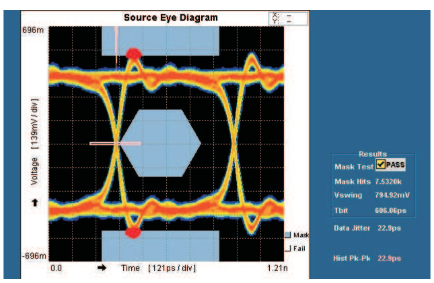


Figure 22. Data at TP1

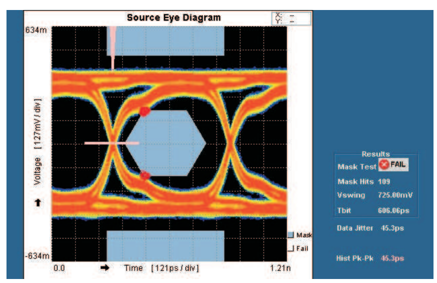


Figure 23. Data at TP2

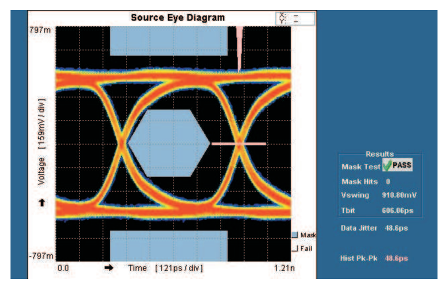


Figure 24. Data at TP3

TYPICAL CHARACTERISTICS (continued)

5-m Cable Length Eye Patterns

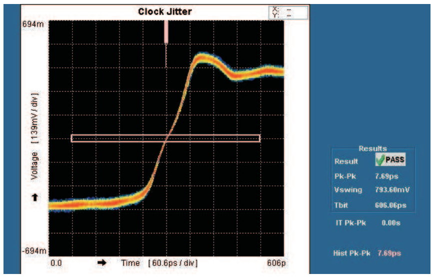


Figure 25. Clock at TP1

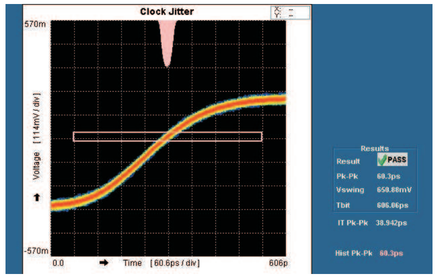


Figure 26. Clock at TP2

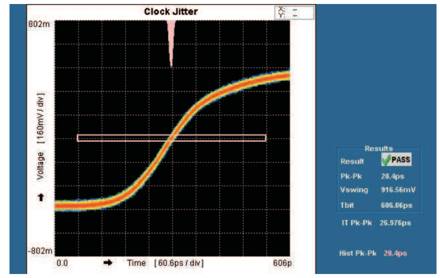


Figure 27. Clock at TP3

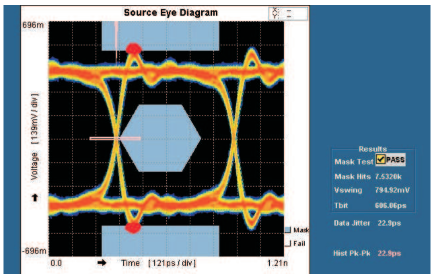


Figure 28. Data at TP1

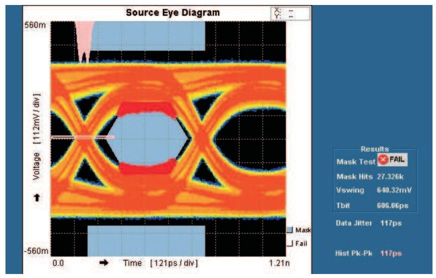


Figure 29. Data at TP2

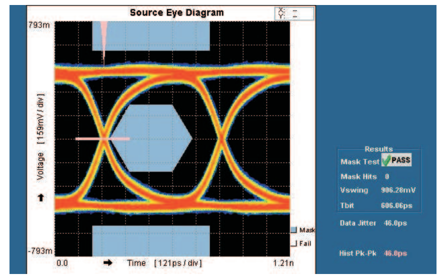


Figure 30. Data at TP3

APPLICATION INFORMATION

Supply Voltage

All V_{CC} pins can be tied to a single 3.3-V power source. A 0.01-µF capacitor is connected from each V_{CC} pin directly to ground to filter supply noise.

TMDS Inputs

Standard TMDS terminations are integrated on all TMDS inputs. External terminations are not required. Each input channel contains an 8-dB equalization circuit to compensate for cable losses. The voltage at the TMDS input pins must be limited per the absolute maximum ratings. An unused input should not be connected to ground as this would result in excessive current flow damaging the device.

TMDS Input Fail-Safe

TMDS input pins do not incorporate fail-safe circuits. An unused input channel can be externally biased to prevent output oscillation. One pin can be left open with the other grounded through a 1-kΩ resistor as shown in Figure 31.

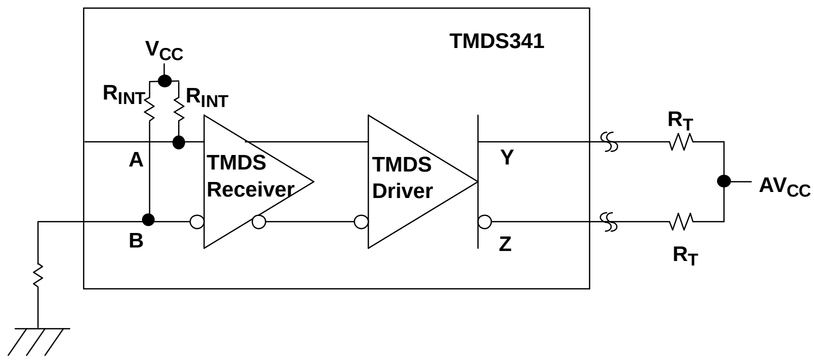


Figure 31. TMDS Input Fail-Safe Recommendation

TMDS Outputs

A 1% precision resister, 4.64-kΩ, connected from VSADJ to ground is recommended to allow the differential output swing to comply with TMDS signal levels. The differential output driver provides a typical 10-mA current sink capability, which provides a typical 500-mV voltage drop across a 50-Ω termination resistor.

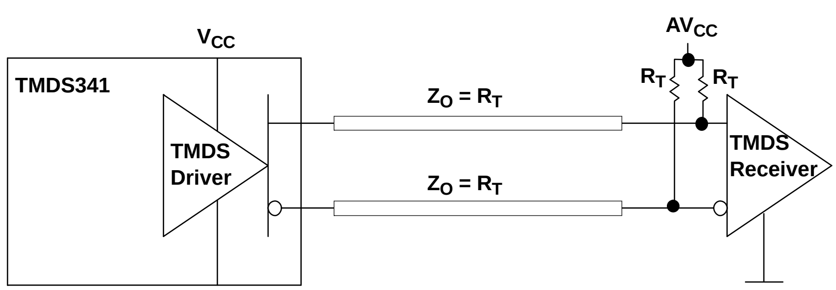


Figure 32. TMDS Driver and Termination Circuit

As shown in Figure 32, if V_{CC} (TMDS341 supply) and AV_{CC} (sink termination supply) are powered, the TMDS output signals are high impedance when $\overline{OE}$ is high. Normal operation is with both supplies active.

Also shown in Figure 32, if V_{CC} is on and AV_{CC} is off, the TMDS outputs source a typical 5-mA current through each termination resistor to ground. The terminations consume a total of 10 mW of power independent of the $\overline{OE}$ logical selection. When AV_{CC} is powered on, normal operation ($\overline{OE}$ controls output impedance) is resumed.

APPLICATION INFORMATION (continued)

When the power source of the device, V_{CC}, is off and the power source to termination, AV_{CC}, is on, the output leakage current ($I_{o(off)}$) specification ensures leakage current is limited to 10-µA or less.

The PRE pin provides 3-dB de-emphasis, allowing output signal pre-conditioning to offset interconnect losses from the TMDS341 outputs to a TMDS receiver. PRE is recommended to be low to the circuit design of a stand-alone switch box.

HPD Pins

The input of the HPD_SINK is 5-V tolerant, allowing direct connection to 5-V signals. The HPD pin output resistance is 35-Ω typically. A 1-kΩ 10% resistor is recommended to be connected from an HPD pin at the TMDS341 to the HPD pin of the HDMI connector.

DDC Channels

The DDC channels are designed with a bi-directional pass gate, providing 5-V signal tolerance. The 5-V tolerance allows direct connection to a standard I^2C bus. The level shifter between 3.3 V and 5 V I^2C interface can be eliminated.

Configuring the TMDS341 as a 2:1 Switch

The TMDS341 can be configured as a 2-to-1 switch by pulling the source selector pin (S1, S2, S3) of the non-active port low and leaving the corresponding TMDS inputs, SCL, SDA, and HPD pins open.

Layout Considerations

The high-speed TMDS inputs are the most critical paths for the TMDS341. There are several considerations to minimize discontinuities on these transmission lines between the connectors and the device:

- Maintain 100-Ω differential transmission line impedance into and out of the TMDS341
- Keep an uninterrupted ground plane beneath the high-speed I/Os
- Keep the ground-path vias to the device as close as possible to allow the shortest return current path
- Layout of the TMDS differential inputs should be with the shortest stubs from the connectors

Connecting Cables Longer Than 5 m

When using the TMDS341 with cables longer than 5 m, the impact to the TMDS signal path as well as the DDC signal path must be considered.

TMDS Signal Path

The TMDS341 receiver equalization circuit provides the capability of compensating inter-symbol interference (ISI) losses in a 5-m 28-AWG DVI cable. Typical cable measurements indicate that the TMDS341 can drive a 5-m 28-AWG HDMI cable and pass the eye mask at the output of a HDMI source (TP1) and a 10-m 28-AWG HDMI cable and pass the eye mask at the input of a HDMI sink (TP2). Figure 33 through Figure 36 show the eye mask measurement results.

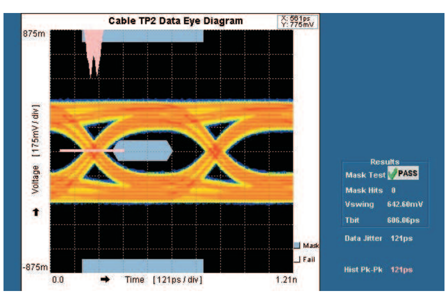


Figure 33. Eye Diagram at Output 5-m 28-AWG Cable vs TP1 Eye Mask

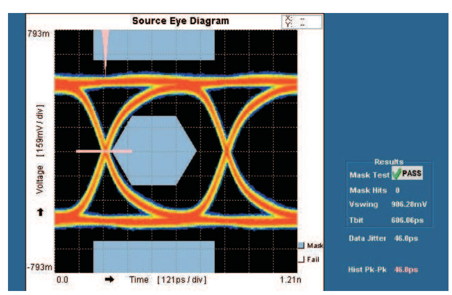


Figure 34. Eye Diagram Recovered by TMDS341 vs TP1 Eye Mask

APPLICATION INFORMATION (continued)

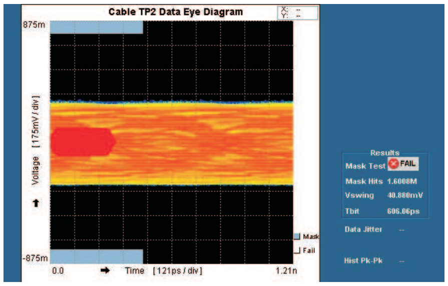


Figure 35. Eye Diagram at Output 10-m 28-AWG Cable vs TP2 Eye Mask

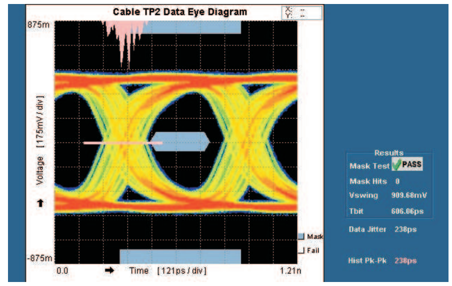


Figure 36. Eye Diagram Recovered by TMDS341 vs TP2 Eye Mask

DDC Signal Path

Observed I^2C bus voltage is dependent on bus resistance, capacitance, and time. The transient bus voltage, when charging from a low state to a high state, can be calculated using equation (1).

$$V(t) = V_{DD}(1 - e^{-t/RC}) \quad (1)$$

Where:

t is the time since the charging started

V_{DD} is the pull-up termination voltage

R is the total resistance on the I^2C link

C is the total capacitance on the I^2C link

In the I^2C bus specification, version 2.1, the high-level threshold voltage is V_{IH} = 0.7 V_{DD}, and the low-level threshold voltage is V_{IL} = 0.3 V_{DD}.

From equation (1), the times to charge from a bus voltage of 0 V to the V_{IH} and V_{IL} levels are:

$t_{IH} = 1.204 \times RC$

$t_{IL} = 0.357 \times RC$

The bus rise time (from 0.3 V_{DD} to 0.7 V_{DD}) is then given by equation (2):

$$t_{r(30\text{-}70)} = t_{IH} - t_{IL} = 0.847 \times RC \quad (2)$$

The TMDS341 can be easily applied in stand-alone switch boxes and digital displays. The following sections show the bus lengths that can be supported in each case.

Maximum Bus Lengths for Switch Applications

Figure 37 shows the TMDS341 being used as a stand-alone switch. Both pull-up resistors are decided by the source and sink equipment. A 1.5-kΩ resistor at the source and a 47-kΩ resistor at the sink are recommended.

APPLICATION INFORMATION (continued)

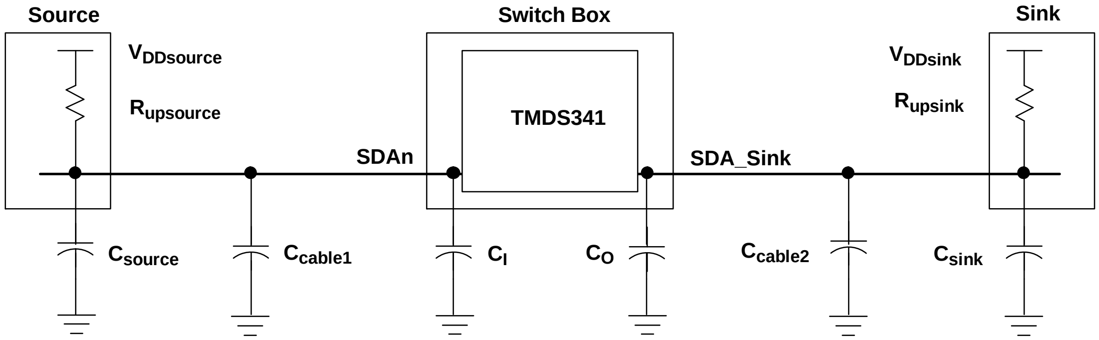


Figure 37. DDC Link from Source to Sink With External Switch Box

$R_{upsource}$ = 1.5-kΩ pull-up to 5 V

R_{upsink} = 47-kΩ pull-up to 5 V

$R_{total} = R_{upsource} // R_{upsink}$ = 1.45 kΩ

$C_{total} = C_{source} // C_{cable1} // C_i // C_o // C_{cable2} // C_{sink}$

For standard mode I^2C, the frequency is at 100 kHz, and the transition time must be less than 1 µs. The total allowable capacitance, C_{total}, is then 814-pF. C_{source} and C_{sink} are limited by the HDMI specification to 50 pF. $C_{i/o}$ for the TMDS341 is 10 pF max. The total capacitance from DVI or HDMI cables, C_{cable1} and C_{cable2}, should then be less than 704 pF.

Typical capacitance is 200 pF for a 28-AWG 5-m HDMI cable and 300 pF for a 28-AWG 5-m DVI cable. The recommended total cable length is the length of cable 1, Lcable1, plus the length of cable 2, Lcable2. For a 28-AWG DVI cable, the total cable length is 11 m; and for a 28-AWG HDMI cable, the total cable length is 17 m.

This calculation is applicable to $V_{IH} \leq V_{pass}$.

Maximum Bus Lengths for DTV Applications

Figure 38 shows the TMDS341 being used as a switch in a DTV and being placed on the same PCB board as the DVI/HDMI receiver. Unlike Figure 37, the output connector of the TMDS341 stand-alone switch and the input connector of the sink are removed, which results in a lower capacitance in the DDC link and eliminates the impedance discontinuity. However, the capacitance of the removed connectors is relatively small, relative to the total allowable capacitance. The results from the previous section *Maximum Bus Lengths for Switch Applications* can be reused if the pull-up resistors and capacitances have the same values. The recommended total cable length is the length from source to sink.

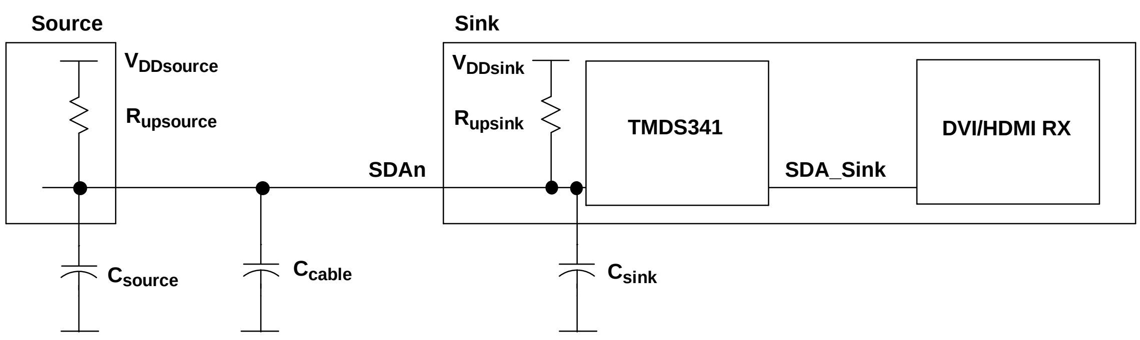


Figure 38. DDC Link From Source to Sink Without External Switch Box

APPLICATION INFORMATION (continued)

Table 2 summarizes the recommended cable lengths based on threshold voltages V_{IH} = 0.7 V_{DD} and V_{IL} = 0.3 V_{DD}.

Table 2. Recommended Cable Lengths Under General Threshold Voltages, 0.7 V_{DD} and 0.3 V_{DD}, of a DDC Interface

DDC THRESHOLD VOLTAGE, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}		TOTAL CABLE LENGTH (m)	
SUGGESTED PULL-UP RESISTANCE (kΩ)	**CABLE TYPE**	**SWITCH BOX Lcable1 + Lcable2**	**DIGITAL DISPLAY Lcable**
$R_{upsource}$ = 1.5 kΩ R_{upsink} = 47 kΩ	28-AWG DVI	11	11
	28-AWG HDMI	17	17

Applying the same methodology to the case of V_{IH} = 1.9 V and V_{IL} = 0.7 V, Table 3 summarizes the recommended cable lengths to meet the timing requirement of the DDC interface.

Table 3. Recommended Cable Lengths Under General Threshold Voltages, 1.9 V and 0.7 V, of a DDC Interface

DDC THRESHOLD VOLTAGE, V_{IH} = 1.9 V, V_{IL} = 0.7 V		TOTAL CABLE LENGTH (m)	
SUGGESTED PULL-UP RESISTANCE (kΩ)	**CABLE TYPE**	**SWITCH BOX Lcable1 + Lcable2**	**DIGITAL DISPLAY Lcable**
$R_{upsource}$ = 1.5 kΩ R_{upsink} = 47 kΩ	28-AWG DVI	16	16
	28-AWG HDMI	24	24

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TMDS341PFC	ACTIVE	TQFP	PFC	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TMDS341PFCG4	ACTIVE	TQFP	PFC	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TMDS341PFCR	ACTIVE	TQFP	PFC	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TMDS341PFCRG4	ACTIVE	TQFP	PFC	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

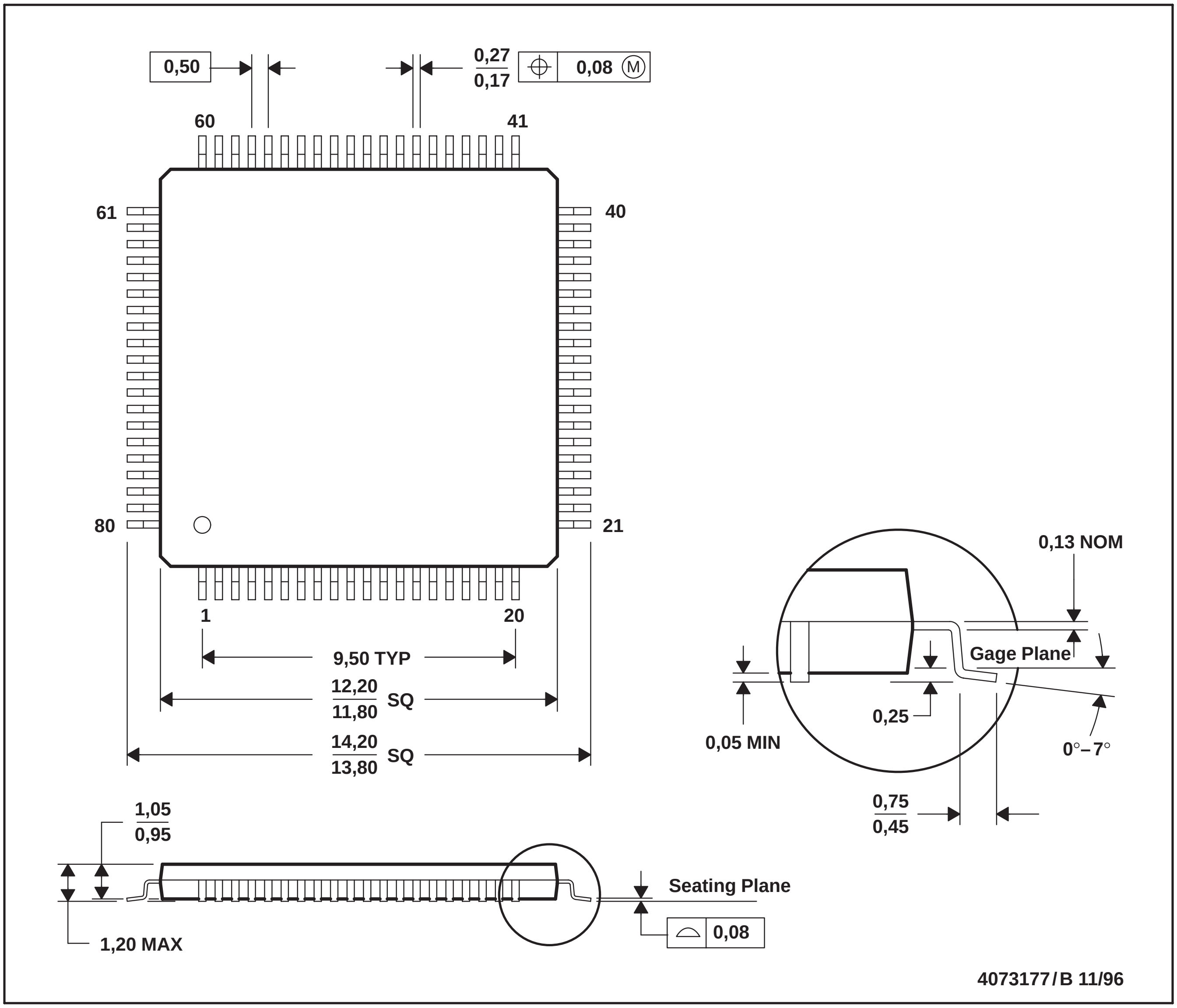
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MTQF009A – OCTOBER 1994 – REVISED DECEMBER 1996

PFC (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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