TMP107-Q1 Automotive Grade, ±0.4°C Temperature Sensor with Daisy-Chain UART, EEPROM, and Alert Function

1 Features

- AEC-Q100 Qualified with:
  - Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- High Accuracy (Without Calibration):
  - ±0.4°C (max) from –20°C to +70°C
  - ±0.55°C (max) from –40°C to +100°C
  - ±0.7°C (max) from –55°C to +125°C
- High Resolution: 14 Bits (0.015625°C)
- UART-Compatible, SMAART Wire™ Interface:
  - Allows Up To 32 Daisy-Chained Devices
- EEPROM Memory for Unique Addressing, Trip Level Programming, and General-Purpose Storage
- Continuous Conversion and Shutdown Mode for Power Savings
- One-Shot Conversion Mode for Custom Update Rates and Power Savings
- Programmable Alert Feature
- Operating Temperature Range: –55°C to +125°C
- Operating Supply Range: 1.7 V to 5.5 V
- Package: SOIC-8

2 Applications

- Battery Management Systems (BMSs)
- Distributed Temperature Sensing
- Hybrid, Electric, and Power-Train Systems
- Body Control Modules (BCMs)
- Building Automation and HVACs
- Engine Control Units
- Infotainment Processor Management
- Diesel Urea Tanks

3 Description

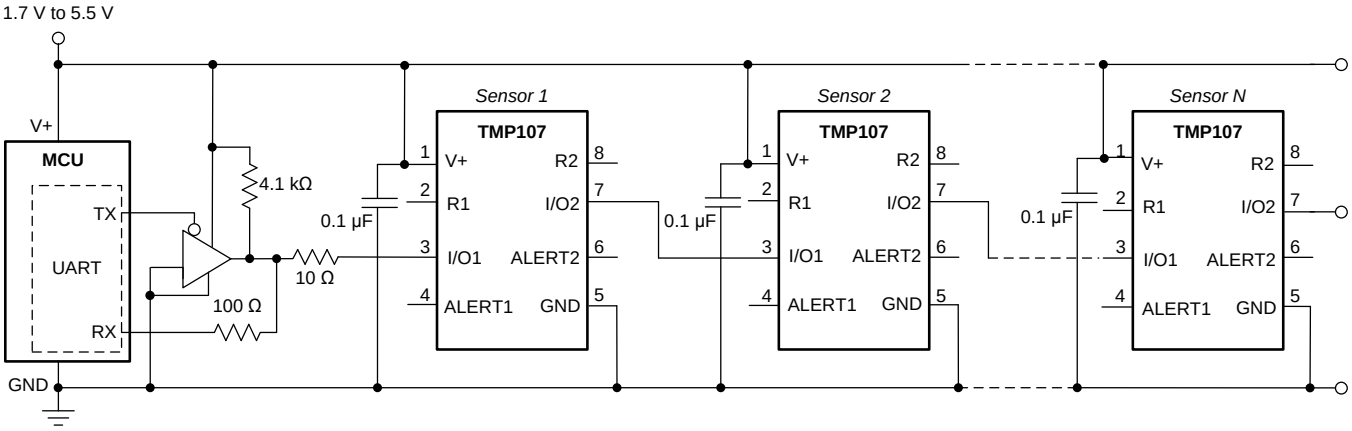
The TMP107-Q1 digital output temperature sensor supports a total of 32 daisy-chained devices. Each sensor has a unique 5-bit address stored in electrically-erasable programmable memory (EEPROM). The TMP107-Q1 is capable of reading temperatures with a resolution of 0.015625°C, and is accurate to within ±0.4°C in the range from –20°C to +70°C. The TMP107-Q1 is ideal for replacing NTC and PTC thermistors where high accuracy is required.

Device Information[1]

DEVICE NAME	PACKAGE	BODY SIZE
TMP107-Q1	SOIC (8)	4.90 mm × 3.90 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

Typical Application



All figures shown as TMP107 represent TMP107-Q1 as well.

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4 Revision History

Changes from Original (October 2015) to Revision A **Page**

- Released to production ... 1

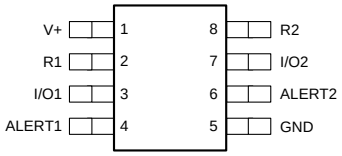
5 Description (continued)

The unique 5-bit address stored in the EEPROM is determined during the automated address assignment operation, and is based on the position of each sensor relative to the SMAART wire host. Multiple operating modes provide maximum flexibility in selecting between low power consumption for battery operation, and high update rates for real-time control applications.

The TMP107-Q1 is ideal for extended temperature measurement in a variety of industrial, instrumentation, communication, and environmental applications. The TMP107-Q1 is available in an 8-pin SOIC package and is specified for operation over a temperature range of −55°C to +125°C.

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V+	—	Supply voltage, 1.7 V to 5.5 V
2	R1	I	Built-in pullup resistor for ALERT1; float or connect to V+
3	I/O1	I/O	SMAART wire input, output 1
4	ALERT1	O	Over- and undertemperature alert. Open-drain output; internally connected to pullup resistor R1.
5	GND	—	Ground
6	ALERT2	O	Over- and undertemperature alert. Open-drain output; internally connected to pullup resistor R2.
7	I/O2	I/O	SMAART wire input, output 2
8	R2	I	Built-in pullup resistor for ALERT2; float or connect to V+

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V+			6	V
Input voltage	I/O1, I/O2	–0.3	(V+) + 0.3	V
	R1, R2	–0.3	6	
	ALERT1, ALERT2	–0.3	6	
Sink current	ALERT1, ALERT2		10	mA
Temperature	Operating junction	–55	150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V+	1.7	3.3	5.5	V
Operating free-air temperature, T_A	–55		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TMP107-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

At T_A = –55°C to 125°C and V+ = +1.7 V to +5.5 V (unless otherwise noted). Typical values at T_A = 25°C and V+ = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT						
	Temperature range		–55		125	°C
	Temperature resolution			0.015625		°C
	Temperature accuracy (error)	–20°C to +70°C; one-shot mode, bus inactive		±0.125	±0.4	°C
		–40°C to +100°C; one-shot mode, bus inactive		±0.125	±0.55	
		–55°C to +125°C; one-shot mode, bus inactive		±0.5	±0.7	
	ADC resolution			14		Bits
DIGITAL OUTPUT (ALERT1, ALERT2)						
V_{OL}	Low-level output voltage	I_{OUT} = –1 mA	0	0.02	0.4	V
I_{OH}	High-level output leakage current	V_O = V+		0.1	1	µA
R_{PU}	Pullup resistors		75	100	125	kΩ
DIGITAL INPUT/OUTPUT (I/O1, I/O2)						
V_{IH}	High-level input voltage		0.7 (V+)		(V+) + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 (V+)	V
I_{IN}	Input current	0 V < V_{IN} < (V+) + 0.3 V	–1		1	µA
V_{OL}	Low-level output voltage	I_{OUT} = –1 mA	0	0.1	0.4	V
V_{OH}	High-level output voltage	I_{OUT} = 1 mA	(V+) – 0.4	(V+) – 0.1	V+	V
	Short-circuit current	Short-circuit I/O1 and I/O2 to ground or V+, V+ = 5 V		60		mA
DEVICE TIMING						
	Conversion time	One-shot mode	12	15	18	ms
	Conversion rate	Programmable	1/16		62	Conv/s
	Device timeout time	Any communication		35	40	ms
		Global address-initialize command		1	1.25	s
EEPROM						
	Programming time	V+ > 1.8 V		7		ms
	Number of writes	V+ > 1.8 V	1000	100,000		Times
	Data retention time		10			Years
POWER SUPPLY						
V+	Operating supply range		1.7	3.3	5.5	V
		EEPROM write	1.8	3.3	5.5	V
I_Q	Quiescent current	ADC conversion on, SMAART wire bus inactive		200	400	µA
		ADC conversion on, SMAART wire bus active (bus baud rate = 57.6 kBd)		300		
		ADC conversion off, SMAART wire bus active (bus baud rate = 57.6 kBd)		100		
		1 conversion per second average, SMAART wire bus inactive		16	35	
		EEPROM write (ADC conversion off)		400		
I_{SD}	Shutdown current	SMAART wire bus inactive (I/O1, I/O2 = V+)		3.8	10	µA
	Power-on reset voltage	Supply voltage rising		1.4		V

7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
FROM HOST TO THE TMP107-Q1					
$1/t_{BAUD}$	SMAART bus baud rate	4.8		115.4	kBd
$t_{RISE} + t_{JITTER}$	SMAART bus transition from low to high + edge timing variance			15	% of (1/baud)
$t_{FALL} + t_{JITTER}$	SMAART bus transition from high to low + edge timing variance			15	% of (1/baud)
FROM THE TMP107-Q1 TO HOST OR NEXT TMP107-Q1 IN DAISY-CHAIN					
t_{JITTER}	Edge timing variance			1	µs
t_{SKEW}	Average phase shift between IO1 and IO2		33		ns
t_{RISE}	SMAART bus transition from low to high, 10-pF load		10		ns
t_{FALL}	SMAART bus transition from high to low, 10-pF load		10		ns

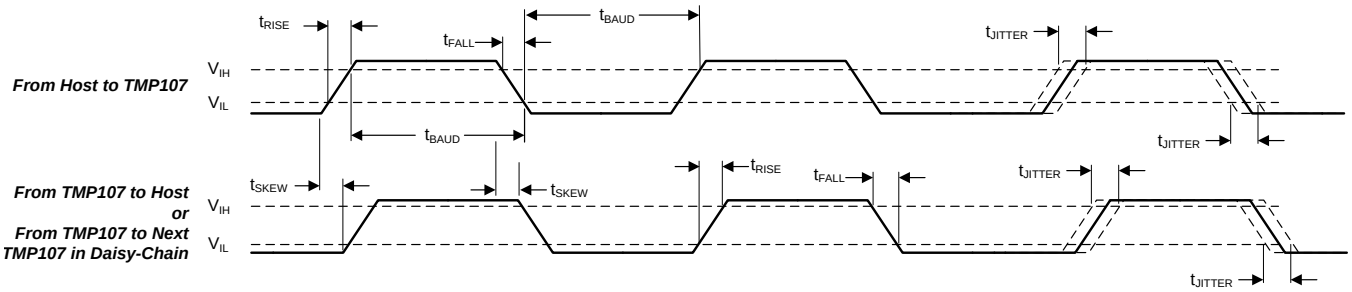
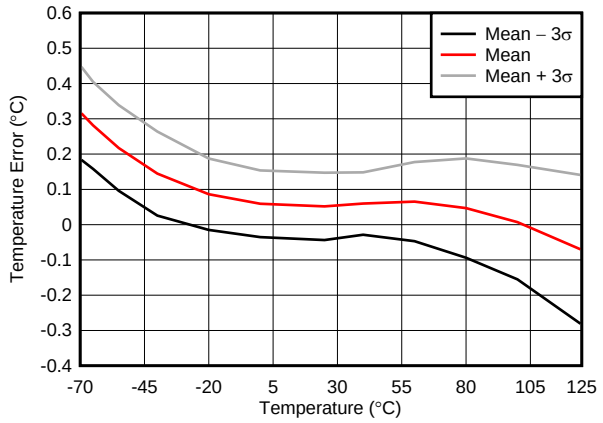


Figure 1. Timing Diagram

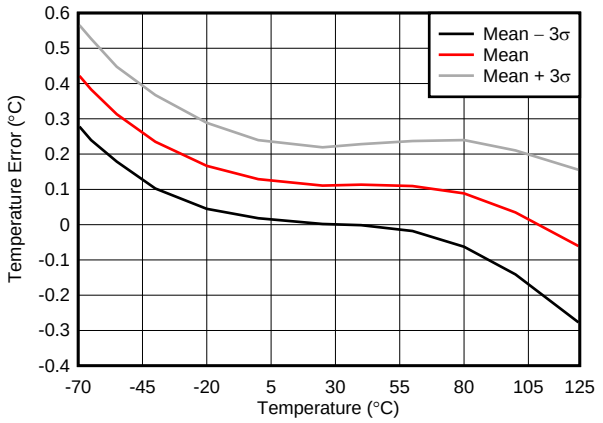
7.7 Typical Characteristics

at T_A = 25°C and V+ = 3.3 V (unless otherwise noted)



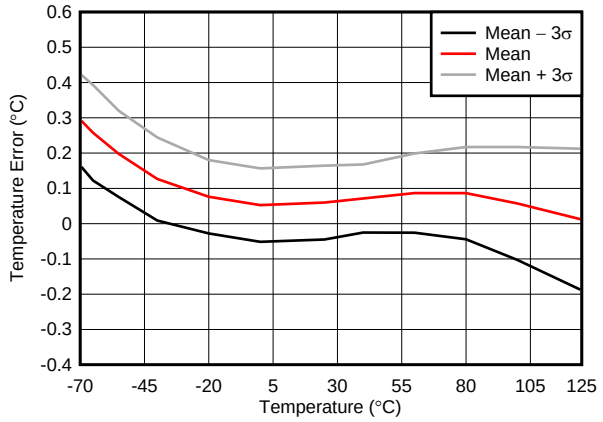
One-shot mode, specified from –55ºC to +125ºC only

Figure 2. Temperature Error vs Temperature



One-shot mode, V+ = 5.5 V, specified from –55ºC to +125ºC only

Figure 3. Temperature Error vs Temperature



One-shot mode, V+ = 1.7 V, specified from –55ºC to +125ºC only

Figure 4. Temperature Error vs Temperature

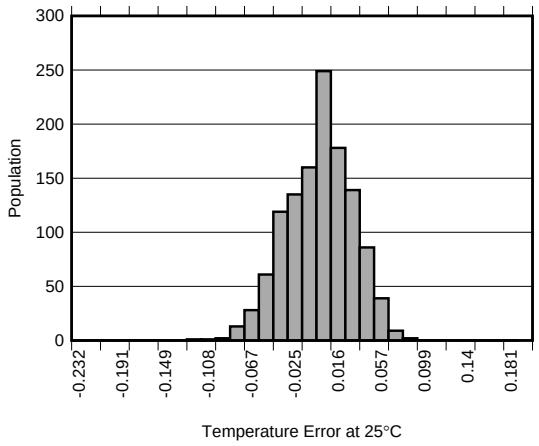
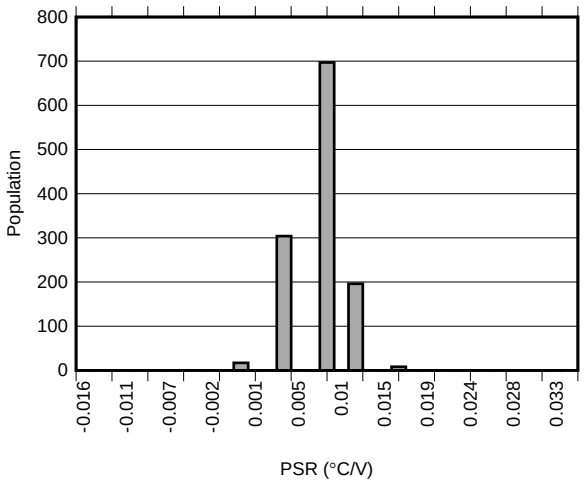
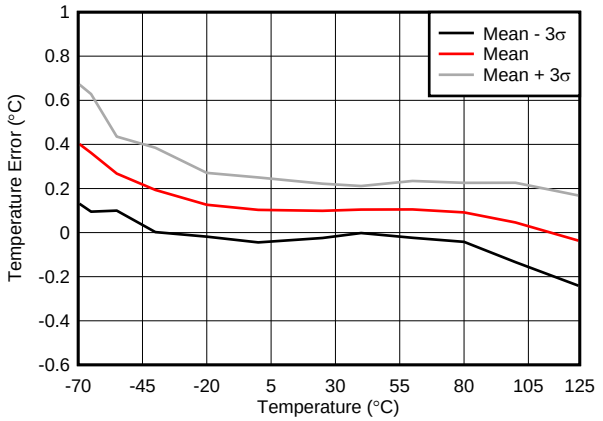


Figure 5. Temperature Error Histogram



One-shot mode, V+ = 1.7 V to 5.5 V

Figure 6. Power-Supply Rejection Histogram



Continuous-conversion mode, maximum conversion rate, bus inactive

Figure 7. Temperature Error vs Temperature

Typical Characteristics (continued)

at T_A = 25°C and V+ = 3.3 V (unless otherwise noted)

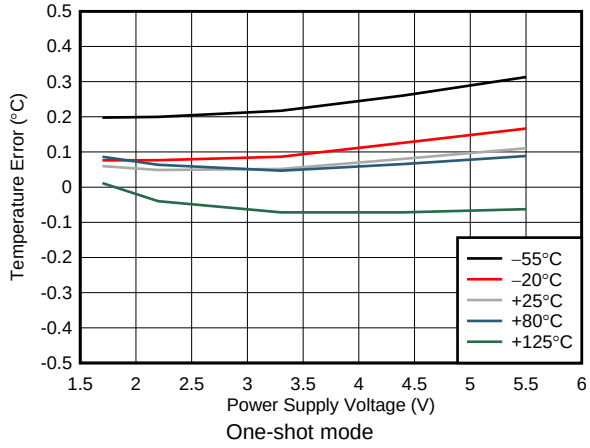


Figure 8. Temperature Error vs Power Supply Voltage

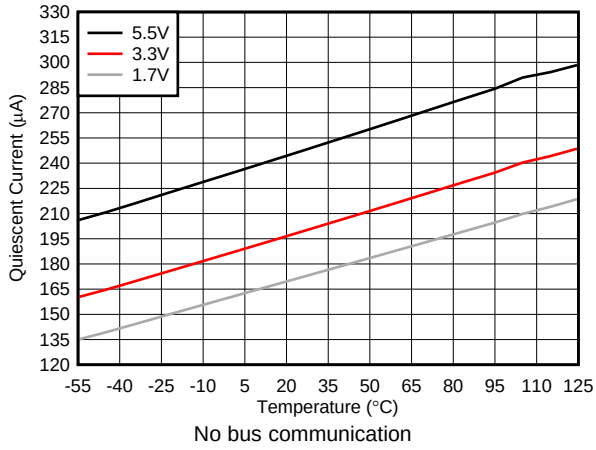


Figure 9. Continuous-Conversion Current vs Temperature

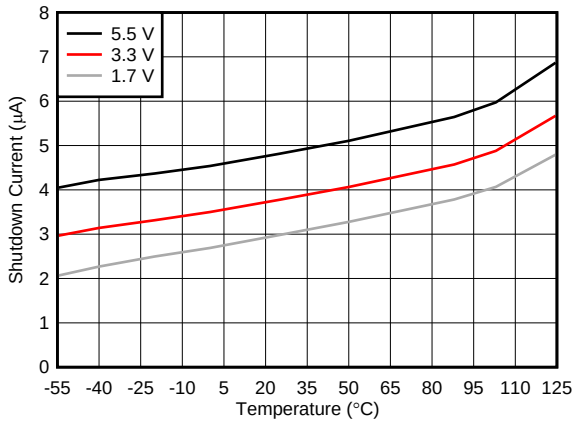


Figure 10. Shutdown Current vs Temperature

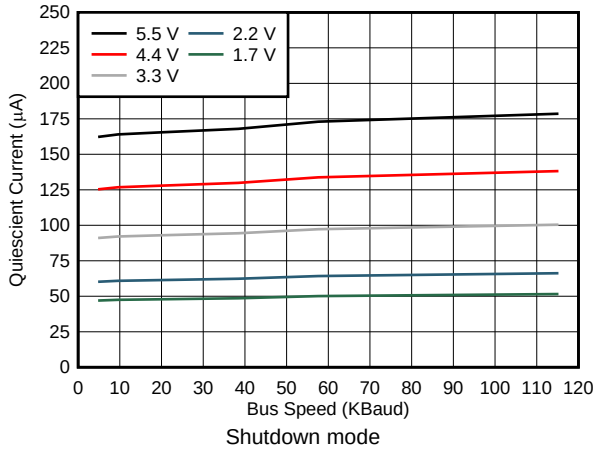


Figure 11. Quiescent Current vs SMAART Wire Bus Speed

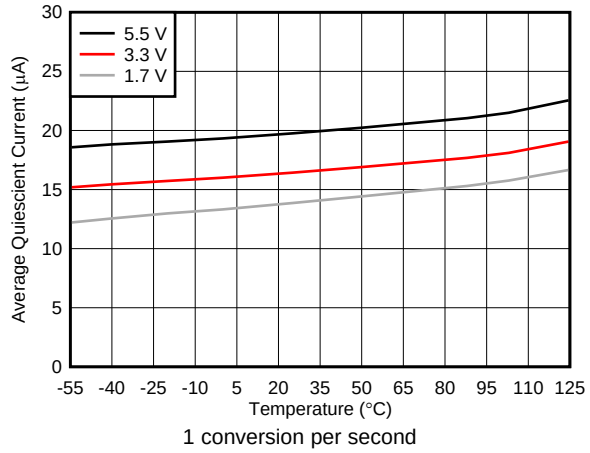


Figure 12. Average Quiescent Current vs Temperature

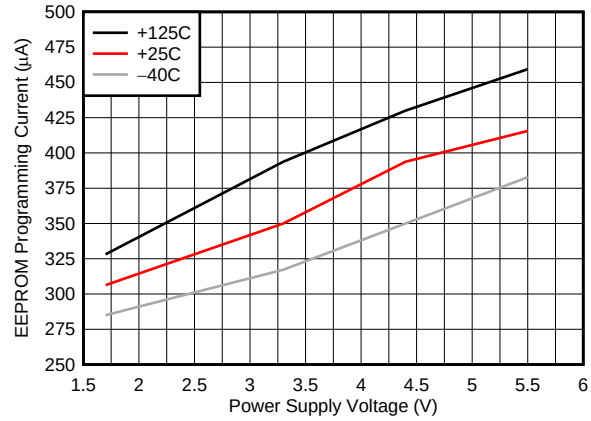


Figure 13. EEPROM Programming (Write) Current vs Power Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C and V+ = 3.3 V (unless otherwise noted)

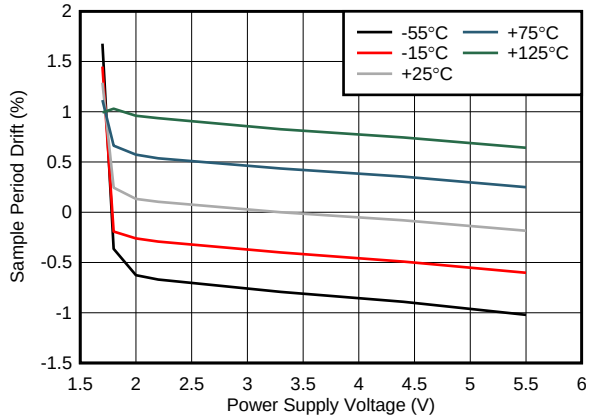


Figure 14. Sample Period Drift vs Power Supply Voltage

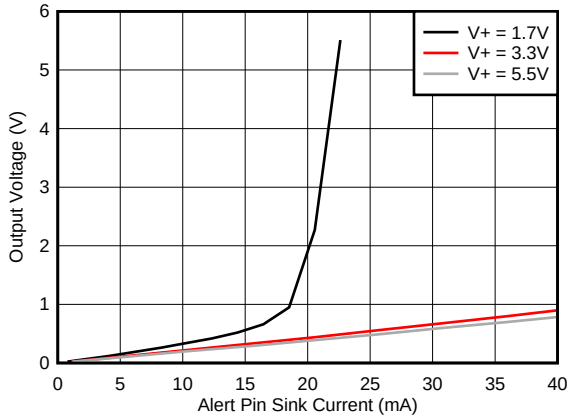


Figure 15. Alert Pin Sink Current Capability

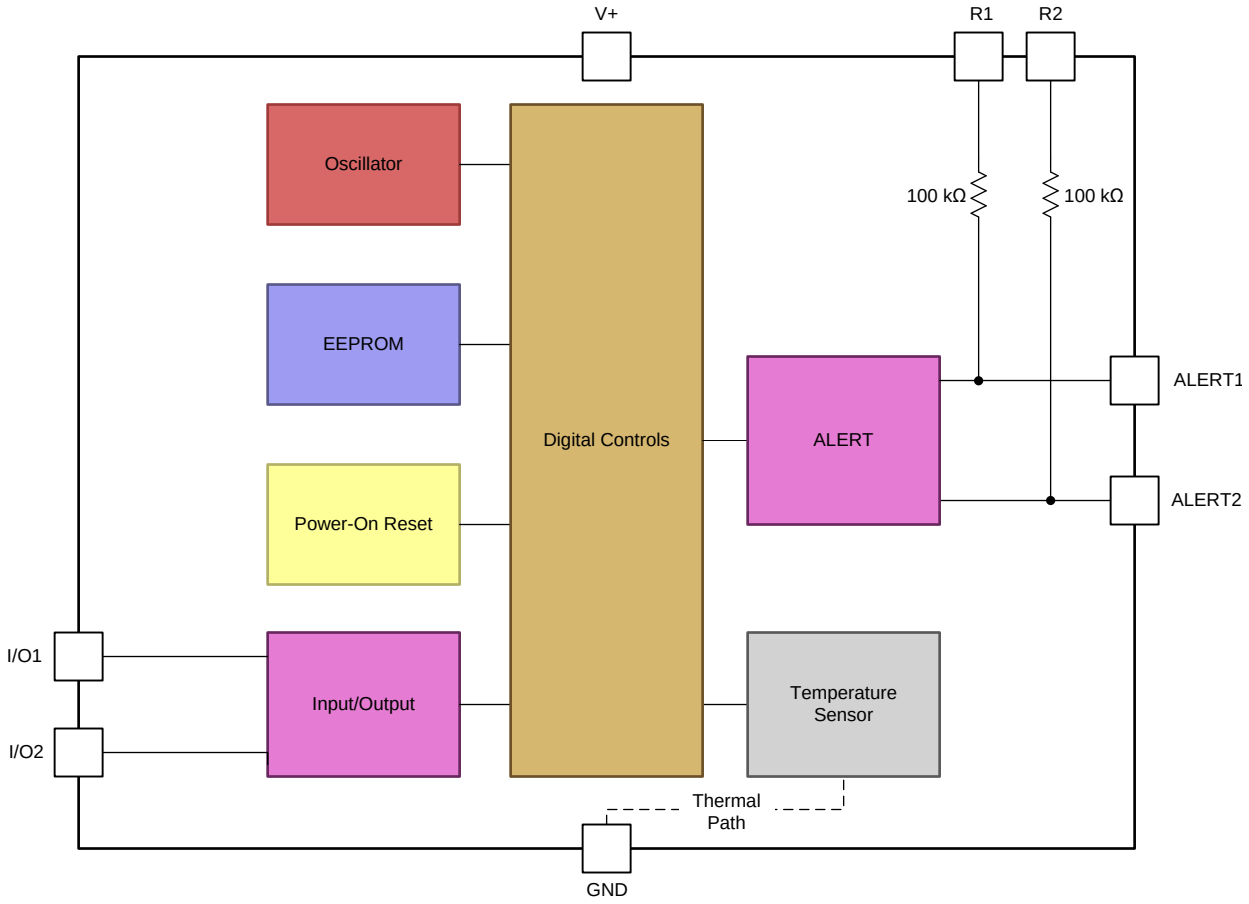
8 Detailed Description

8.1 Overview

The TMP107-Q1 is a digital temperature sensor that is optimal for thermal monitoring of large areas over long distances. The robust UART-compatible SMAART wire interface transfers data over a single wire at distances of up to 1000 feet (300 meters) between consecutive devices in the chain, and is capable of communicating in a daisy-chained configuration with up to 32 devices on a single bus.

The TMP107-Q1 supports individual commands to a specific device in the daisy chain, and also supports global commands that allow multiple TMP107-Q1s in the chain to respond to a single command.

8.2 Functional Block Diagram



NOTE: The temperature sensor of the TMP107-Q1 is the silicon chip. Thermal paths run through the package leads. The lower thermal resistance of metal enables the leads to provide the primary thermal path.

8.3 Feature Description

8.3.1 Digital Temperature Output

The 14-bit digital output from each temperature measurement conversion is stored in the temperature register. Read two bytes to obtain the data. Table 1 summarizes the temperature data format. Negative numbers are represented in binary twos complement format. The temperature sensor resolution is 0.015625ºC/LSB.

Table 1. Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
127.984	01 1111 1111 1111	1FFF
100	01 1001 0000 0000	1900
80	01 0100 0000 1000	1408
75	01 0010 1100 0000	12C0
50	00 1100 1000 0000	C80
25	00 0110 0100 0000	640
0.25	00 0000 0001 0000	10
0	00 0000 0000 0000	0
–0.25	11 1111 1111 0000	3FF0
–25	11 1001 1100 0000	39C0
–55	11 0010 0100 0000	3240

Use the following rules to obtain the data for a given temperature, and vice versa.

- *To convert positive temperatures to a digital data format*:

  Divide the temperature by the resolution. Then, convert the result to binary code with a 14-bit, left-justified format.

  Example: (50°C) / (0.015625°C / LSB) = 3200 = C80h = 00 1100 1000 0000 = C80h
- *To convert a positive digital data format to temperature*:

  Convert the 14-bit, left-justified, binary temperature result to a decimal number. Then, multiply the decimal number by the resolution to obtain the positive temperature.

  Example: 00 1100 1000 0000 = C80h = 3200 × (0.015625°C / LSB) = 50°C
- *To convert negative temperatures to a digital data format*:

  Divide the absolute value of the temperature by the resolution and convert the result to binary code with a 14-bit, left-justified format. Then, generate the twos complement of the result by complementing the binary number and adding one.

  Example: (|–25°C|) / (0.015625°C / LSB) = 1600 = 640h = 00 0110 0100 0000

  Twos complement format: 11 1001 1011 1111 + 1 = 11 1001 1100 0000 = 39C0h
- *To convert a negative digital data format to temperature*:

  Generate the twos complement of the 14-bit, left-justified binary number of the temperature result by complementing the binary number and adding one. This number is the binary representation of the absolute value of the temperature. Convert to a decimal number and multiply by the resolution to obtain the absolute temperature, then multiply by –1 for the negative sign.

  Example: 11 1001 1100 0000 has a twos complement of 00 0110 0011 1111 + 1 = 00 0110 0100 0000

  Convert to temperature: 00 0110 0100 0000 = 640h = 1600; 1600 × (0.015625°C / LSB) = 25°C = (|–25°C|); (|–25°C|) × (–1) = –25°C

8.3.2 Temperature Limits and Alert

The TMP107-Q1 has two ALERT*x* pins (ALERT1 and ALERT2) for under- and overtemperature monitor functions. Both pins have independent, dynamically-programmable limits. At the end of each conversion, the temperature result is compared with the high limit and low limit registers. If the temperature is outside the limit window, the respective ALERT*x* pin trips. There are two polarity bits that set the active state of the ALERT*x* pin. The TMP107-Q1 has two flag bits (FH*x* and FL*x*) for each alert condition to indicate in which direction the temperature has moved outside of the limit window.

There are two operating modes used for alerts and flags: *therm* and *alert*. In therm mode, the ALERT*x* pins and FH*x* and FL*x* flags are outputs of a transparent comparator. In alert mode, the ALERT*x* pins and FH*x* and FL*x* flags are latched interrupts. Select between alert mode or therm mode by using the T*x*/$\overline{\text{A}x}$ (T1/$\overline{\text{A1}}$ and T2/$\overline{\text{A2}}$) bits in the configuration register.

In alert mode (T*x*/$\overline{\text{A}x}$ = 0, default), the high and low limits form a temperature window. At the end of a conversion, if the temperature result exceeds the high limit or is less than the low limit, the respective flag (either FH*x* or FL*x*) and the ALERT*x* pin are asserted. If the alert outputs of multiple TMP107-Q1s are connected together, the TMP107-Q1 tripped alerts are still identifiable. To clear the ALERT*x* pin, issue a global alert clear *x* command, or read the configuration register as shown in Figure 16. To clear the FH*x* or FL*x* flag, read the configuration register. Alert-mode operation is shown in Figure 16.

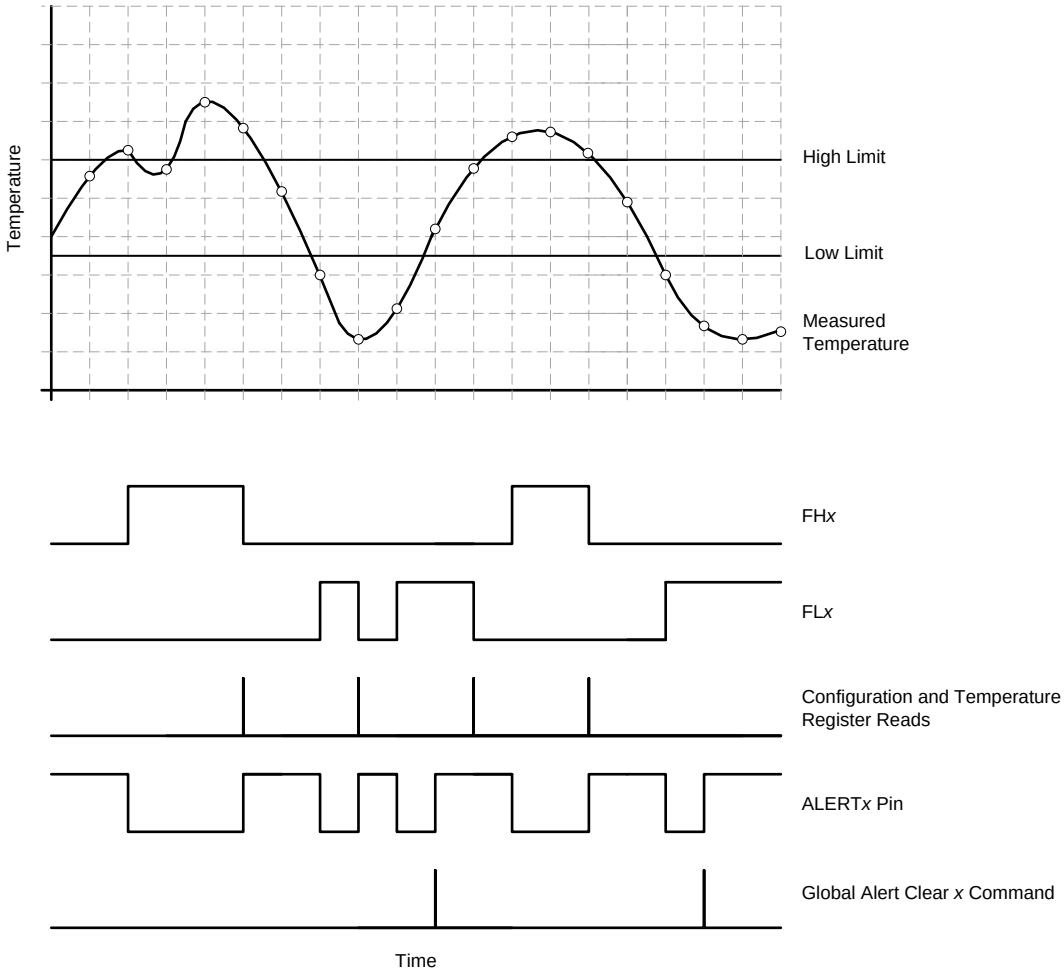


Figure 16. ALERT*x* Pin Behavior in Alert Mode (POL*x* = 0)

In therm mode (T*x*/$\overline{A}$*x* = 1), the high and low limits are used to form an upper-limit threshold detector. If the temperature result exceeds the high limit, the FH*x* flag and the ALERT*x* pin are asserted. The FH*x* flag and the ALERT*x* pin are then deasserted only after the temperature falls below the low limit. In therm mode, only the FH*x* flag is active. The FL*x* flag always reads 0. In therm mode, ALERT*x* and the flags are asserted and deasserted only at the end of a conversion and cannot be cleared by a configuration register read or global alert clear *x* command. Figure 17 shows therm-mode operation.

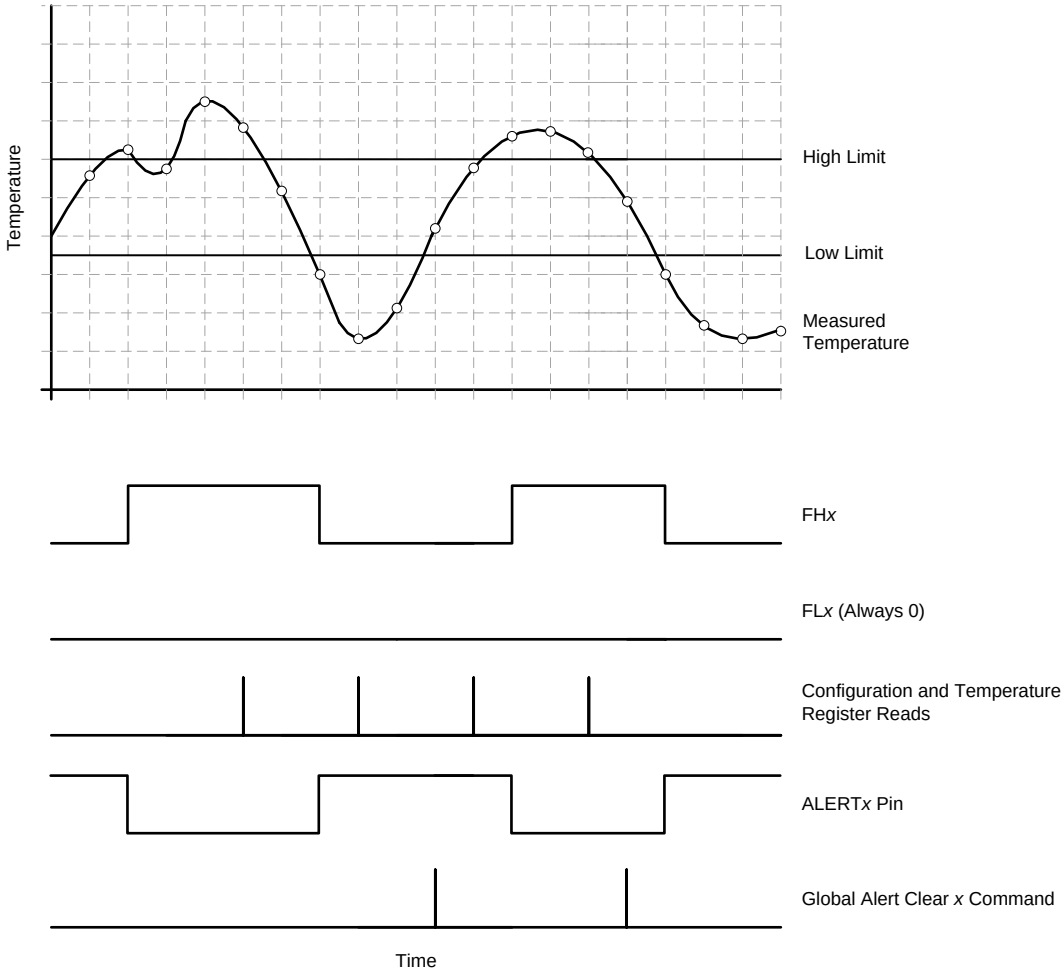


Figure 17. ALERT*x* Pin Behavior in Therm Mode (POL*x* = 0)

The limit registers default values are programmed in the EEPROM, and are acquired during power up or reset. The values can be dynamically changed by writing to the register. Disable alert and flag functionality by programming the high limit register to the highest temperature (7FFCh) and the low limit register to the lowest temperature (8000h). When disabled, the alert pins can still be controlled by polarity bits POL1 and POL2 (bit 7 and bit 3, respectively, in the configuration register) so that they work like general-purpose outputs (GPOs).

8.3.2.1 ALERT1, ALERT2, R1, and R2 Pins

ALERT1 and ALERT2 are open-drain output pins that require pullup resistors to operate properly. The TMP107-Q1 contains internal 100-kΩ pullup resistors connected between pins ALERT1 and R1, and pins ALERT2 and R2. To use the internal pullup resistors, connect pins R1 and R2 to V+, or to a voltage suitable for use with pullup resistors in the system. If external pullup resistors are used, float pins R1 and R2.

8.3.3 SMAART Wire Communication Interface

The TMP107-Q1 uses a TI proprietary, one-wire, UART-compatible, bidirectional, communication protocol called SMAART wire. It is a true one-wire communication protocol where the host can communicate with multiple daisy-chained TMP107-Q1 devices. The host device can be an off-the-shelf UART transceiver, or a microcontroller in which communication is performed by bit banging of the GPIO pins. When bit banging, follow the communication protocol format and specified parameters. All TMP107-Q1 devices have the default device addresses set to 0h.

After the devices are assembled in a daisy-chain configuration per the application requirements, the host must send the address-initialize command. This command initializes the daisy-chain so that all of the devices in the chain are assigned a unique incremental address respective to their position from the host controller (see the *Address Initialize* section for more information). The generated device addresses are stored in the internal EEPROM memory of each TMP107-Q1 in the chain. After the address initialization process is completed, the TMP107-Q1 devices restore their addresses from their respective EEPROM memories upon reset events.

After the daisy-chain is initialized with the address-initialize command operation, the host device can perform individual read and write operations to any device in the daisy chain by directly addressing that device. The host can also perform global read, global write, or global software reset operations on all devices in the daisy chain.

The inactive state of the bus is logic high. Every communication operation in the SMAART wire protocol consists of multiple 10-bit words. Each word is transferred least significant bit (LSB) first, with a start bit that is logic low in the beginning, a stop bit that is logic high in the end, and 8-bit data located between the start and stop bits. Each phase consists of one or more words that are transferred least significant word first. By using a start bit and stop bit for each word, the TMP107-Q1 devices can detect the start of every word and maintain synchronous communication. SMAART wire protocol communication is divided into two categories: address operations and command operations. Address operations are used to perform individual and multiple device read and write operations. Command operations are address initialize, last device polling, and global software reset operations.

Figure 18 shows the top-level phase sequences for the two types of operation. Detailed descriptions with timing diagrams are provided.

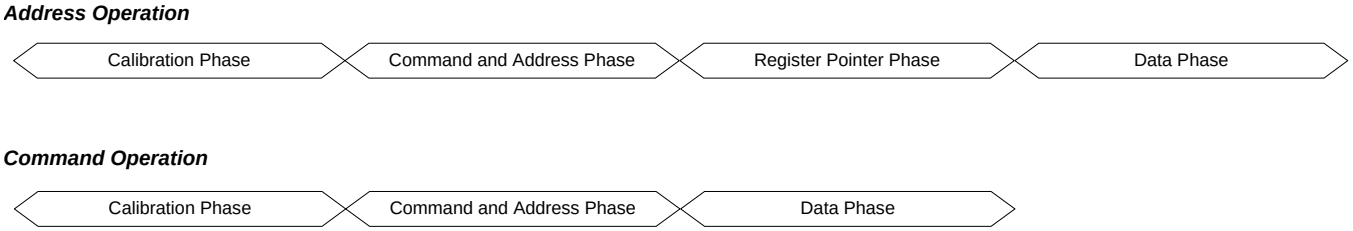


Figure 18. Address and Command Operations

8.3.3.1 Communication Protocol

Only the host initiates communication. Before communication begins, all the daisy-chained devices are in transparent mode. In this mode, all the host operations are sequentially transferred to all the devices in the chain. The devices in the chain cannot communicate with each other with the exception of the address initialize command. After initialization, the devices in the chain are in one of the following four modes:

- wait for a command from the host (default mode)
- transmit the device data back to the host
- transmit the commands from the host to the subsequent device in the chain
- transmit the data from the subsequent device back to the host

8.3.3.1.1 Calibration Phase

The calibration phase is the first phase of every communication, and consists of the host sending 10-bits, as shown in Figure 19. Pull the line low in the beginning to notify each device that the host is initiating communication. Next, the host transmits calibration sequence 55h at the desired communication baud rate. The connected devices receive this calibration byte and calculate the baud rate to communicate with the host. This calibration byte is sent at the beginning of every operation; therefore, each address or command operation can be performed at a different baud rate.

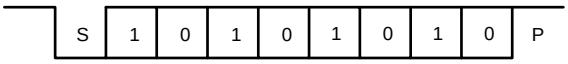


Figure 19. Calibration Phase

8.3.3.1.2 Command and Address Phase

The second phase of every communication is the command and address phase. The values of the bits in this phase determine the format and structure of subsequent phases in the communication operation. Table 2 lists the command and address phase values.

Table 2. Command and Address Phase Values

COMMAND AND ADDRESS OPERATIONS	COMMAND AND ADDRESS PHASE VALUES								HEX VALUE
	0	1	2	3	4	5	6	7	
	G/nI (LSB)	R/nW	C/nA	AC0	AC1	AC2	AC3	AC4 (MSB)	
Address initialize	1	0	1	0	1	0	0	1	95
Last device poll	1	1	1	0	1	0	1	0	57
Global software reset	1	0	1	1	1	0	1	0	5D
Global alert clear 1	1	0	1	0	1	1	0	1	B5
Global alert clear 2	1	0	1	0	1	1	1	0	75
Global read	1	1	0	A0	A1	A2	A3	A4	Varies based on A0-A4
Global write	1	0	0	A0	A1	A2	A3	A4	Varies based on A0-A4
Individual read	0	1	0	A0	A1	A2	A3	A4	Varies based on A0-A4
Individual write	0	0	0	A0	A1	A2	A3	A4	Varies based on A0-A4

8.3.3.1.2.1 Global or Individual (G/nI) Bit

The G/nI bit indicates if the communication is a global operation (intended for more than one device) or individual (intended for only one device).

All command operations are global; therefore, for command operations, always set the G/nI bit to 1.

For read and write address operations to multiple devices in the daisy chain simultaneously, set this bit to 1. To access an individual device, set the G/nI bit to 0.

During global operation, the host sets the address portion of the command to the maximum address required to perform the communication. For example, to perform a write to the high-limit register of all devices between addresses 1h to 5h in the daisy chain, set the G/nI bit to 1 and the address field to 5h. For individual accesses, set the address field to the desired device address.

8.3.3.1.2.2 Read/Write (R/nW) Bit

The R/nW bit indicates whether the operation is read or write to the TMP107-Q1 device.

8.3.3.1.2.3 Command or Address (C/nA) Bit:

The C/nA bit indicates whether the current communication is a command operation or address operation. The C/nA bit = 1 indicates a command operation. The codes for specific commands in the TMP107-Q1 are listed in Table 2. Codes other than those listed in Table 2 are reserved for factory use only.

The C/nA bit = 0 indicates an address operation. The five bits following the C/nA bit (A4 to A0) are the address bits of the device or devices that the host intends to communicate with in the chain, as shown in Figure 20.

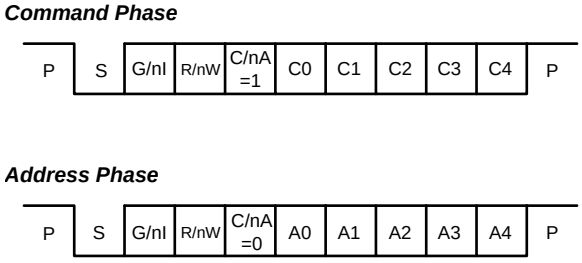


Figure 20. Command and Address Phase

8.3.3.1.3 Register Pointer Phase

The register pointer phase is provided only if the communication is an address operation. This phase of the communication shows the register pointer of the device that the host in going to write to or read from. The pointer byte has special identification code bits, as shown in Figure 21.

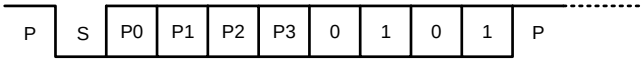


Figure 21. Register Pointer Phase

8.3.3.1.4 Data Phase

The data phase is the last phase of communication. Every register location consists of two words of data. Therefore, this last phase of communication consists of at least two bytes of data with the least significant byte sent first, followed by the most significant byte.

For a write operation, the host sends data to the device or devices at the specified register pointer location.

For a read operation, the specified device or devices respond back with the data from the location specified in the register pointer phase.

Depending on the value of G/nI bit in the command and address phase, the data in this phase are either written to a targeted individual device, or to multiple devices in the daisy-chain. Individual and global read or write operations are explained in more detail in subsequent sections. Figure 22 shows a diagram of the data phase.

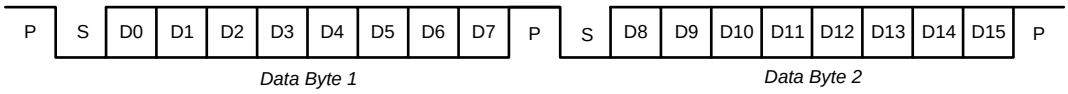


Figure 22. Data Phase for an Individual Read or Write Scenario

8.3.3.2 SMAART Wire Operations

This section describes various types of communication operations and is illustrated with timing diagrams. The diagrams in this section are used only to understand functional aspects of the communication; for timing aspects, see the *Timing Requirements* table. The color of the phases in Figure 23 through Figure 29 indicates the direction of the communication. The communication phases marked in black indicate the host controller is driving the bus. The communication phases marked in red indicate one of the devices in the daisy chain is responding to the host by driving the bus. The device communicates to the host controller through intermediate devices. The intermediate devices are automatically configured as buffers to allow data to pass through from the I/O2 pin to the I/O1 pin, and vice versa.

8.3.3.2.1 Command Operations

8.3.3.2.1.1 Address Initialize

The address-initialize command initializes the addresses of the devices in the daisy chain. This command must be performed one time because the addresses are stored in the devices EEPROM and loaded on every reset event.

After the address-initialize command phase, the host provides one word of address-assign, command-byte data, as shown in Figure 23. This word contains the desired address of the first device on the daisy chain in the A4:A0 field. Although any value from 0 to 31 is allowed for this field, it is recommended to keep first device address at 01h. The last device address must never exceed 31. After the address-assign command bytes have been transmitted by the host, the daisy chain goes through a sequence of position detection and self-programming events where the devices in the chain identify their respective locations on the bus. During this process, the host receives incremental address response data from the individual TMP107-Q1 devices in the daisy chain that indicate the point in the chain up to which the address assignment has been completed. These responses arrive at intervals of 7 ms. This procedure is represented in Figure 23.

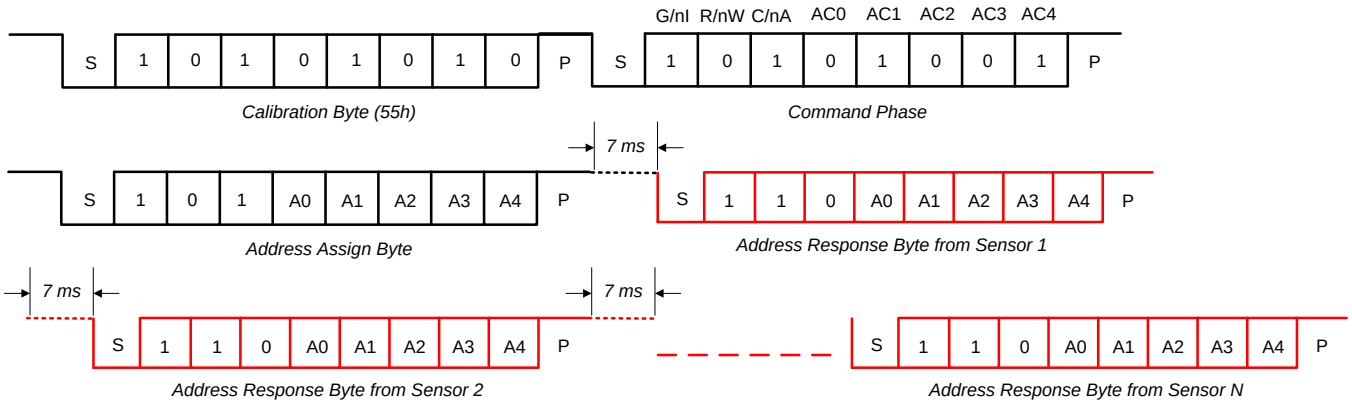


Figure 23. Address-Initialize Command

Until the initialization process is completed, daisy-chain communication is directed toward the host. Do not send any new commands to the chain during this period. If the address initialization sequence is interrupted as a result of glitches or disconnects in the daisy chain, the devices stall communication. In the event of a stall, each device has an internal timeout of one second (only for the address-initialize command). After one second, the communication interface in the TMP107-Q1 device resets, and the host regains control of the chain. Float the I/O2 pin of the last device in the chain. The address initialization procedure occurs serially from one device to the next; therefore, the maximum current consumed by the chain must not exceed the current required to initialize one device.

8.3.3.2.1.2 Last Device Poll

When the host issues a last-device-poll command, the last sensor on the initialized daisy chain responds back with the last device address, as shown in Figure 24. The last-device-poll command is also used to check if the daisy-chain address set is intact. If the daisy chain is not intact, the host does not receive a response to the last-device-poll command. This command only works if the last device in the chain was the last device during initialization. For example, if there are ten devices in the chain during address initialization and two devices are removed, running this command does not provide the host with the address of device eight. Device eight was not the last device during chain initialization, so it cannot report that device eight is the last device in the chain. In this example, the command is not answered.

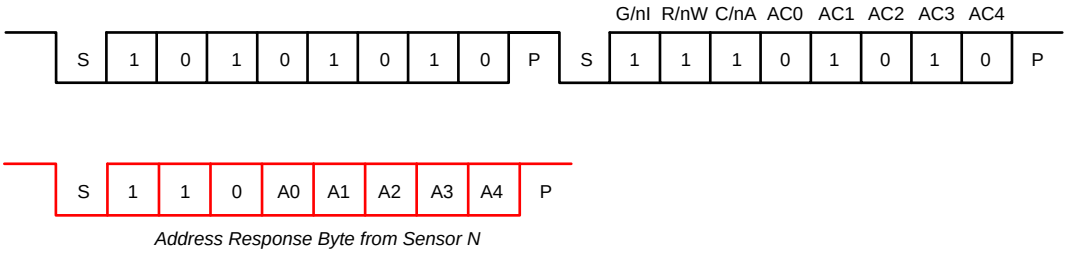


Figure 24. Last-Device-Poll Command

8.3.3.2.1.3 Global Software Reset

Use the global-software-reset command to issue a software reset to the chain in order for the devices to load the power-on reset values from EEPROM and clear the temperature result register. This command performs the same function as writing a 1 to RST (bit 1 in the configuration register). The sequence of this command is shown in Figure 25.

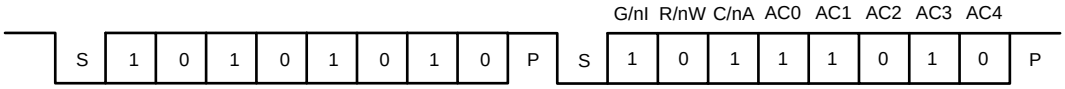


Figure 25. Global Software Reset Command

8.3.3.2 Address Operations

8.3.3.2.1 Individual Write

Use the individual write operation to write data to a specific register in a specific device in the daisy chain, as shown in Figure 26.

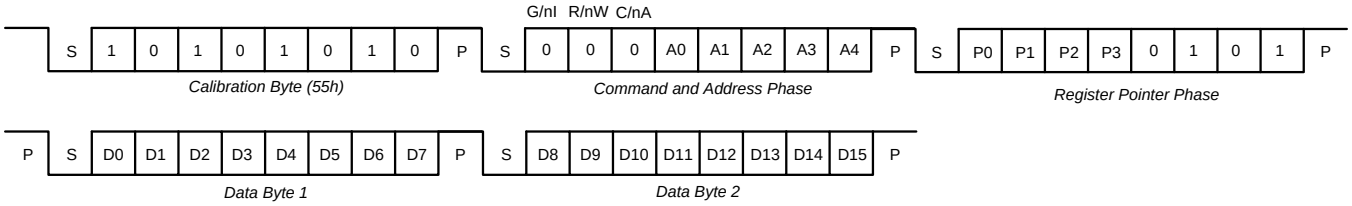


Figure 26. Individual Write Operation

8.3.3.2.2.2 Individual Read

Use the individual read operation to read the value of a register in a single device in the daisy chain, as shown in Figure 27. There is delay of up to 1.5 baud before the device responds back to the host. The host reads the data from the device by synchronizing to the falling edge of the start bit.

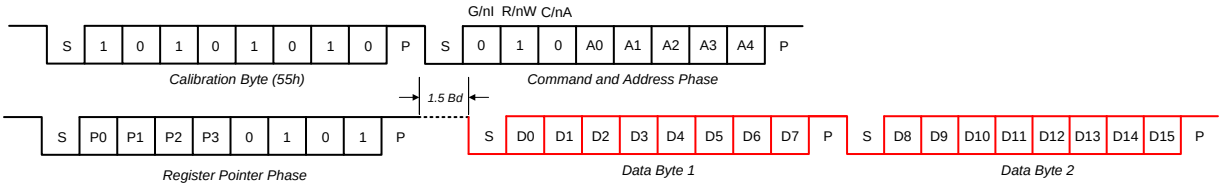


Figure 27. Individual Read Address Operation

8.3.3.2.2.3 Global Write

Use the global write operation to write data to a specific register in multiple parts. The sequence of the communication is shown in Figure 28. Data in this operation are written to the registers in all the devices from the first device to the address specified in the address field of the command and address phase.

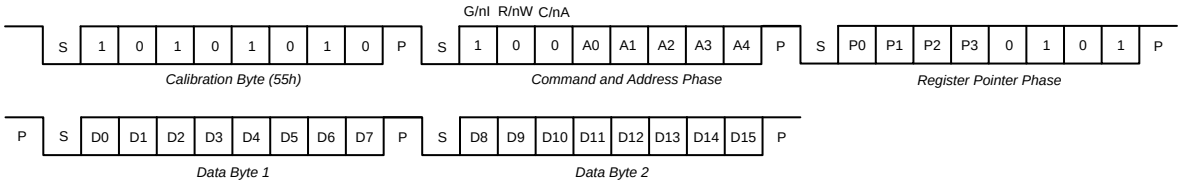


Figure 28. Global Write Operation

8.3.3.2.2.4 Global Read

Use the global read address operation to read the value of the register pointed to by the *Register Pointer Phase* section. The daisy chain returns data starting from the address specified in the command or address phase, and ending with the address of the first device in the daisy chain. The data phase of the global read address operation is different from other address operations because the data phase consists of data read back from every device on the bus between the addressed device and first device, as shown in Figure 29. If the address specified exceeds the address of the last device, the operation halts and the bus times out after 35 ms. There is a delay of up to 1.5 baud before the devices respond back to the host. The host reads the data from the devices by synchronizing to the falling edge of the start bits.

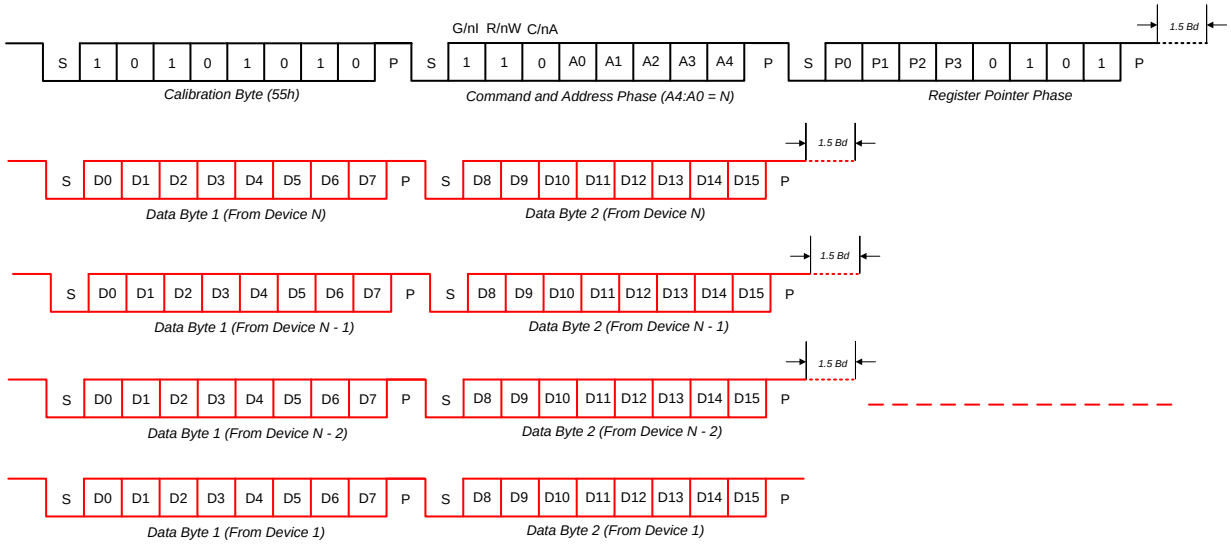


Figure 29. Global Read Operation

8.4 Device Functional Modes

8.4.1 Continuous-Conversion Mode

Continuous conversion is the default operating mode for the TMP107-Q1. In continuous-conversion mode, the TMP107-Q1 continuously measures temperature (see Table 6). After each temperature conversion, the temperature register updates with the conversion result, and the configuration register updates with the alert flags.

8.4.2 Shutdown Mode

Shutdown mode minimizes power dissipation because the TMP107-Q1 shuts down all of the internal active circuitry except for those that are required to allow communication with the device. During shutdown mode, all registers can be read from or written to. To trigger a single temperature conversion in shutdown mode, issue a one-shot command (see the *One-Shot Mode* section for more details). When the conversion is complete, the TMP107-Q1 returns to shutdown mode.

8.4.3 One-Shot Mode

One-shot mode triggers single temperature measurements by writing a 1 to OS (bit 12 in the configuration register) when the device is in shutdown mode. Following the completion of the single temperature conversion, the TMP107-Q1 returns to shutdown mode. Reading the OS bit always results in a 0. Use one-shot mode to achieve the lowest power consumption. For highest power savings and accuracy, do not communicate through the I/O bus during this mode.

8.5 Programming

8.5.1 EEPROM

The TMP107-Q1 has an internal EEPROM that is used to program and store values for writable registers, such as the configuration, high limit, and low limit registers. The EEPROM also has eight, 16-bit locations of general-purpose memory. By programming the configuration register, the EEPROM is used to store critical, system information, such as unique calibration information for the host, unique system serial ID, or a user-specific conversion rate. During the reset event, the data from the EEPROM are copied into the corresponding registers. Two registers that are not updated by the EEPROM are the temperature register and die identification register.

The electrical and timing specifications for the EEPROM are provided in the *Specifications* section. See Table 3 for the register map to the eight, internal EEPROM locations (register addresses 6h to Dh).

8.5.2 EEPROM Operations

8.5.2.1 EEPROM Unlock

After power up, the EEPROM is locked for programming by default. When locked, all writes to the EEPROM are ignored. In order to program the EEPROM, first unlock the memory for programming by writing logic 1 to NUS (bit 0 in the temperature register) using a regular write communication. EEPROM locations are readable whether locked or unlocked. Locking the EEPROM by default is a protection provided to prevent unintentional triggering of EEPROM programming during normal device operations.

8.5.2.2 EEPROM Lock

If the EEPROM is unlocked for programming, make sure to lock the EEPROM after the programming operations. Lock the EEPROM by writing logic 0 to NUS (bit 0 in the temperature register).

8.5.2.3 EEPROM Programming

After the EEPROM is unlocked, a write to any EEPROM-associated register triggers EEPROM programming. A programming event takes up to 16 ms, depending on the device conditions; therefore, space out successive commands in 16-ms write periods.

Poll BUSY (bit 1 in the temperature register) to check the EEPROM programming status. The BUSY bit = 1 when the EEPROM program is in progress. The BUSY bit = 0 after programming is complete and the EEPROM is ready for another program operation. While the EEPROM is being programmed, writes to every other register are prevented in order to protect device data from corruption until programming is complete.

When the global write operation is issued to program the EEPROM locations, all of the devices in the daisy chain specified within the address field perform the programming simultaneously. This simultaneous programming leads to an increase in current in the supply wire of the daisy chain, and may create a drop in the supply voltage. It is important to maintain the supply voltage at greater than 1.8 V during the EEPROM programming in order to program devices in the daisy chain.

8.5.2.4 EEPROM Acquire or Read

The EEPROM locations that store the power-on reset values of the registers are automatically loaded into the corresponding registers at reset. The general-purpose EEPROM locations are readable even when the EEPROM is locked. While a read is performed on an EEPROM location in the register map, there is a slightly longer delay in the stop bit (~100 µs) between the pointer phase and the phase data in the communication in order to allow the EEPROM to be read. The standard UART protocol allows for such delays when the UART transceiver is being used. The amount of current consumption from the EEPROM read is negligible compared to the current consumption from communication.

8.6 Register Map

Figure 30 shows the internal register structure of the TMP107-Q1.

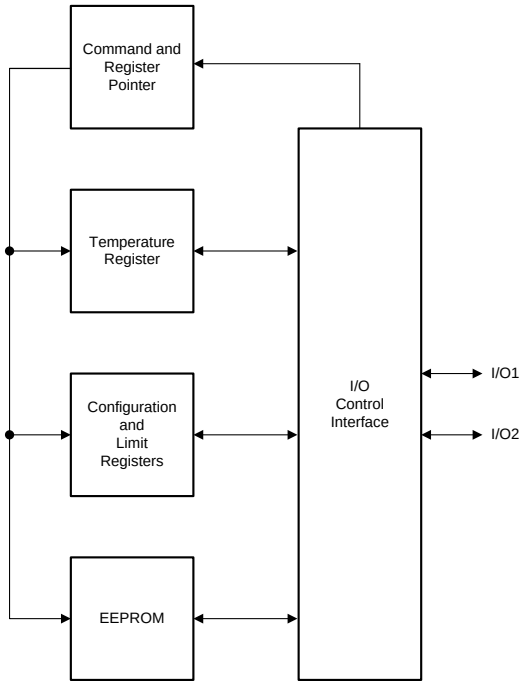


Figure 30. Register Structure

Table 3 describes the registers available with their addresses, followed by the description of the bits in each register. All register default values (except for the temperature register and die ID register) can be modified by writing to the EEPROM. All reset values listed are the factory-default values.

Table 3. Register Map and Pointer Addresses

P3	P2	P1	P0	ADDRESS (HEX)	REGISTER NAME
0	0	0	0	0h	Temperature register
0	0	0	1	1h	Configuration register
0	0	1	0	2h	High limit 1
0	0	1	1	3h	Low limit 1
0	1	0	0	4h	High limit 2
0	1	0	1	5h	Low limit 2
0	1	1	0	6h	EEPROM 1 register
0	1	1	1	7h	EEPROM 2 register
1	0	0	0	8h	EEPROM 3 register
1	0	0	1	9h	EEPROM 4 register
1	0	1	0	Ah	EEPROM 5 register
1	0	1	1	Bh	EEPROM 6 register
1	1	0	0	Ch	EEPROM 7 register
1	1	0	1	Dh	EEPROM 8 register
1	1	1	1	Fh	Die identification (read only)

8.6.1 Temperature Register (address = 0h) [reset = 0h]

The temperature register of the TMP107-Q1 is configured as a 16-bit register that stores the output of the most recent conversion and two status bits. Two bytes must be read to obtain data, and they are described in Figure 31. The upper 14 bits are used to indicate temperature. One LSB equals 0.015625°C. The temperature is represented in binary twos complement format. Following power-up or reset, the temperature register reads 0°C until the first conversion is complete. The remaining two bits indicate the EEPROM status. When the EEPROM is locked, the EEPROM cannot be programmed and all writes to the EEPROM addresses are ignored. By default, the EEPROM is locked for programming at power-on reset and must be unlocked in order to be programmed.

Figure 31. Temperature Register

15	14	13	12	11	10	9	8
T13	T12	T11	T10	T9	T8	T7	T6
R-0h							
7	6	5	4	3	2	1	0
T5	T4	T3	T2	T1	T0	BUSY	NUS
R-0h						R-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. Temperature Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	T13-T0	R	0h	Temperature result (resolution of 0.015625°C). Range: –128°C to +128°C.
1	BUSY	R	0h	This bit indicates the status of the EEPROM. 0: Indicates that the EEPROM is ready; the EEPROM has finished the last transaction and is ready to accept new commands. 1: Indicates that the EEPROM is busy completing a command and must not be given more commands. Any new commands given to the EEPROM are ignored by the EEPROM controller.
0	NUS	R/W	0h	EEPROM unlock state. 0: EEPROM locations are locked for programming. 1: EEPROM locations are unlocked for programming.

8.6.2 Configuration Register (address = 1h) [reset = A000h]

The configuration register is a read and write register used to store bits that control the part operation. The format and power-up or reset value of the configuration register for the TMP107-Q1 is shown in Figure 32 and Table 5. When the NUS bit is 0, all writes to this register are stored in register logic. When NUS is 1, then all writes to this register program the EEPROM location that stores the configuration bits. Writes to this location are followed by a 16-ms wait period for programming the EEPROM. When the configuration register is written, the current conversion is aborted and new action is taken based on the new written bits. Thus, if the TMP107-Q1 is put into shutdown, the device goes into shutdown immediately. If the conversion rate is changed, any ongoing conversion is aborted and a new conversion starts with the new conversion rate.

Figure 32. Configuration Register

15	14	13	12	11	10	9	8
CR2	CR1	CR0	OS	SD	FH1	FL1	T1/$\overline{A1}$
R/W-5h			R/W-0h	R/W-0h	R-0h	R-0h	R/W-0h
7	6	5	4	3	2	1	0
POL1	FH2	FL2	T2/$\overline{A2}$	POL2	Reserved	RST	Reserved
R/W-0h	R-0h	R-0h	R/W-0h	R/W-0h	R-0h	W-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 5. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	CR2-CR0	R/W	5h	Conversion rate. The conversion rate bits control the update rate of the analog-to-digital converter (ADC). Table 6 describes the relationship between the values of the conversion rate bits and the corresponding conversion time and average quiescent current. These bits only affect continuous-conversion mode and not one-shot mode.
12	OS	R/W	0h	One-shot mode. 0: Default. 1: Starts a single temperature conversion if the SD bit is set to 1. The TMP107-Q1 returns to the shutdown state at the completion of the single conversion. When the configuration register is read, OS always reads zero.
11	SD	R/W	0h	Shutdown mode. 0: The TMP107-Q1 is in continuous-conversion mode. 1: The TMP107-Q1 is in shutdown mode. Initiate a conversion by writing a 1 to the OS bit.
10	FH1	R	0h	High limit 1 flag. 0: Indicates that the temperature result does not exceed high limit 1. 1: Indicates when the temperature result exceeds high limit 1.
9	FL1	R	0h	Low limit 1 flag. In therm mode, this bit is not used and always reads 0. 0: In alert mode, this bit indicates that the temperature result is greater than low limit 1. 1: In alert mode, this bit indicates when the temperature result is less than low limit 1.
8	T1/$\overline{A1}$	R/W	0h	Alert and therm mode 1. 0: Alert mode: In this mode, the high limit 1 and low limit 1 form a window. If the temperature result is greater than high limit 1 or less than low limit 1, the respective flag (either FH1 or FL1) is asserted. After the flag is asserted, clear the flag by reading the configuration register. 1: Therm mode: In this mode, the limits are used to form an upper limit threshold detector. If the temperature result is greater than high limit 1, the FH1 flag is asserted. The FH1 flag is then deasserted only after the temperature drops below low limit 1. In therm mode, only the FH1 flag is active. The FL1 flag always reads 0. In this mode, the flags are asserted and deasserted only at the end of a conversion and cannot be cleared by a configuration register read.
7	POL1	R/W	0h	0: Polarity of the ALERT1 pin is active low. 1: Polarity of the ALERT1 pin is active high.
6	FH2	R	0h	High limit 2 flag. 0: Indicates that the temperature result does not exceed high limit 2. 1: Indicates when the temperature result exceeds high limit 2.
5	FL2	R	0h	Low Limit 2 Flag. In therm mode, this bit is not used and always reads 0. 0: In alert mode, this bit indicates that the temperature result is greater than low limit 2. 1: In alert mode, this bit indicates when the temperature result is less than low limit 2.

Table 5. Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	T2/$\overline{A2}$	R/W	0h	Alert and therm mode 2. 0: Alert mode: in this mode, the high limit 2 and low limit 2 form a window. If the temperature result is greater than high limit 2 or less than low limit 2, the respective flag (either FH2 or FL2) is asserted. After the flag is asserted, clear the flag by reading the configuration register. 1: Therm mode: in this mode, the limits are used to form an upper limit threshold detector. If the temperature result is greater than high limit 2, the FH2 flag is asserted. The FH2 flag is then deasserted only after the temperature drops below low limit 2. In therm mode, only the FH2 flag is active. The FL2 flag always reads 0. In this mode, the flags are asserted and deasserted only at the end of a conversion and cannot be cleared by a configuration register read.
3	POL2	R/W	0h	0: Polarity of the ALERT2 pin is active low. 1: Polarity of the ALERT2 pin is active high.
2	Reserved	R	0h	Reserved
1	RST	W	0h	Software reset. 0: Default. 1: Reset. This bit is a write-only bit and is used to perform a software reset on the TMP107-Q1.
0	Reserved	R/W	0h	Reserved

Table 6. Conversion Rates

CR2	CR1	CR0	CONVERSION PERIOD	CONVERSIONS PER SECOND	AVERAGE I_Q (V+ = 3.3 V)
0	0	0	15 ms	62	200 µA
0	0	1	50 ms	20	20 µA
0	1	0	100 ms	10	15 µA
0	1	1	250 ms	4	11 µA
1	0	0	500 ms	2	9 µA
1	0	1	1 s (default)	1 (default)	7 µA
1	1	0	4 s	0.25	6 µA
1	1	1	16 s	0.0625	5 µA

8.6.3 High Limit 1 Register (address = 2h) [reset = 7FFCh]

Figure 33. High Limit 1 Register

15	14	13	12	11	10	9	8
TH1_13	TH1_12	TH1_11	TH1_10	TH1_9	TH1_8	TH1_7	TH1_6
R/W-7Fh							
7	6	5	4	3	2	1	0
TH1_5	TH1_4	TH1_3	TH1_2	TH1_1	TH1_0	Reserved	
R/W-3Fh						R-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. High Limit 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	TH1_13-TH1_0	R/W	1FFFh	High limit for alert function 1. Resolution is 0.015625°C. Data is in twos complement form.
1-0	Reserved	R	0h	Reserved

8.6.4 Low Limit 1 Register (address = 3h) [reset = 8000h]

Figure 34. Low Limit 1 Register

15	14	13	12	11	10	9	8
TL1_13	TL1_12	TL1_11	TL1_10	TL1_9	TL1_8	TL1_7	TL1_6
R/W-80h							
7	6	5	4	3	2	1	0
TL1_5	TL1_4	TL1_3	TL1_2	TL1_1	TL1_0	Reserved	
R/W-0h						R-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. Low Limit 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	TL1_13-T1_L0	R/W	2000h	Low limit for alert function 1. Resolution is 0.015625°C. Data is in twos complement form.
1-0	Reserved	R	0h	Reserved

8.6.5 High Limit 2 Register (address = 4h) [reset = 7FFCh]

Figure 35. High Limit 2 Register

15	14	13	12	11	10	9	8
TH2_13	TH2_12	TH2_11	TH2_10	TH2_9	TH2_8	TH2_7	TH2_6
R/W-7Fh							
7	6	5	4	3	2	1	0
TH2_5	TH2_4	TH2_3	TH2_2	TH2_1	TH2_0	Reserved	
R/W-3Fh						R-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. High Limit 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	TH2_13-TH2_0	R/W	1FFFh	High limit for alert function 2. Resolution is 0.015625°C. Data is in twos complement form.
1-0	Reserved	R	0h	Reserved

8.6.6 Low Limit 2 Register (address = 5h) [reset = 8000h]

Figure 36. Low Limit 2 Register

15	14	13	12	11	10	9	8
TL2_13	TL2_12	TL2_11	TL2_10	TL2_9	TL2_8	TL2_7	TL2_6
R/W-80h							
7	6	5	4	3	2	1	0
TL2_5	TL2_4	TL2_3	TL2_2	TL2_1	TL2_0	Reserved	
R/W-0h						R-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. Low Limit 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	TL2_13-TL2_0	R/W	2000h	Low limit for alert function 2. Resolution is 0.015625°C. Data is in twos complement form.
1-0	Reserved	R	0h	Reserved

8.6.7 EEPROM *n* Register (where *n* = 1 to 8) (addresses = 6h to Dh) [reset = 0h]

Figure 37. EEPROM Register

15	14	13	12	11	10	9	8
EE*n*_15	EE*n*_14	EE*n*_13	EE*n*_12	EE*n*_11	EE*n*_10	EE*n*_9	EE*n*_8
R/W-0h							
7	6	5	4	3	2	1	0
EE*n*_7	EE*n*_6	EE*n*_5	EE*n*_4	EE*n*_3	EE*n*_2	EE*n*_1	EE*n*_0
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11. EEPROM Register bits

Bit	Field	Type	Reset	Description
15-8	EE*n*_15-EE*n*_0	R/W	0h	16-bit programable EEPROM. Only available for programming when NUS (bit 0 in the temperature register) is set to 1. Writes to this location with the NUS bit set to 0 are ignored.

8.6.8 Die ID Register (address = Fh) [reset = 1107h]

Figure 38. Die ID Register

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R-11h							
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R-07h							

LEGEND: R = Read only; -n = value after reset

Table 12. Die ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	D15 - D0	R	1107h	The die ID register is a read-only register.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

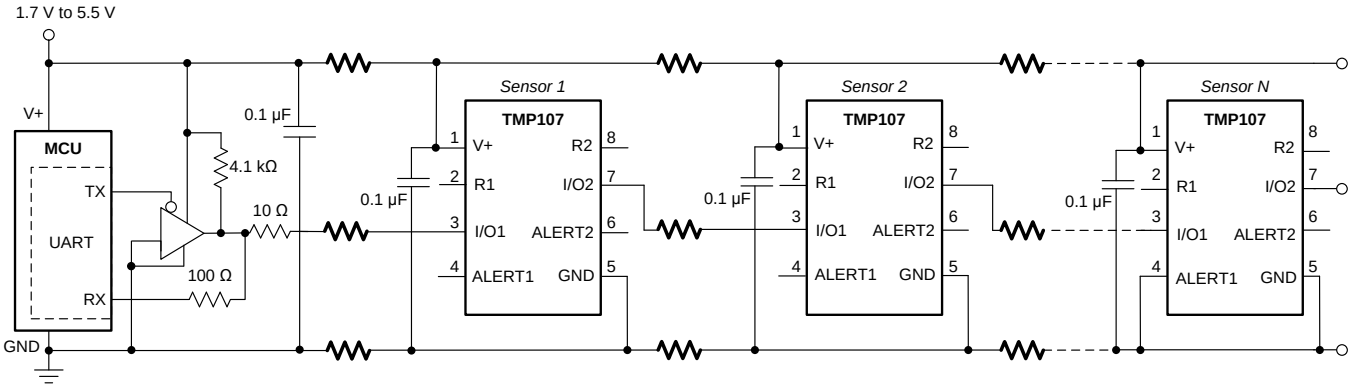
9.1 Application Information

The TMP107-Q1 is a digital temperature sensor that is optimal for thermal monitoring of large areas and over long distances between the host and the sensors. The SMAART-wire interface of the TMP107-Q1 allows for data transfer over a single wire at distances of up to 1000 feet (300 meters) between consecutive devices in the chain.

9.2 Typical Applications

9.2.1 Connecting Multiple Devices

Figure 39 shows typical connections for TMP107-Q1 devices in a daisy-chain configuration.



NOTE: **Bold** resistors represent wire resistance.

Figure 39. Connecting Multiple Devices

9.2.1.1 Design Requirements

To avoid any bus contention between the host and the TMP107-Q1 devices, use a tri-state buffer, such as the SN74LVC1G125. Use a 100-Ω resistor (typical) in series with the RX input to limit the amount of current in case of overshoot. A 10-Ω resistor (typical) between the tri-state buffer and the first TMP107-Q1 device reduces any signal collisions between the buffer and the TMP107-Q1 by limiting the amount of current flow. The pullup resistor at the output of the tri-state buffer defines the baud rate of communication. Use a 4.1-kΩ pullup resistor, as shown in Figure 39, to support the entire baud rate range specified in the *Timing Requirements*. A 0.1-µF bypass capacitor is recommended for each TMP107-Q1 device in the daisy-chain.

Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

Multiple devices are connected with cables in this typical application. The maximum cable length between two TMP107-Q1 devices can vary because of the effective resistance and capacitance of the type of cable used in a customer application.

9.2.1.2.1 Voltage Drop Effect

Take into account the voltage drop that occurs along the supply and ground lines as a result of the currents of all the devices on the line. This voltage drop occurs as a result of multiple devices simultaneously consuming current through the combined resistance of the common wire, connectors, and solder contacts. Make sure that the supply on the last device does not fall below the minimum operating supply of 1.7 V during any mode of operation, or below 1.8 V during EEPROM programming and chain initialization.

9.2.1.2.2 EEPROM Programming Current

Another parameter to consider is the EEPROM programming current. The device consumes higher current during EEPROM programming than during regular operation, as specified in the *Electrical Characteristics* section. This higher current consumption results in a larger voltage drop along the supply and ground lines and may lead to similar issues as mentioned previously. To avoid large, simultaneous, programming currents from multiple devices, program the EEPROM on the devices using the individual write commands instead of the global write commands.

9.2.1.2.3 Power Savings

In continuous-conversion mode, the TMP107-Q1 continuously measures temperature and consumes the most power out of any of the operating modes. For maximum power savings, place the TMP107-Q1 in shutdown mode. In shutdown mode, the TMP107-Q1 shuts down all internal active circuitry except for the required circuit elements that allow communication with the device. Issue a one-shot command when in shutdown mode to trigger a single temperature measurement.

9.2.1.2.4 Accuracy

In order to achieve the best temperature accuracy when multiple devices are connected in the daisy-chain, configure the devices in shutdown mode, and then issue a one-shot conversion. Read the temperature from all devices on the bus by issuing a global read after a delay of 20 ms. This delay after the one-shot command makes sure the internal ADC conversion is finished, and the voltages of the supply bypass capacitors over the daisy chain are stable, before the data are read by the host.

9.2.1.2.5 Electromagnetic Interference (EMI)

The typical, three-conductor TMP107-Q1 measurement chain is fairly insensitive to electromagnetic distortions because the supply, ground and signal wires are running in parallel and located in the same cable housing. To help maintain this insensitivity, do not make any additional electric connections at intermediate nodes in the cable, or at the end of the chain of TMP107-Q1 devices.

There can be environmental effects on a TMP107-Q1 cable implementation in the form of conducted emission. The conducted susceptibility of the cable can be investigated if this is a suspected source of interference. Designing for electromagnetic compatibility with the intended operating environment can mitigate interference. There can be radiated emission from the TMP107-Q1 cable implementation that may affect the radiated susceptibility of surrounding equipment. See specification *IEC61000-4-3: Testing and measurement techniques - Radiated, radio-frequency, electromagnetic field immunity test* for more information on testing for radiated immunity to signals in the 80-MHz to 6-GHz range. Also, see *IEC61000-4-6: Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields* for information on testing for conducted immunity in the 9-kHz to 80-MHz range.

Typical Applications (continued)

Physical shielding and electrical filtering can mitigate much of the interference into and out of the surrounding environment and electronics. See *IEC62153-4-X: Metallic Communication Cable Test Methods* for information on determining the screening effectiveness of a metallic cable shield. The thermal conductivity of additional material around the cable implementation can affect the settling time of the TMP107-Q1 at its position in the cable. This thermal conductivity can also reduce the allowable temperature range exposure of the cable implementation depending on the materials chosen. Generally, passive electrical filtering is very effective at suppressing conducted interference. Circuit board components, such as an EMI filter that increases in resistance significantly in response to higher frequency content, are widely available and often easy to implement. Even simple RC and LC filter configurations on transmission lines provide some immunity.

9.2.1.3 Application Curves

Figure 40 shows the step response of the TMP107-Q1 to a submersion in an oil bath of 100ºC from room temperature (24ºC) at a 3.3-V supply. The time-constant, or the time for the output to reach 63% of the input step, is 1.375 s. The time-constant depends on the printed circuit board (PCB) that the device is mounted on. For this test, the device is soldered to a two-layer PCB that measures 0.551 in × 0.748 in.

Figure 41 shows the TMP107-Q1 eye diagram as a measure of quality for the transmission path (cable). Measurement of eye patterns is performed by a setup where a source generates a known bit stream that is fed into a transmission channel. The eye diagram of TMP107-Q1 is taken on the I/O line at the far end of a 300-meter cable connecting two TMP107-Q1 devices. The baud rate is 9600 Kbps, and the supply voltage is set to 3.3 V. The scope is set to trigger on I/O rising (or falling) edge, with an infinite persistent time. The superimposed, captured waveforms create the eye diagram. Excellent eye diagram parameters are maintained at 9600 Kbps speed.

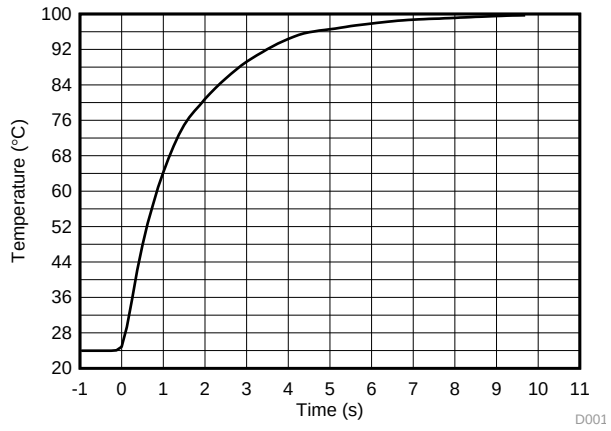


Figure 40. Temperature Step Response

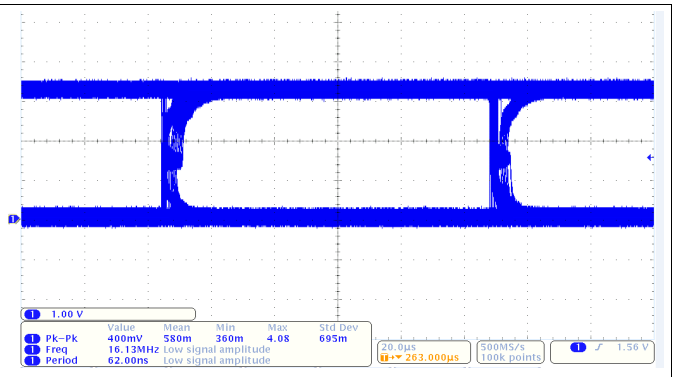


Figure 41. TMP107-Q1 Eye Diagram

Typical Applications (continued)

9.2.2 Connecting ALERT1 and ALERT2 Pins

As described in the *ALERT1, ALERT2, R1, and R2 Pins* section, the TMP107-Q1 contains internal 100-kΩ pullup resistors connected between pins ALERT1 and R1, and pins ALERT2 and R2. Connect R1 and R2 to V+ in order to enable the internal pullup resistors. Figure 42 shows a schematic example of how to connect these pins for multiple TMP107-Q1 devices in a daisy-chain configuration.

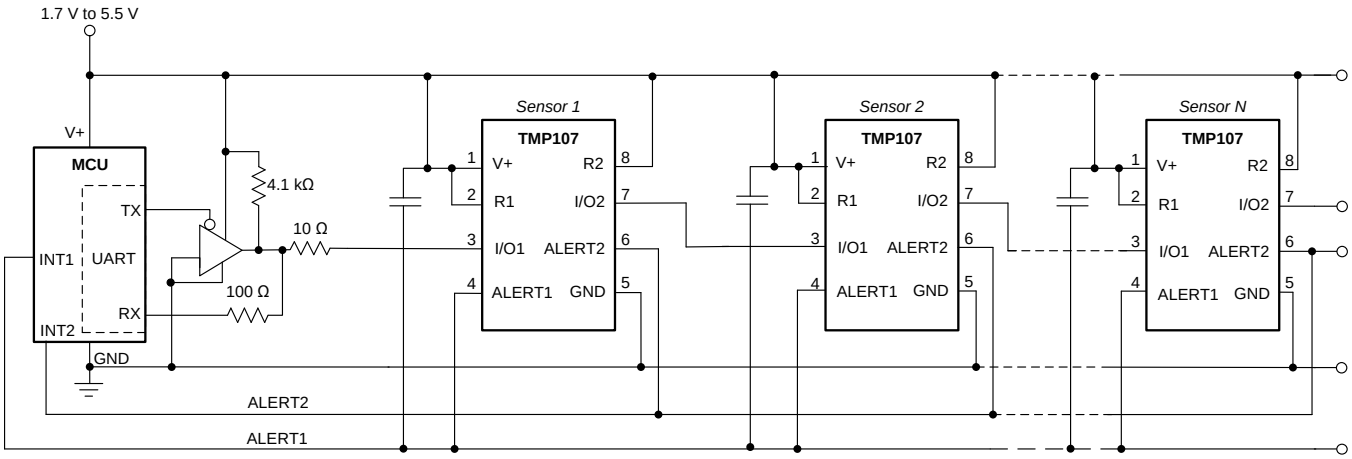


Figure 42. Connecting ALERT1 and ALERT2 Pins

9.2.3 ALERT1 and ALERT2 Pins Used as General-Purpose Output (GPO)

The TMP107-Q1 alert pins are also used as a GPO to control external switches or LEDs. This feature is useful in applications wherein the wiring between general-purpose output lines from the microcontroller or host to a control switch or LED can be eliminated by communicating through the I/O pins of TMP107-Q1. To configure the ALERT*x* pins as a GPO, program the high-limit register to the highest temperature (7FFCh) and the low-limit register to the lowest temperature (8000h). This programming disables the ALERT*x* pins from performing high- and low-limit temperature controls. The configuration register polarity bits (POL1 and POL2) are used to toggle the ALERT*x* pin output. The ALERT*x* pins are open-drain outputs; therefore, make sure the R1 and R2 pins are connected to the supply voltage, as shown in Figure 43.

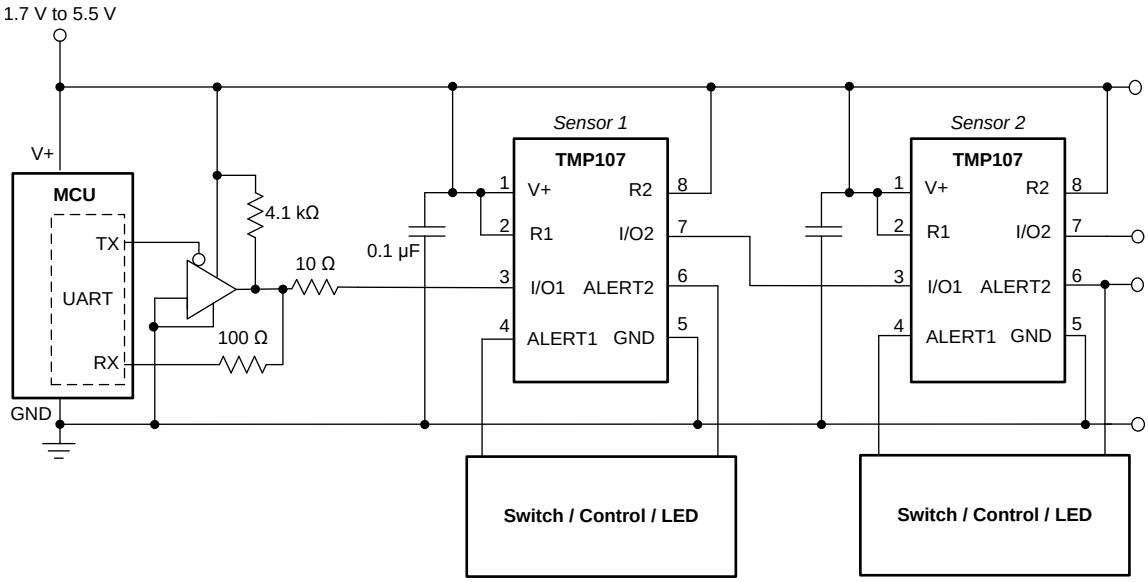


Figure 43. ALERT1 and ALERT2 Pins Used as General-Purpose Output

10 Power Supply Recommendations

The TMP107-Q1 device operates with a power supply in the range of 1.7 V to 5.5 V. The device is optimized for operation at a 3.3-V supply, but measures temperature accurately for the full supply range. For best performance, use a 0.1-µF power-supply bypass capacitor. Place the bypass capacitor as close as possible to the supply and ground pins of the device. Applications with noisy or high-impedance power supplies may require additional bypass capacitors to reject power-supply noise.

11 Layout

11.1 Layout Guidelines

Mount the TMP107-Q1 to a PCB as shown in Figure 44. Obtaining acceptable performance with alternate layout schemes is possible, however this layout produces good results and is intended as a guideline.

- Bypass the V+ pin to ground with a low-ESR ceramic bypass-capacitor. The typical recommended bypass capacitance is a 0.1-µF ceramic capacitor with a X5R or X7R dielectric. The optimum placement is closest to the V+ and GND pins of the device. Take care to minimize the loop area formed by the bypass-capacitor connection, the V+ pin, and the GND pin of the IC.
- Use larger copper area pads to reduce self-heating and lower thermal resistance to the environment.
- If possible, use PCB boards with thick copper layers.
- If possible, do not use stain to protect the IC because stain can increase thermal resistance.

11.2 Layout Example

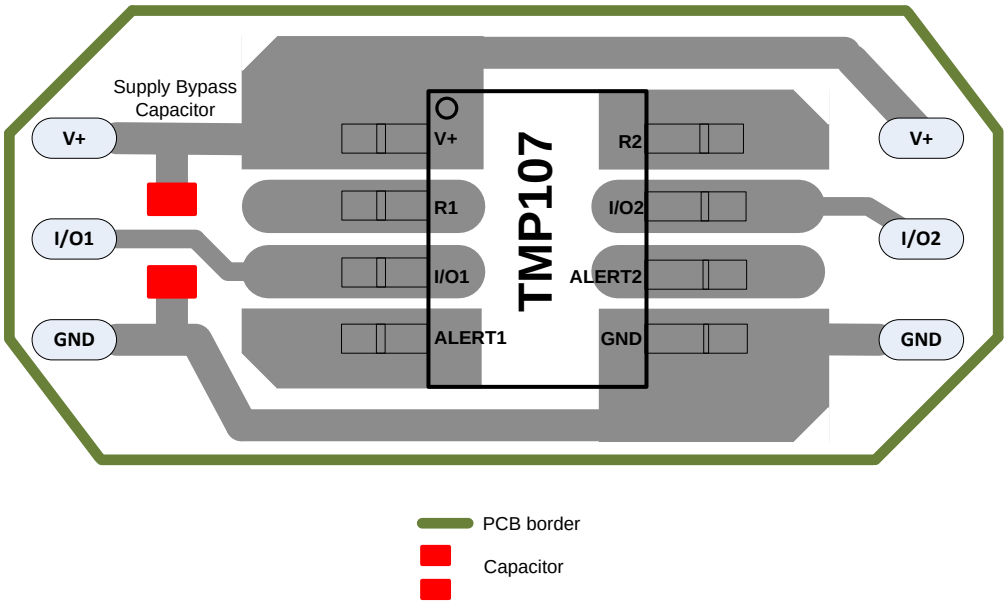


Figure 44. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

- TMP107EVM User's Guide, SBOU158
- SN74LVC1G125 Data Sheet, SCES223

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP107BQDQ1	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-2-260C-1 YEAR	-40 to 125	T107BQ	Samples
TMP107BQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-2-260C-1 YEAR	-40 to 125	T107BQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

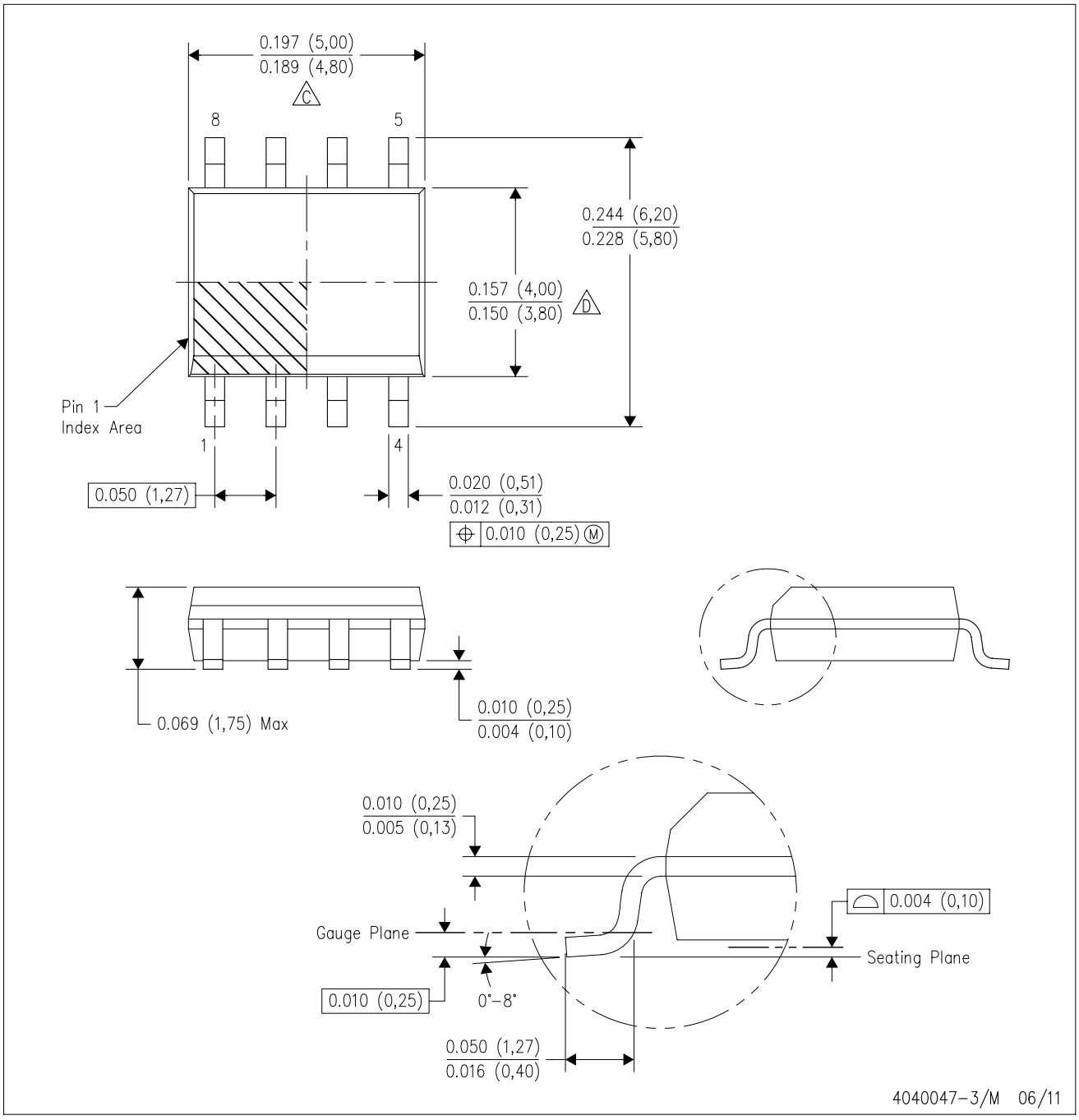
OTHER QUALIFIED VERSIONS OF TMP107-Q1 :

- Catalog: TMP107

NOTE: Qualified Version Definitions:

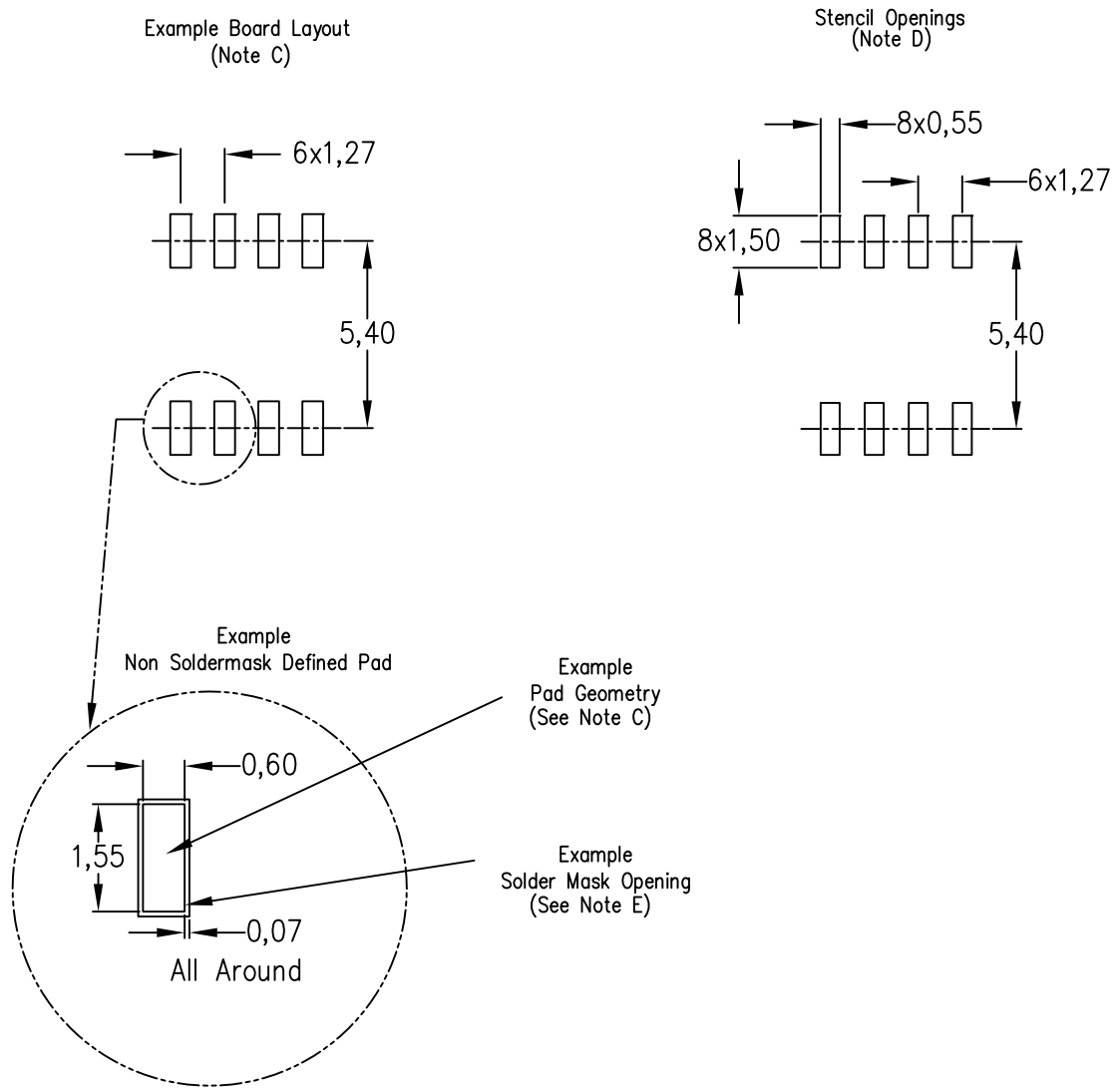
- Catalog - TI's standard catalog product

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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