1.5°C ACCURATE PROGRAMMABLE DIGITAL TEMPERATURE SENSORS WITH SPI™ INTERFACE

FEATURES

- **Digital Output: SPI-Compatible Interface**
- **Programmable Resolution: 9 to 12 Bits + Sign**
- **Aaccuracy: ±1.5°C from -25°C to 85°C (max)**
  ±2.0°C from -55°C to 125°C (max)
- **Low Quiescent Current: 50 μA**
- **Wide Supply Range: 2.7 V to 5.5 V**
- **Tiny SOT23-6 Package**
- **Operation to 150°C**
- **Programmable High/Low Setpoints**

APPLICATIONS

- **Power-Supply Temperature Monitoring**
- **Computer Peripheral Thermal Protection**
- **Notebook Computers**
- **Cell Phones**
- **Battery Management**
- **Office Machines**
- **Thermostat Controls**
- **Environmental Monitoring and HVAC**
- **Electromechanical Device Temperature**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

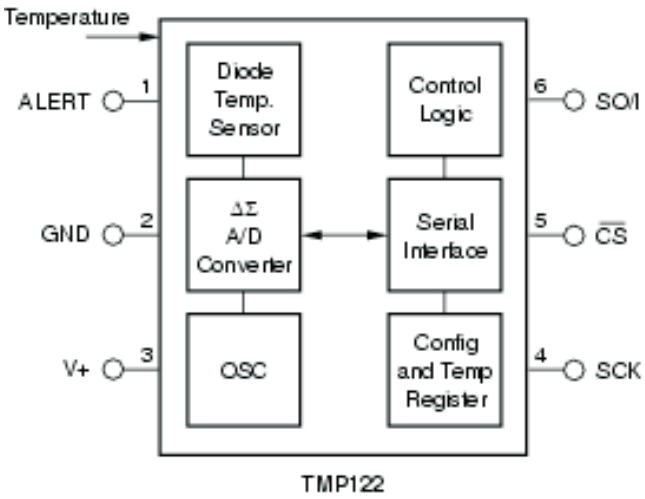
- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Additional temperature ranges are available - contact factory

DESCRIPTION

The TMP122 is an SPI-compatible temperature sensor available in an SOT23-6 package. Requiring only a pull-up resistor for complete function, the TMP122 temperature sensor is capable of measuring temperatures within 2°C of accuracy over a temperature range of -55°C to 125°C, with operation up to 150°C. Programmable resolution, programmable set points and shut down function provide versatility for any application. Low supply current and a supply range from 2.7 V to 5.5 V make the TMP122 an excellent candidate for low-power applications.

The TMP122 is ideal for extended thermal measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications.



TMP122

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SPI is a trademark of Motorola.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOT23-6	Tape and reel of 250	TMP122AMDBVTEP	122E

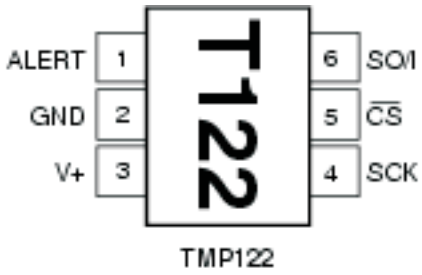
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V+	Power supply	7	V
V_I	Input voltage	-0.3 to 7	V
	Inout current	10	mA
	Operating temperature range	-55 to 150	°C
	Storage temperature range	-60 to 150	°C
T_J (max)	Junction temperature	150	°C
	Lead temperature (soldering)	300	°C

PIN CONFIGURATION



TMP122

ELECTRICAL CHARACTERISTICS

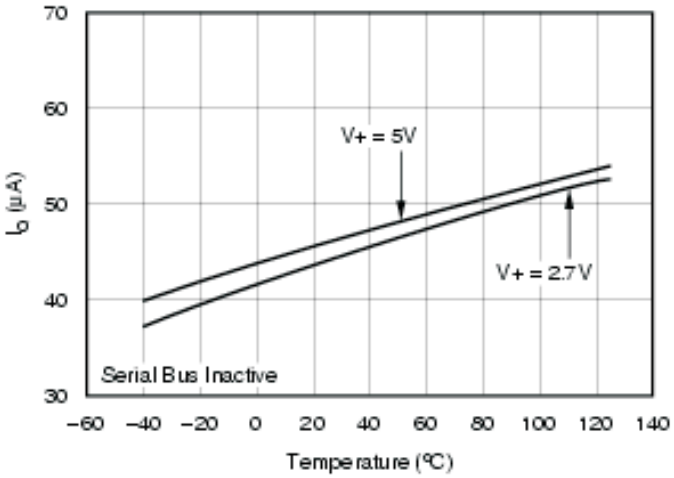
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temperature input	Range		-55		125	°C
	Accuracy (temperature error)	-25°C to 85°C		±0.5	±1.5	°C
		-55°C to 125°C		±1.0	±2.0	
		-55°C to 150°C		±1.5		
	vs supply			0.1		°C/V
	Resolution(1)	Selectable		±0.0625		°C
Digital input/output	V_{IH}		0.7 (V+)			V
	V_{IL}				0.3 (V+)	V
	Input current, SO/I, SCK, $\overline{CS}$	0 V ≤ V_{IN} ≤ V+			±1	µA
	V_{OL} SO/I	I_{SINK} = 3mA			0.4	V
	V_{OH} SO/I	I_{SOURCE} = 2mA	(V+) - 0.4			V
	V_{OL} ALERT	I_{SINK} = 4mA			0.4	V
	Leakage current ALERT	0 V ≤ V_{IN} ≤ 6 V			±1	µA
	Input capacitance, SO/I, SCK, $\overline{CS}$, ALERT			2.5		pF
	Reolution	Selectable		9 to 12 + sign		bits
	Conversion time	9 bit + sign		30	40	ms
		10 bit + sign		60	80	
		11 bit + sign		120	160	
		12 bit + sign		240	320	
Power supply	Operating range		2.7		5.5	V
	Quiescent current I_Q	Serial bus inactive		50	75	µA
	Shutdown current I_{SD}	Serial bus inactive		0.1	1	
Temperature range	Specified range		-55		125	°C
	Operating range		-55		150	
	Storage range		-60		150	
	Thermal resistance, θ_{JA}	SOT23-6 surface-mount		200		°C/W

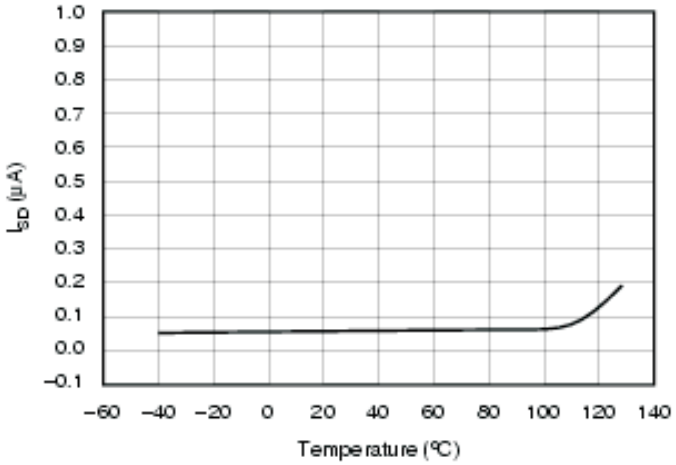
(1) Specified for 12-bit resolution.

TYPICAL CHARACTERISTICS

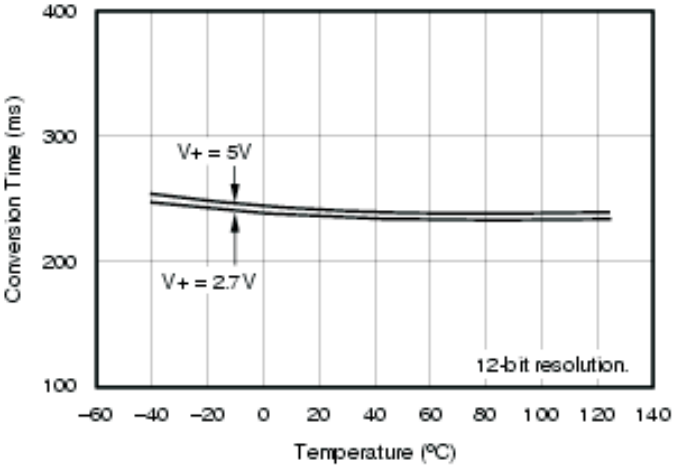
QUIESCENT CURRENT vs TEMPERATURE



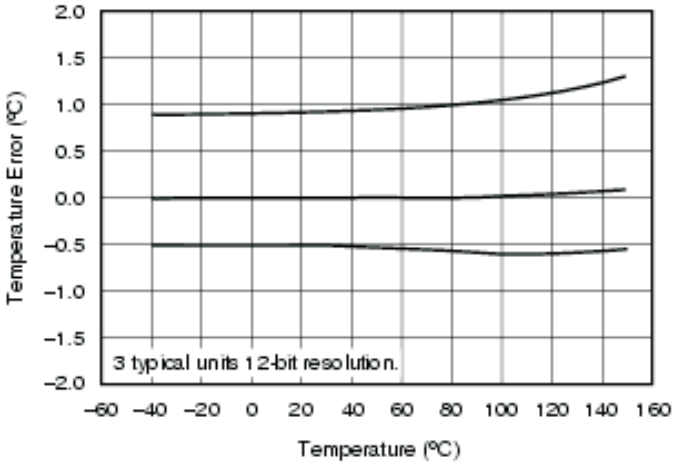
SHUTDOWN CURRENT vs TEMPERATURE



CONVERSION TIME vs TEMPERATURE



TEMPERATURE ACCURACY vs TEMPERATURE



APPLICATION INFORMATION

The TMP122 digital temperature sensor is optimal for thermal management and thermal protection applications. The TMP122 is SPI interface-compatible and specified for a temperature range of -55°C to 125°C.

The TMP122 requires minimal external components for operation, needing only a pullup resistor on the ALERT pin and a bypass capacitor on the supply. Bypass capacitors of 0.1 µF is recommended. Figure 1 shows typical connections for the TMP122.

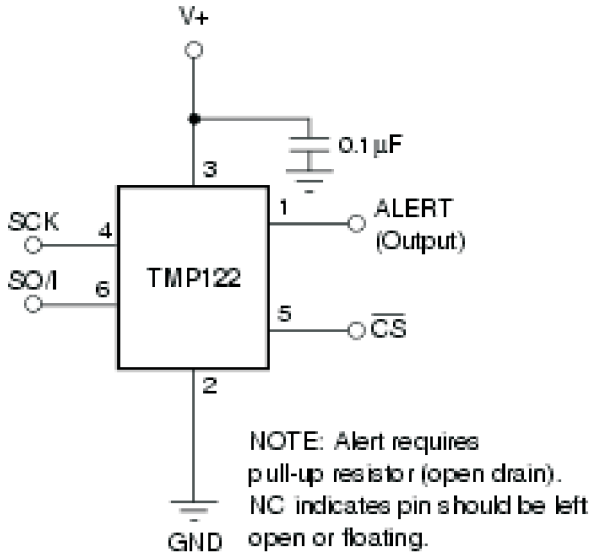


Figure 1. Typical Connections

To maintain accuracy in applications requiring air or surface temperature measurement, care should be taken to isolate the package and leads from ambient air temperature.

Figure 2. Multiple Command Sequence

COMMUNICATING WITH THE TMP122

The TMP122 converts continuously. If $\overline{CS}$ is brought low during a conversion the conversion process continues, but the last completed conversion is available at the output register. Communication with the TMP122 is initiated by pulling $\overline{CS}$ low. The first 16 clocks of data transfer will return temperature data from the temperature sensors. The 16-bit data word is clocked out sign bit first, followed by the MSB. Any portion of the 16-bit word may be read before raising $\overline{CS}$. If the user wishes to continue with $\overline{CS}$ low, the following 16 clocks transfer in a READ or WRITE command. READ and WRITE commands are described in Table 1 and Table 2.

The READ command contains an embedded address in bits D4 and D3 to identify which register to read. Bits D4 and D3 are internally registered and will hold their value following a READ command until an entire 16-bit read is completed by the user. The completion of the 16-bit READ acknowledges that the READ command has been completed. If the user issues a READ command and then raises $\overline{CS}$ with less than 16 subsequent clocks, the data from that register will be available at the next fall of $\overline{CS}$. Teh registered READ address will remain in effect until a full 16 clocks have been received. After the compleation of a 16-bit READ from the part, the READ address is reset to return data from the Temperature Register. A WRITE command to a register will not change the READ address registered. For further discussion on the READ address register, see the *Read Address Register* section.

Multiple commands may be strung together as illustrated in Figure 2. The TMP122 accepts commands alternating with 16-bit response data. On lowering $\overline{CS}$, the part always responds with a READ from the address location indicated by the READ address register. If the next command is a READ command then data is returned from the address specified by the READ command with the 16th clock resetting the READ address register to the default temperature register. The TMP122 then expects a 16-bit command. If the command is a WRITE command, then the 16 clocks following the command will again return temperature data.

Figure 3, Figure 4, Figure 5, and Figure 6 detail the communication sequences.

Table 1. READ Command

READ Command	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Temperature	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Configuration register	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Low temperature threshold	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
High temperature threshold	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

Table 2. WRITE Command

WRITE Command	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Temperature	0	0	0	0	D1	D0	R1	R0	F1	F0	POL	TM1	TM0	0	1	0
Low temperature threshold	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	1	0	0
High temperature threshold	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	1	1	0
Shutdown command	x	x	x	x	x	x	x	x	1	1	1	1	1	1	1	1

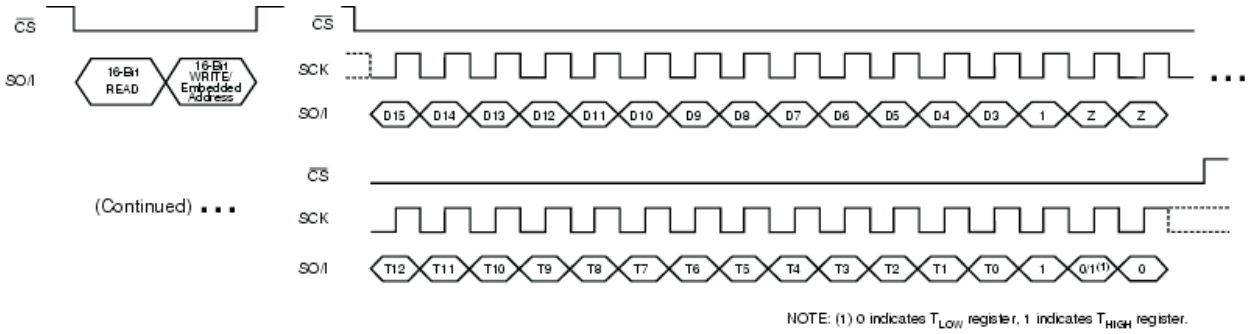


Figure 3. READ followed by WRITE Command to T_{LOW}/T_{HIGH} Register

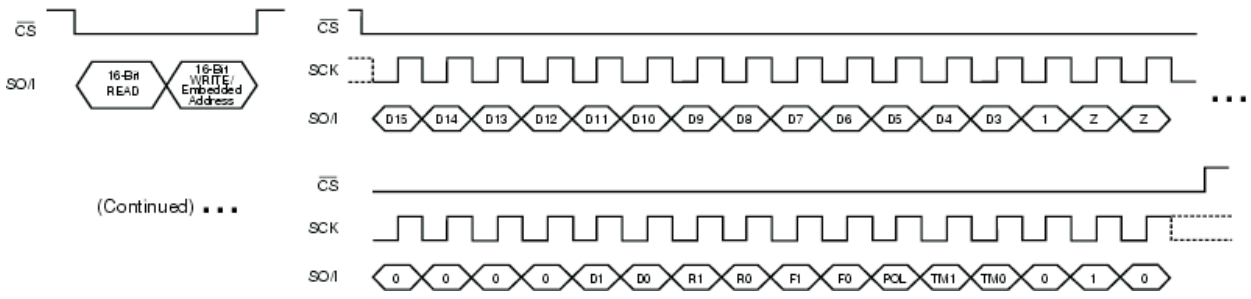


Figure 4. READ followed by WRITE Command to Configuration Register

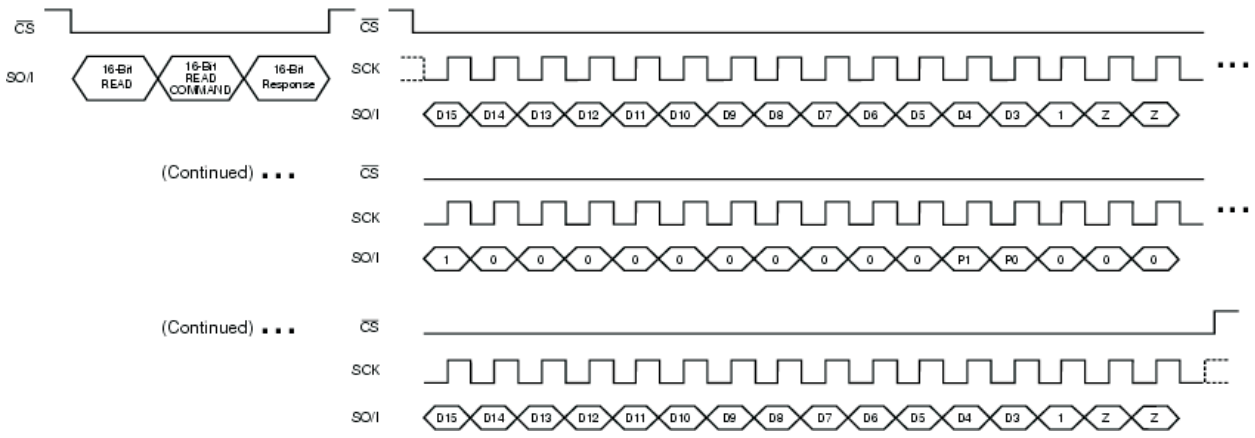


Figure 5. READ followed by READ Command and Response

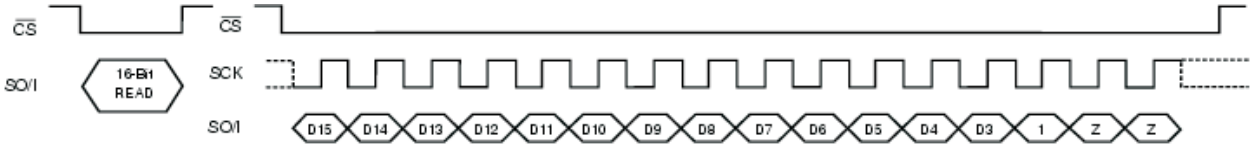


Figure 6. Data READ

READ ADDRESS REGISTER

Figure 7 shows the internal register structure of the TMP122/TMP124. Table III describes the addresses of the registers available. The READ address register uses the two bits to identify which of the data registers should respond to a read command. Following a complete 16-bit read, the READ address register is reset to the default power-up state of P1/P0 equal 0/0.

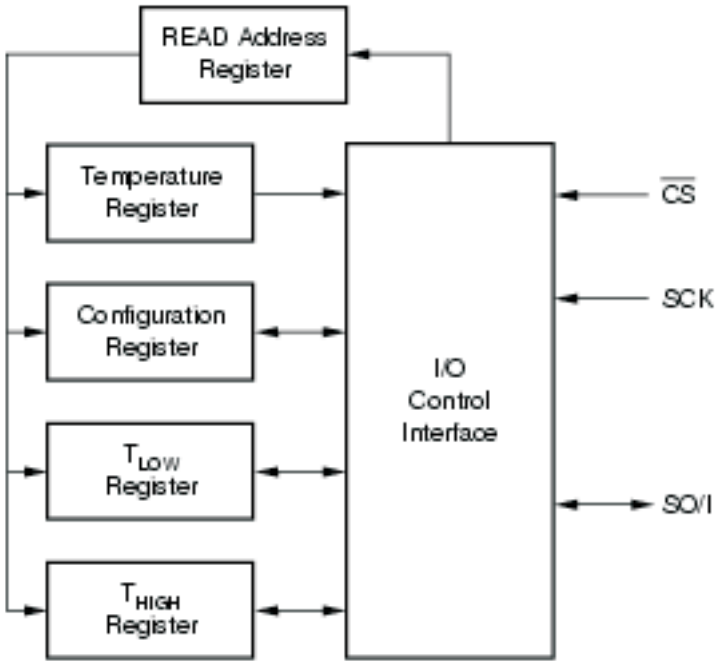


Figure 7. Internal Register Structure

Table 3. Pointer Addresses

P1	P0	REGISTER
0	0	Temperature Register (READ only)
0	1	Configuration Register (READ/WRITE)
1	0	T_{LOW} Register (READ/WRITE)
1	1	T_{HIGH} Register (READ/WRITE)

TEMPERATURE REGISTER

The Temperature Register of the TMP122 is a 16-bit, signed read-only register that stores the output of the most recent conversion. The TMP122 is specified for the temperature range of -55°C to 125°C with operation from -55°C to 150°C. Up to 16 bits can be read to obtain data and are described in Table 4. The first 13 bits are used to indicate temperature where bit D2 is 1, and D1, D0 are in a high impedance state. Data format for temperature is summarized in Table 5. Following power-up or reset, the Temperature Register will read 0°C until the first conversion is complete.

Table 4. Temperature Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	1	Z	Z

Table 5. Temperature Data Format

TEMPERATURE (°c)	DIGITAL OUTPUT(1) (BINARY)	HEX
150	0100 1011 0000 0111	4B07
125	0011 1110 1000 0111	3E87
25	0000 1100 1000 0111	0C87
0.0625	0000 0000 0000 1111	000F
0	0000 0000 0000 0111	0007
-0.0625	1111 1111 1111 1111	FFFF
-25	1111 0011 1000 0111	F387
-55	1110 0100 1000 0111	E487

(1) The last two bits are high impedance and are shown as 11 in the table.

The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the Configuration Register and setting the resolution bits accordingly. For 9-, 10-, or 11-bit resolution, the most significant bits in the Temperture Register are used with the unused LSBs set to zero.

CONFIGURATION REGISTER

The Configuration Register is a 16-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. The format of the Configuration Register for the TMP122 is shown in Table 6, followed by a break-down of the register bits. The power-up/reset value of the Configuration Register bits R1/R0 equal 1/1, all other bits equal zero.

Table 6. Configuration Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	D1	D0	R1	R0	F1	F0	POL	TM1	TM0	0	1	0

SHUTDOWN MODE (SD)

The Shutdown Mode of the TMP122 can be used to shut down all device circuitry except the serial interface. Shutdown mode occurs when the last 8 bits of the WRITE command are equal to 1, and will occur once the current conversion is completed, reducing current consumption to less than 1 μA. To take the part out of shutdown, send any command or pattern after the 16-bit read with the last 8 bits not equal to one. Power on default is in active mode.

THERMOSTAT MODE (TM1/TM0)

The Thermostat Mode bits of the TMP122 indicate to the device whether to operate in Comparator Mode, Interrupt Mode or Interrupt Comparator Mode. For more information on Comparator and Interrupt Mode, see text HIGH and LOW limit registers. The bit assignments for thermostat mode are described in Table 7. Power on default is comparator mode.

Table 7. Mode Settings

TM1	TM0	MODE OF OPERATION
0	0	Comparator mode
0	1	Interrupt mode
1	0	Interrupt comparator mode
1	1	Reserved

POLARITY (POL)

The Polarity Bit of the TMP122 adjusts the polarity of the ALERT pin output. By default, POL = 0 and the ALERT pin will be active LOW, as shown in Figure 8. For POL = 1 the ALERT Pin will be active HIGH, and the state of the ALERT Pin is inverted.

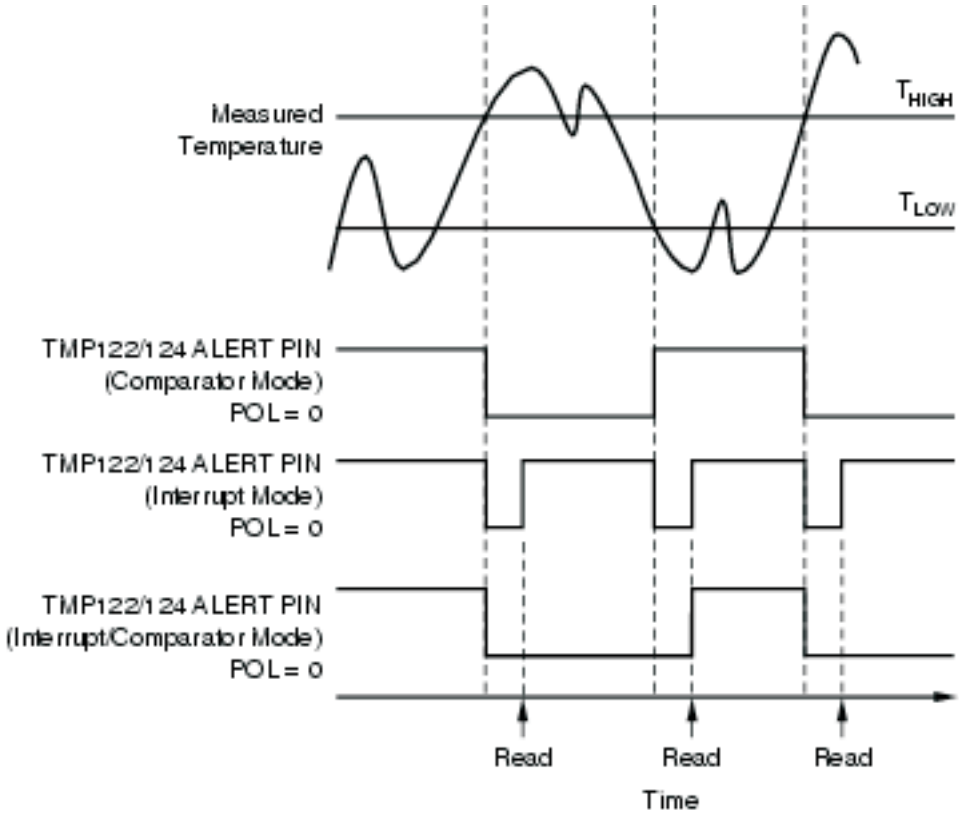


Figure 8. ALERT Output Transfer Function Diagrams

FAULT QUEUE (F1/F0)

A fault condition occurs when the measured temperature exceeds the limits set in the T_{HIGH} and T_{LOW} registers. The Fault Queue is provided to prevent a false alert due to environmental noise and requires consecutive fault measurements to trigger the alert function of the TMP122. Table 8 defines the number of consecutive faults required to trigger a consecutive alert condition. Power-on default for F1/F0 is 0/0.

Table 8. Fault Settings

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

HIGH AND LOW LIMIT REGISTERS

In Comparator Mode (TM1/TM0 = 0/0), the ALERT Pin of the TMP122 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin will remain active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In Interrupt Mode (TM1/TM0 = 0/1) the ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs. The ALERT pin will also be cleared if the device is placed in Shutdown Mode. Once the ALERT pin is cleared, it will only become active again by the temperature falling below T_{LOW}. When the temperature falls below T_{LOW}, the ALERT pin becomes active and remains active until cleared by a read operation of any register. Once the ALERT pin is cleared, the above cycle will repeat with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}.

In Interrupt/Comparator Mode (TM1/TM0 = 1/0), the ALERT Pin of the TMP122 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin will remain active until the temperature falls below the indicated T_{LOW} value for the same number of faults and a communication with the device has occurred after that point.

Operational modes are represented in Figure 8. Table 9 and Table 10 describe the format for the T_{HIGH} and T_{LOW} registers. Power-up reset values for T_{HIGH} and T_{LOW} are: T_{HIGH} = 80°C and T_{LOW} = 75°C. The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register. TABLE IX. T_{HIGH} Register.

All 13 bits for the Temperature, T_{HIGH}, and T_{LOW} registers are used in the comparisons for the ALERT function for all converter resolutions. The three LSBs in T_{HIGH} and T_{LOW} can affect the ALERT output even if the converter is configured for 9-bit resolution.

Table 9. T_{HIGH} Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
H12	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0	1	1	0

Table 10. T_{LOW} Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0	1	0	0

CONVERTER RESOLUTION (R1/R0)

The Converter Resolution Bits control the resolution of the internal analog-to-digital (A/D) converter. This allows the user to maximize efficiency by programming for higher resolution or faster conversion time. Table 11 identifies the resolution bits and the relationship between resolution and conversion time. The TMP122 has a default resolution of 12 bits.

Table 11. Resolution

R1	R2	RESOLUTION	CONVERSION TIME (TYPICAL)
0	0	9 bits (0.5°C) + sign	30 ms
0	1	10 bits (0.25°C) + sign	60 ms
1	0	11 bits (0.125°C) + sign	120 ms
1	1	12 bits (0.0625°C) + sign	240 ms

DELAY TIME

The Delay Bits control the amount of time delay between each conversion. This feature allows the user to maximize power savings by eliminating unnecessary conversions, and minimizing current consumption. During active conversion the TMP122 typically requires 50 µA of current for approximately 0.25s conversion time, and approximately 20 µA for idle times between conversions. Delay settings are identified in Table 12 as conversion time and period, and are shown in Figure 9. Default power up is D1/D0 equal 0/0. Conversion time and conversion periods scale with resolution. Conversion period denotes time between conversion starts.

Table 12. Conversion Delay for 12-Bit Resolution

D1	D2	CONVERSION TIME	CONVERSION PERIOD
0	0	0.25 s	0.25 s
0	1	0.25 s	0.5 s
1	0	0.25 s	1 s
1	1	0.25 s	8 s

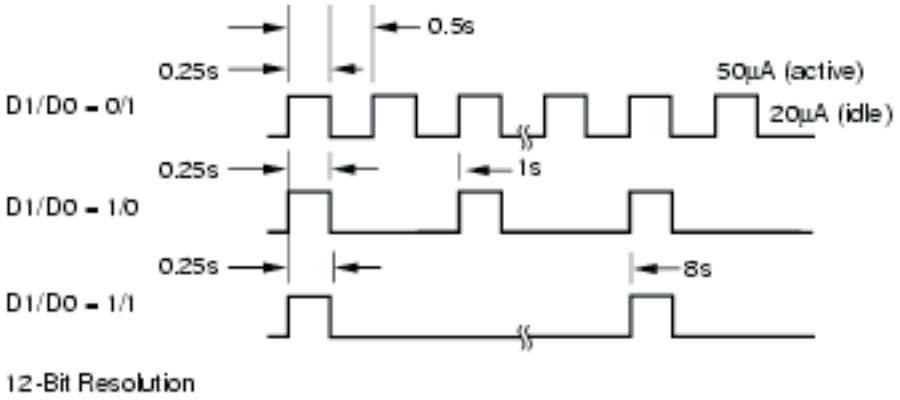


Figure 9. Conversion Time and Period Description

TIMING DIAGRAMS

The TMP122 is SPI compatible. Figure 10 to Figure 12 describe the various timing parameters of the TMP122 with timing definitions in Table 13.

Table 13. Timing Description

	PARAMETER	MIN	MAX	UNIT
t_1	SCK period	100		ns
t_2	Data in to rising edge SCK setup time	20		ns
t_3	SCK falling edge to output data delay		30	ns
t_4	SCK rising edge to input data hold time	20		ns
t_5	$\overline{CS}$ to rising edge SCK set-up time	40		ns
t_6	$\overline{CS}$ to output data delay		30	ns
t_7	$\overline{CS}$ rising edge to output high impedance		30	ns

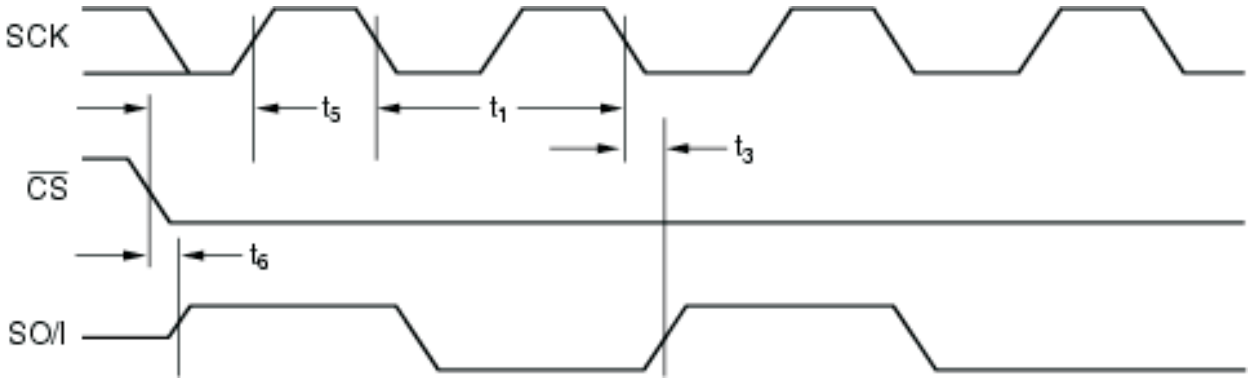


Figure 10. Output Data Timing Diagram

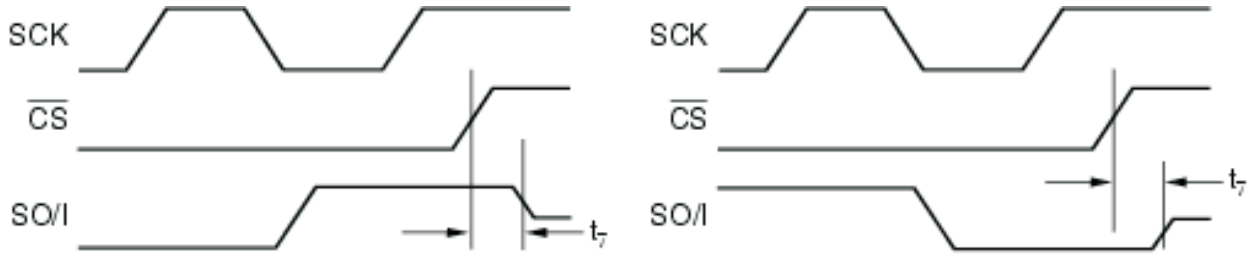


Figure 11. High Impedance Output Timing Diagram

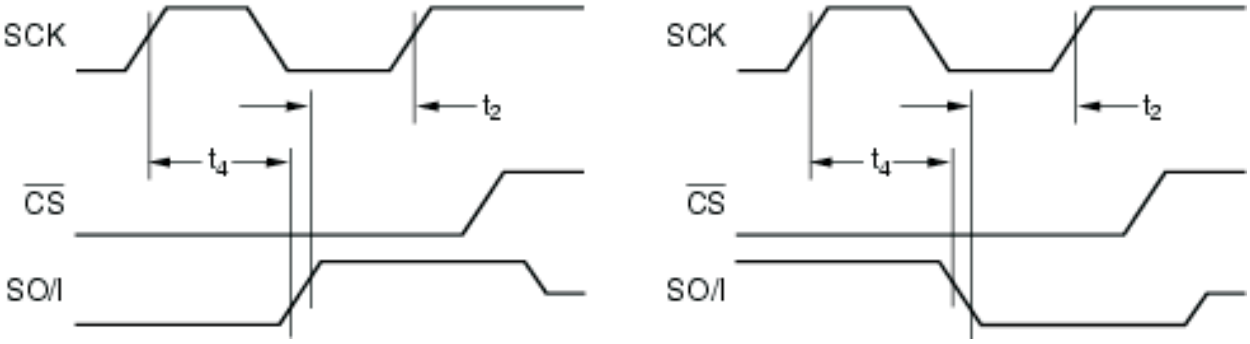


Figure 12. Input Data Timing Diagram

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TMP122AMDBVTEP	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	122E	Samples
V62/09607-01XE	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	122E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

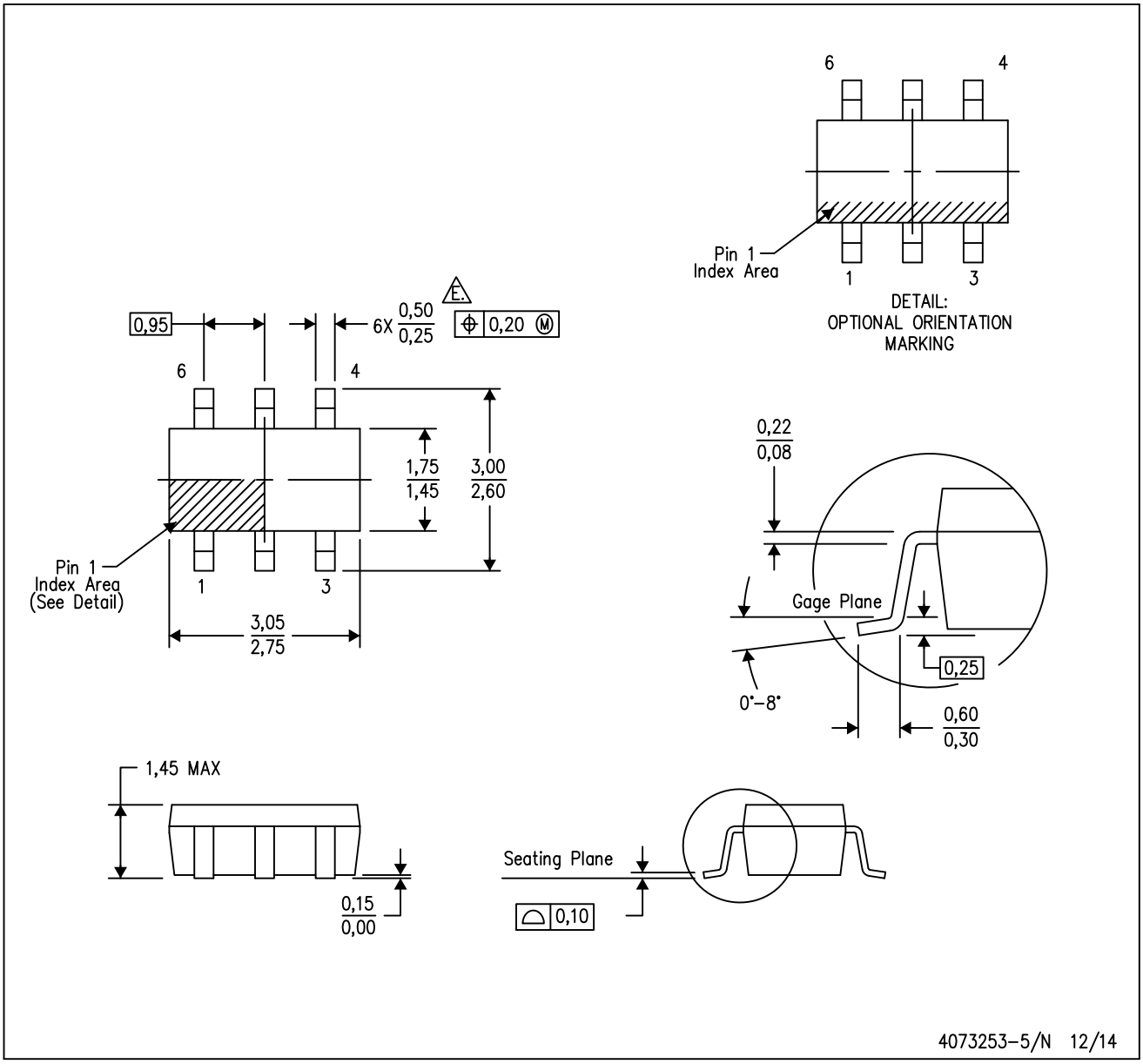
OTHER QUALIFIED VERSIONS OF TMP122-EP :

- Catalog: TMP122

NOTE: Qualified Version Definitions:

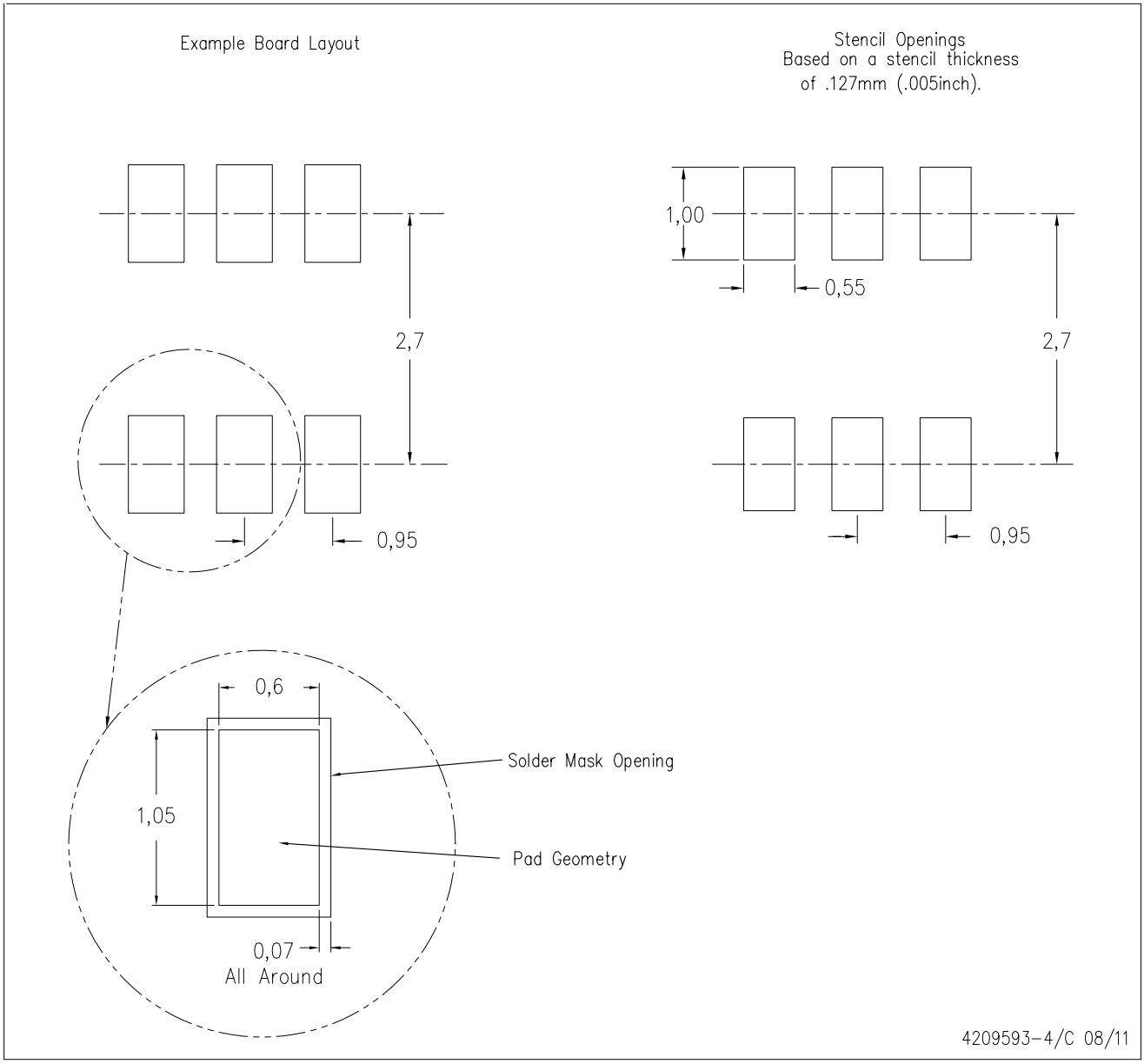
- Catalog - TI's standard catalog product

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265