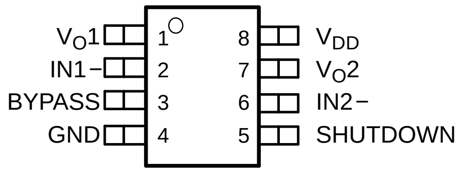
# 150-mW STEREO AUDIO POWER AMPLIFIER

## FEATURES

- 150-mW Stereo Output
- PC Power Supply Compatible
  - – Fully Specified for 3.3-V and 5-V Operation
  - – Operation to 2.5 V
- Pop Reduction Circuitry
- Internal Midrail Generation
- Thermal and Short-Circuit Protection
- Surface-Mount Packaging
  - – PowerPAD™ MSOP
  - – SOIC
- Pin Compatible With LM4880 and LM4881 (SOIC)

**D OR DGN PACKAGE**
**(TOP VIEW)**

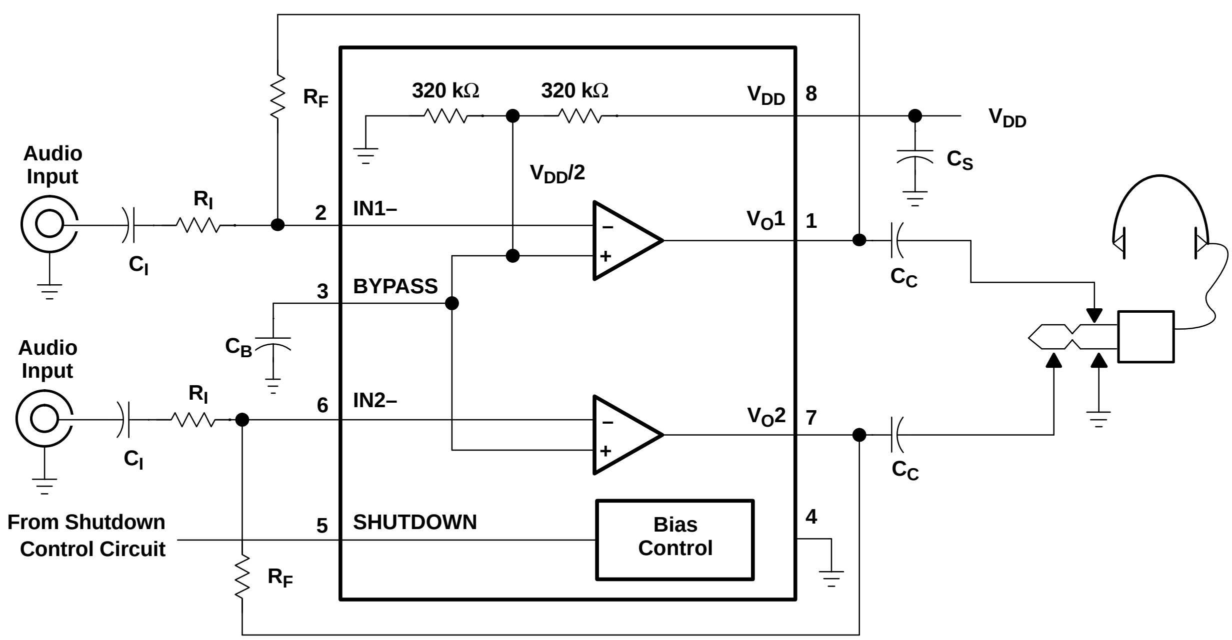



## DESCRIPTION

The TPA122 is a stereo audio power amplifier packaged in either an 8-pin SOIC, or an 8-pin PowerPAD™ MSOP package capable of delivering 150 mW of continuous RMS power per channel into 8-Ω loads. Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 1 to 10.

THD+N when driving an 8-Ω load from 5 V is 0.1% at 1 kHz, and less than 2% across the audio band of 20 Hz to 20 kHz. For 32-Ω loads, the THD+N is reduced to less than 0.06% at 1 kHz, and is less than 1% across the audio band of 20 Hz to 20 kHz. For 10-kΩ loads, the THD+N performance is 0.01% at 1 kHz, and less than 0.02% across the audio band of 20 Hz to 20 kHz.

## TYPICAL APPLICATION CIRCUIT



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## AVAILABLE OPTIONS

| $T_A$ | PACKAGED DEVICES | | MSOP SYMBOLIZATION |
|---|---|---|---|
| | SMALL OUTLINE(1) (D) | MSOP(1) (DGN) | |
| –40°C to 85°C | TPA122D | TPA122DGN | TI AAE |

(1) The D and DGN packages are available in left-ended tape and reel only (e.g., TPA122DR, TPA122DGNR).

## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| BYPASS | 3 | I | Tap to voltage divider for internal mid-supply bias supply. Connect to a 0.1 µF to 1 µF low ESR capacitor for best performance. |
| GND | 4 | I | GND is the ground connection. |
| IN1- | 2 | I | IN1- is the inverting input for channel 1. |
| IN2- | 6 | I | IN2- is the inverting input for channel 2. |
| SHUTDOWN | 5 | I | Puts the device in a low quiescent current mode when held high |
| $V_{DD}$ | 8 | I | $V_{DD}$ is the supply voltage terminal. |
| $V_O1$ | 1 | O | $V_O1$ is the audio output for channel 1. |
| $V_O2$ | 7 | O | $V_O2$ is the audio output for channel 2. |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

| | | UNIT |
|---|---|---|
| $V_{DD}$ | Supply voltage | 6 V |
| $V_I$ | Input voltage | –0.3 V to $V_{DD}$ + 0.3 V |
| | Continuous total power dissipation | Internally limited |
| $T_J$ | Operating junction temperature range | –40°C to 150°C |
| $T_{stg}$ | Storage temperature range | –65°C to 150°C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## DISSIPATION RATING TABLE

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| D | 725 mW | 5.8 mW/°C | 464 mW | 377 mW |
| DGN | 2.14 W(1) | 17.1 mW/°C | 1.37 W | 1.11 W |

(1) See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* of that document.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2.5 | 5.5 | V |
| $T_A$ | Operating free-air temperature | –40 | 85 | °C |
| $V_{IH}$ | High-level input voltage, (SHUTDOWN) | $0.80 \times V_{DD}$ | | V |
| $V_{IL}$ | Low-level input voltage, (SHUTDOWN) | | $0.40 \times V_{DD}$ | V |

## DC ELECTRICAL CHARACTERISTICS

at $T_A$ = 25°C, $V_{DD}$ = 3.3 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OO}$ | Output offset voltage | | | | 10 | mV |
| PSRR | Power supply rejection ratio | $V_{DD}$ = 3.2 V to 3.4 V | | 83 | | dB |
| $I_{DD}$ | Supply current | $V_{DD}$ = 2.5, SHUTDOWN = 0 V | | 1.5 | 3 | mA |
| $I_{DD(SD)}$ | Supply current in SHUTDOWN mode | $V_{DD}$ = 2.5, SHUTDOWN = $V_{DD}$ | | 10 | 50 | µA |
| $Z_I$ | Input impedance | | | > 1 | | MΩ |

## AC OPERATING CHARACTERISTICS

$V_{DD}$ = 3.3 V, $T_A$ = 25°C, $R_L$ = 8 Ω

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_O$ | Output power (each channel) | THD≤ 0.1% | | 70 (1) | | mW |
| THD+N | Total harmonic distortion + noise | $P_O$ = 70 mW, 20 Hz–20 kHz | | 2% | | |
| $B_{OM}$ | Maximum output power BW | G = 10, THD < 5% | | > 20 | | kHz |
| | Phase margin | Open loop | | 58° | | |
| | Supply ripple rejection | f = 1 kHz | | 68 | | dB |
| | Channel/channel output separation | f = 1 kHz | | 86 | | dB |
| SNR | Signal-to-noise ratio | $P_O$ = 100 mW | | 100 | | dB |
| $V_n$ | Noise output voltage | | | 9.5 | | µV(rms) |

(1) Measured at 1 kHz

## DC ELECTRICAL CHARACTERISTICS

at $T_A$ = 25°C, $V_{DD}$ = 5.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OO}$ | Output offset voltage | | | | 10 | mV |
| PSRR | Power supply rejection ratio | $V_{DD}$ = 4.9 V to 5.1 V | | 76 | | dB |
| $I_{DD}$ | Supply current | SHUTDOWN = 0 V | | 1.5 | 3 | mA |
| $I_{DD(SD)}$ | Supply current in SHUTDOWN mode | SHUTDOWN = $V_{DD}$ | | 60 | 100 | µA |
| $\|I_{IH}\|$ | High-level input current (SHUTDOWN) | $V_{DD}$ = 5.5 V, $V_I$ = $V_{DD}$ | | | 1 | µA |
| $\|I_{IL}\|$ | Low-level input current (SHUTDOWN) | $V_{DD}$ = 5.5 V, $V_I$ = 0 V | | | 1 | µA |
| $Z_I$ | Input impedance | | | > 1 | | MΩ |

## AC OPERATING CHARACTERISTICS

$V_{DD}$ = 5 V, $T_A$ = 25°C, $R_L$ = 8 Ω

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_O$ | Output power (each channel) | THD≤ 0.1% | | 70[1] | | mW |
| THD+N | Total harmonic distortion + noise | $P_O$ = 150 mW, 20 Hz–20 kHz | | 2% | | |
| $B_{OM}$ | Maximum output power BW | G = 10, THD < 5% | | > 20 | | kHz |
| | Phase margin | Open loop | | 56° | | |
| | Supply ripple rejection ratio | f = 1 kHz | | 68 | | dB |
| | Channel/channel output separation | f = 1 kHz | | 86 | | dB |
| SNR | Signal-to-noise ratio | $P_O$ = 150 mW | | 100 | | dB |
| $V_n$ | Noise output voltage | | | 9.5 | | µV(rms) |

(1) Measured at 1 kHz

## AC OPERATING CHARACTERISTICS

$V_{DD}$ = 3.3 V, $T_A$ = 25°C, $R_L$ = 32 Ω

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_O$ | Output power (each channel) | THD≤ 0.1% | | 40[1] | | mW |
| THD+N | Total harmonic distortion + noise | $P_O$ = 30 mW, 20 Hz–20 kHz | | 0.5% | | |
| $B_{OM}$ | Maximum output power BW | G = 10, THD < 2% | | > 20 | | kHz |
| | Phase margin | Open loop | | 58° | | |
| | Supply ripple rejection | f = 1 kHz | | 68 | | dB |
| | Channel/channel output separation | f = 1 kHz | | 86 | | dB |
| SNR | Signal-to-noise ratio | $P_O$ = 100 mW | | 100 | | dB |
| $V_n$ | Noise output voltage | | | 9.5 | | µV(rms) |

(1) Measured at 1 kHz

## AC OPERATING CHARACTERISTICS

$V_{DD}$ = 5 V, $T_A$ = 25°C, $R_L$ = 32 Ω

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_O$ | Output power (each channel) | THD≤ 0.1% | | 40[1] | | mW |
| THD+N | Total harmonic distortion + noise | $P_O$ = 60 mW, 20 Hz–20 kHz | | 0.4% | | |
| $B_{OM}$ | Maximum output power BW | G = 10, THD < 2% | | > 20 | | kHz |
| | Phase margin | Open loop | | 56° | | |
| | Supply ripple rejection | f = 1 kHz | | 68 | | dB |
| | Channel/channel output separation | f = 1 kHz | | 86 | | dB |
| SNR | Signal-to-noise ratio | $P_O$ = 150 mW | | 100 | | dB |
| $V_n$ | Noise output voltage | | | 9.5 | | µV(rms) |

(1) Measured at 1 kHz

# TYPICAL CHARACTERISTICS

## Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| THD+N | Total harmonic distortion plus noise | vs Frequency | 1, 2, 4, 5, 7, 8, 10, 11, 13, 14, 16, 17, 34, 36 |
| | | vs Output power | 3, 6, 9, 12, 15, 18 |
| | Supply ripple rejection | vs Frequency | 19, 20 |
| $V_n$ | Output noise voltage | vs Frequency | 21, 22 |
| | Crosstalk | vs Frequency | 23-26, 37, 38 |
| | Mute attenuation | vs Frequency | 27, 28 |
| | Open-loop gain and phase margin | vs Frequency | 29, 30 |
| | Output power | vs Load resistance | 31, 32 |
| | Phase | vs Frequency | 39-44 |
| $I_{DD}$ | Supply current | vs Supply voltage | 33 |
| SNR | Signal-to-noise ratio | vs Voltage gain | 35 |
| | Closed-loop gain | vs Frequency | 39-44 |
| | Power dissipation/amplifier | vs Output power | 45, 46 |

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

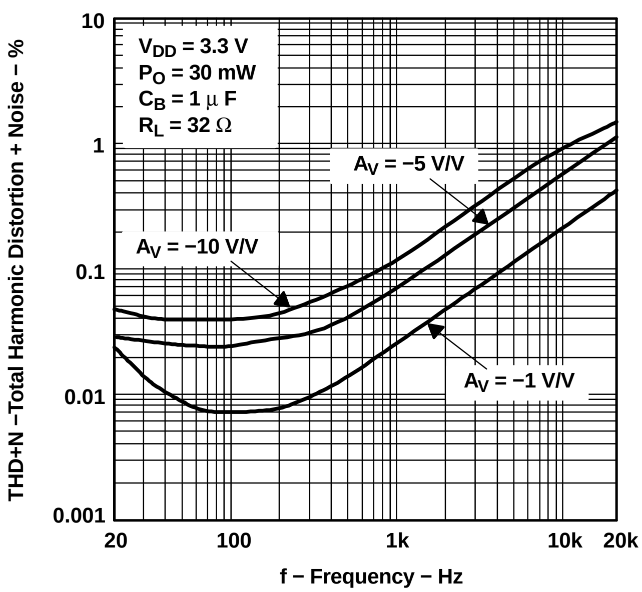



Figure 1.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

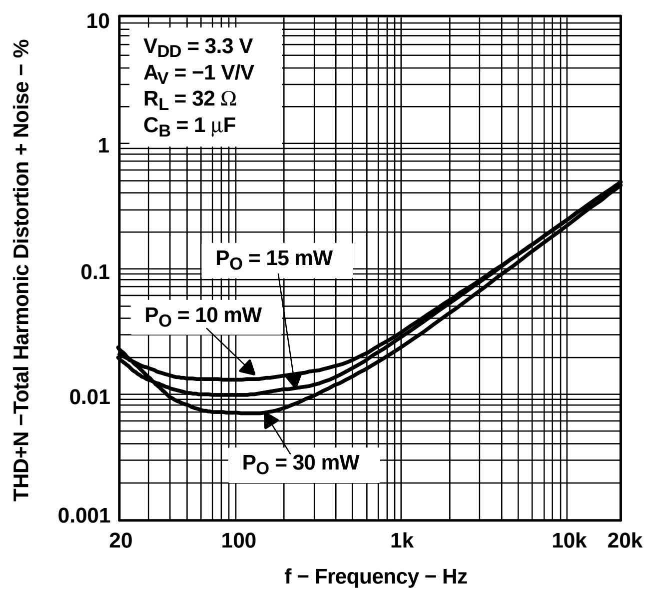



Figure 2.

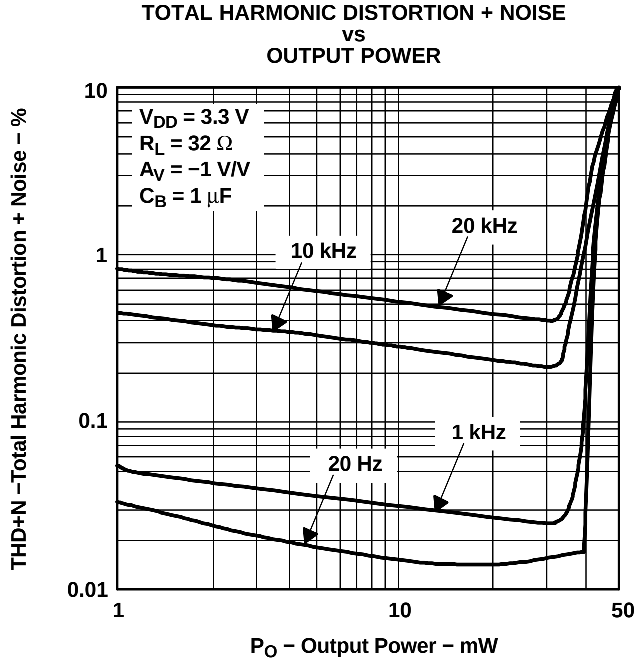



Figure 3.

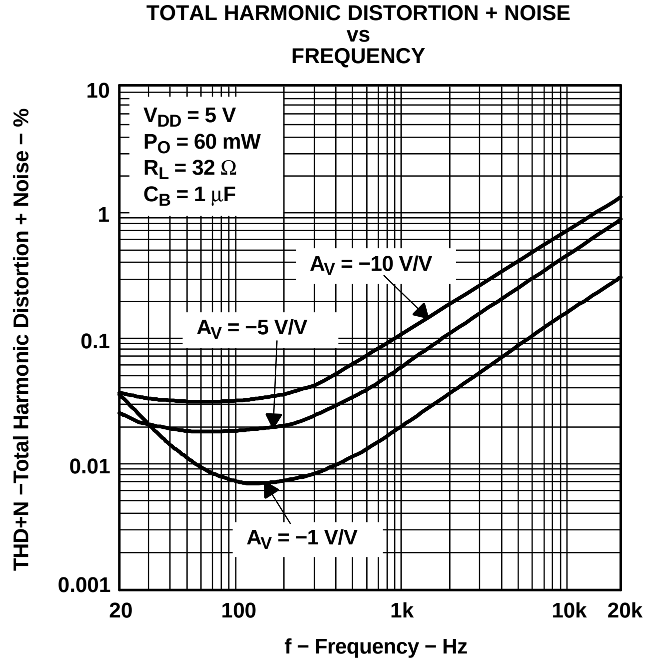



Figure 4.

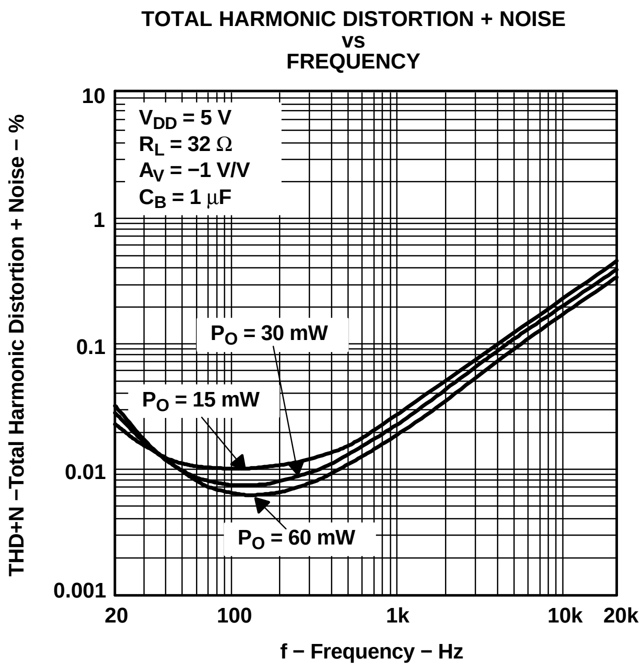



Figure 5.

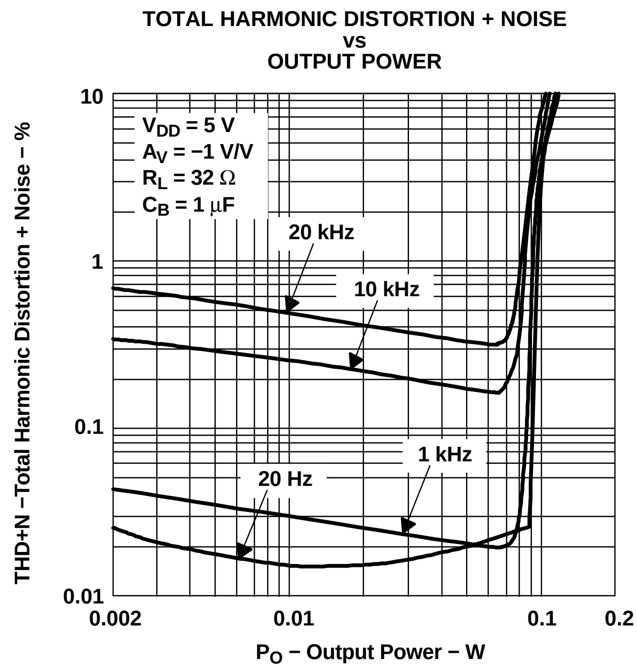



Figure 6.

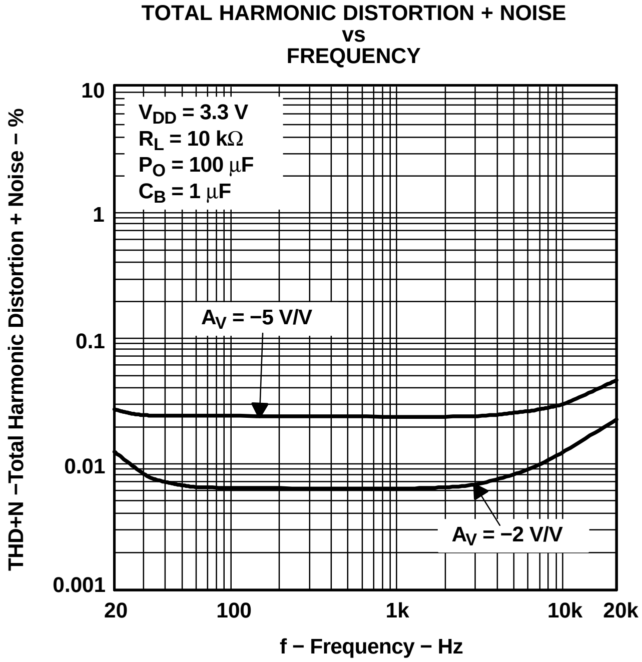
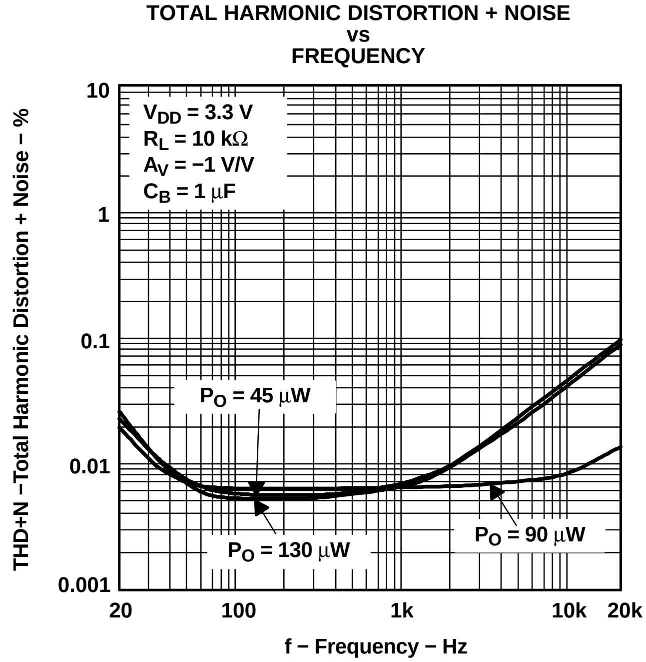



Figure 7.

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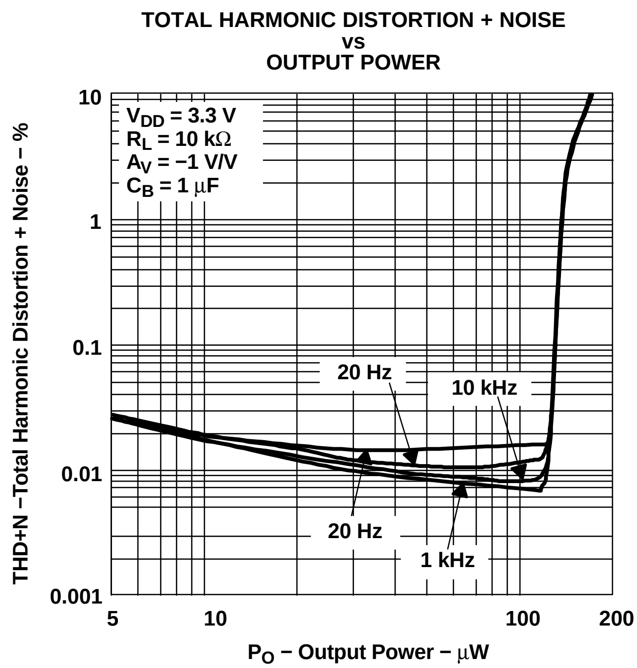



Figure 9.

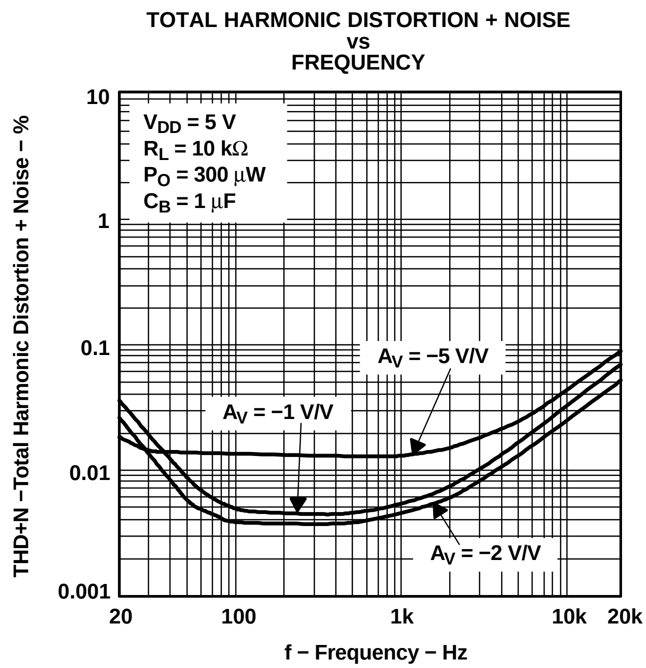



Figure 10.

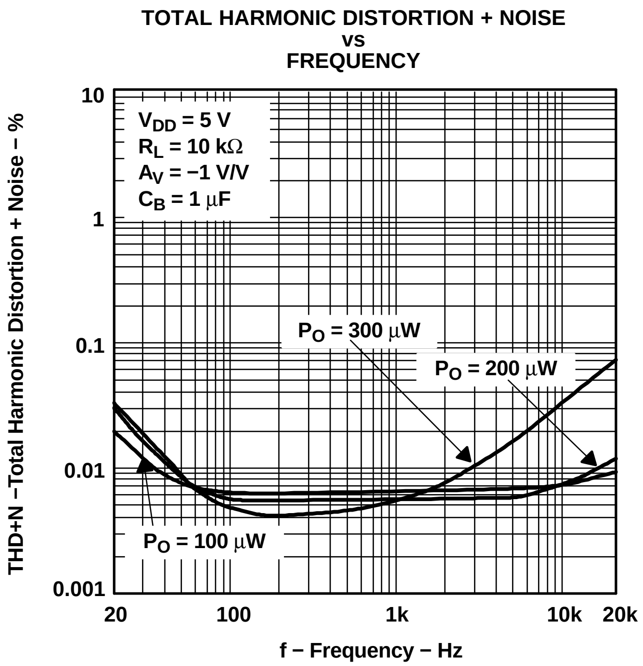



Figure 11.

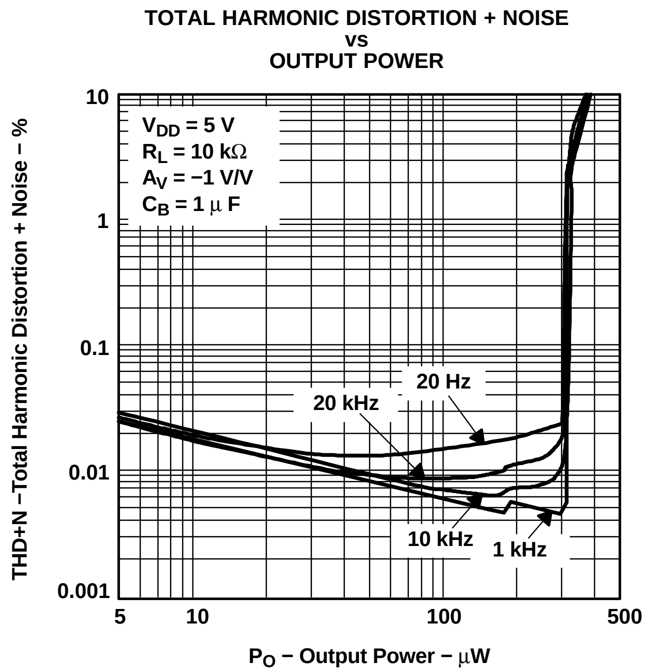



Figure 12.

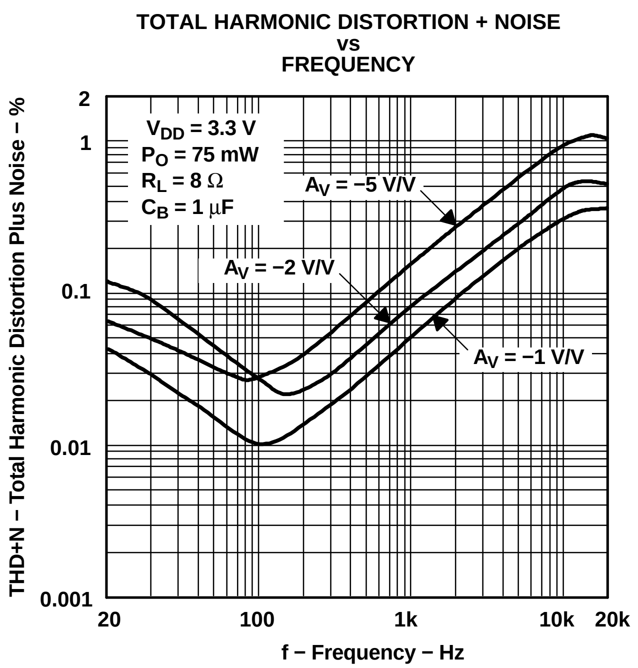



Figure 13.

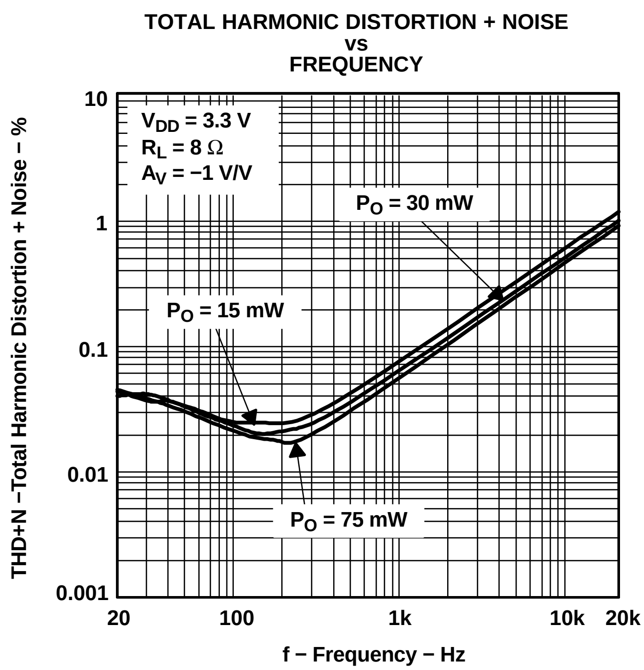



Figure 14.

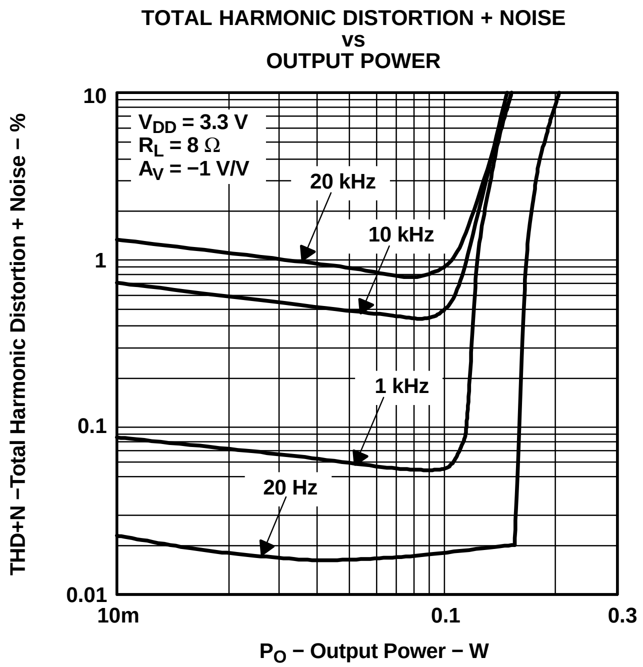



**Figure 15.**

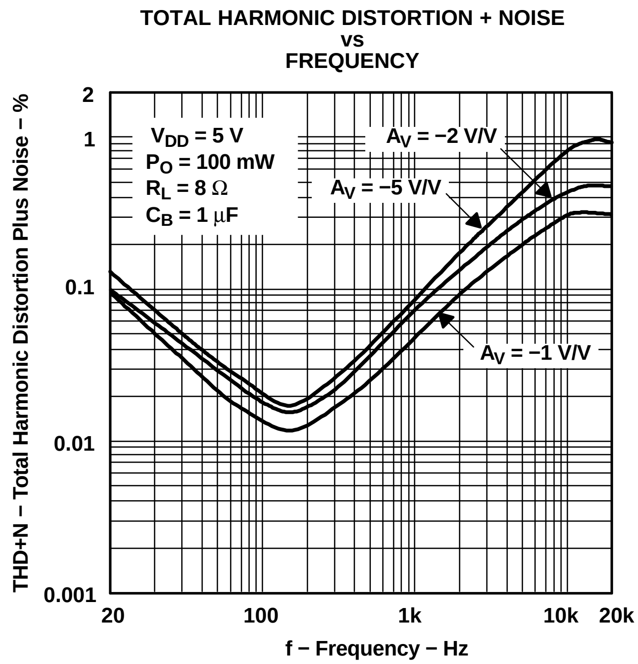



**Figure 16.**

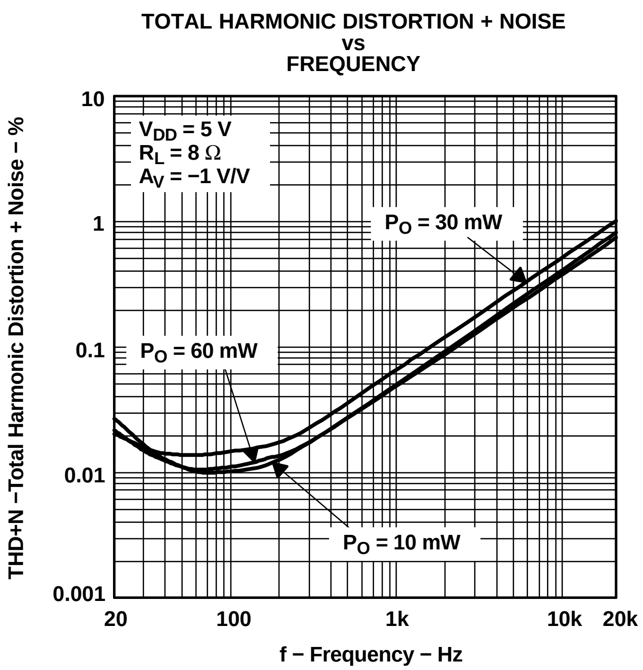



**Figure 17.**

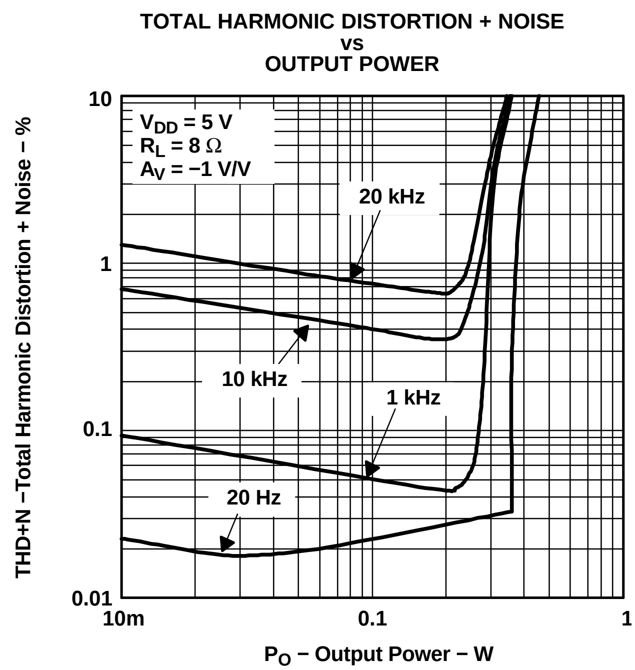



**Figure 18.**

**SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY**

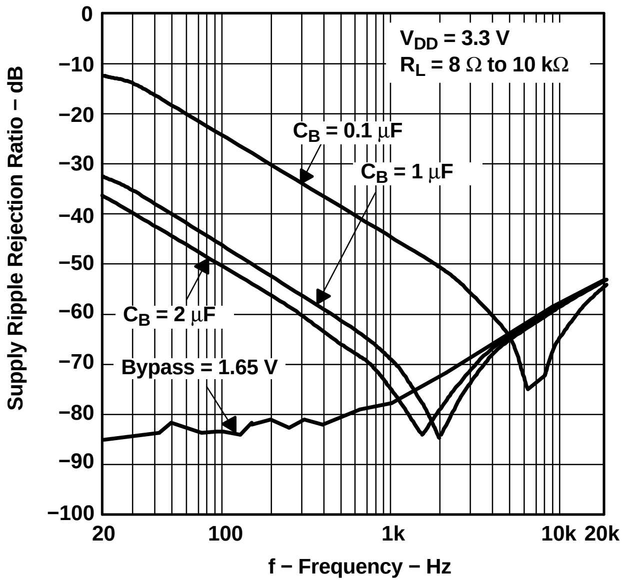



**Figure 19.**

**SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY**

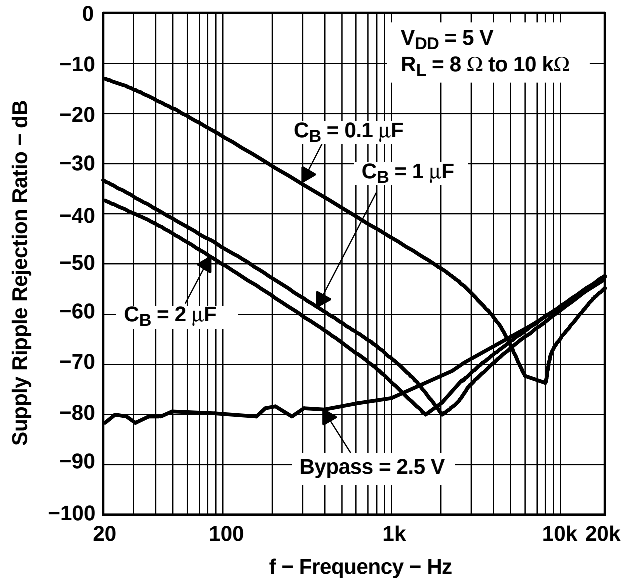



**Figure 20.**

**OUTPUT NOISE VOLTAGE
vs
FREQUENCY**

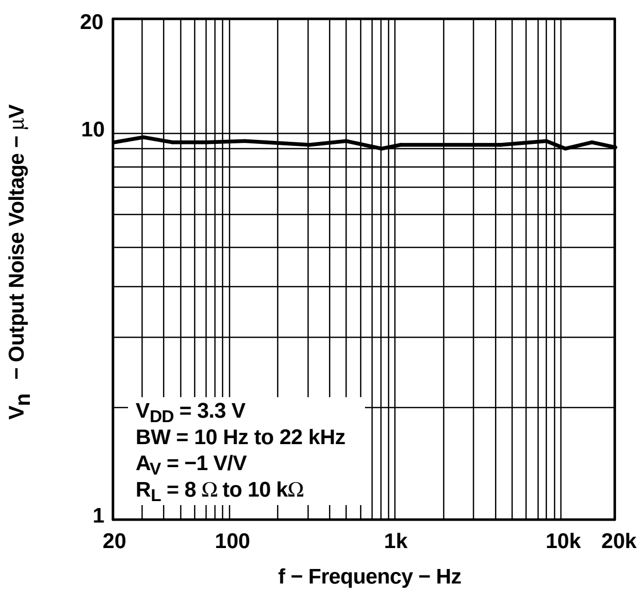



**Figure 21.**

**OUTPUT NOISE VOLTAGE
vs
FREQUENCY**

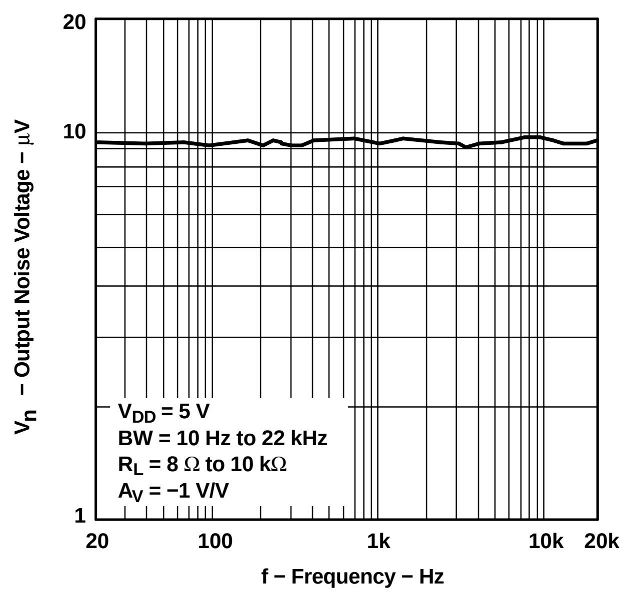



**Figure 22.**

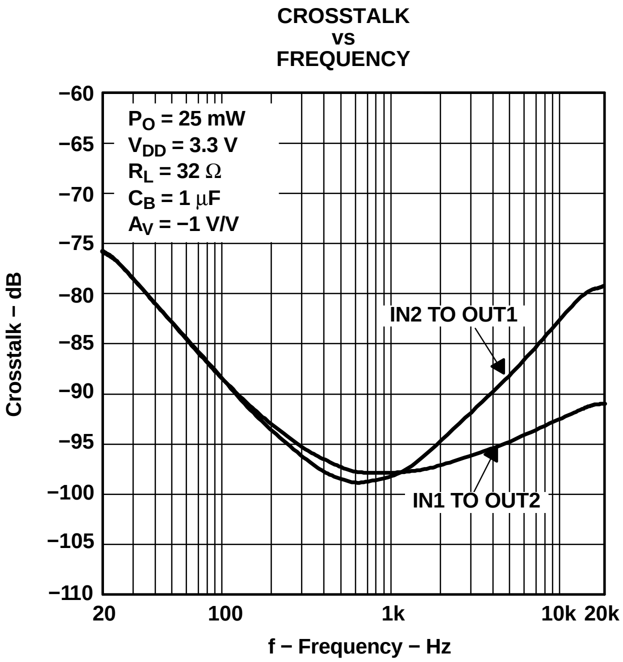
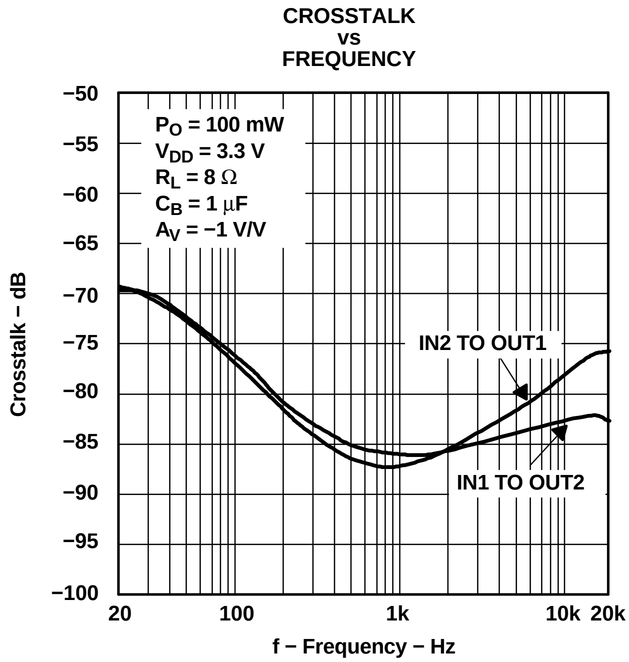



Figure 23.

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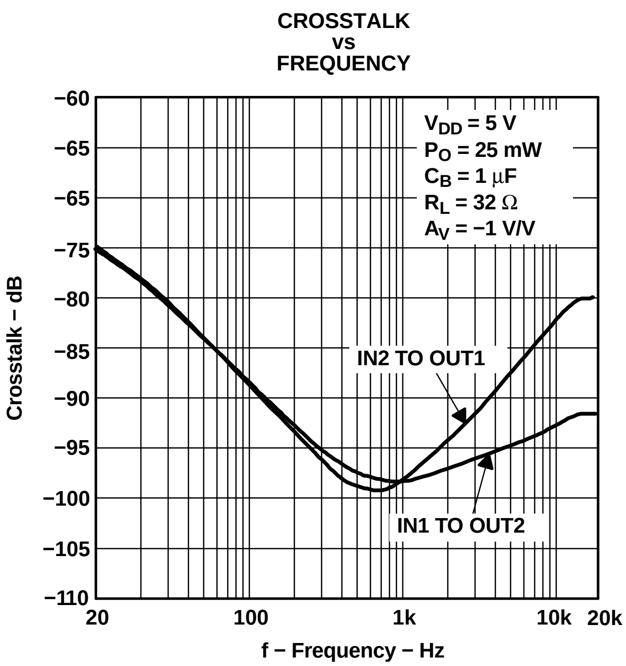



Figure 25.

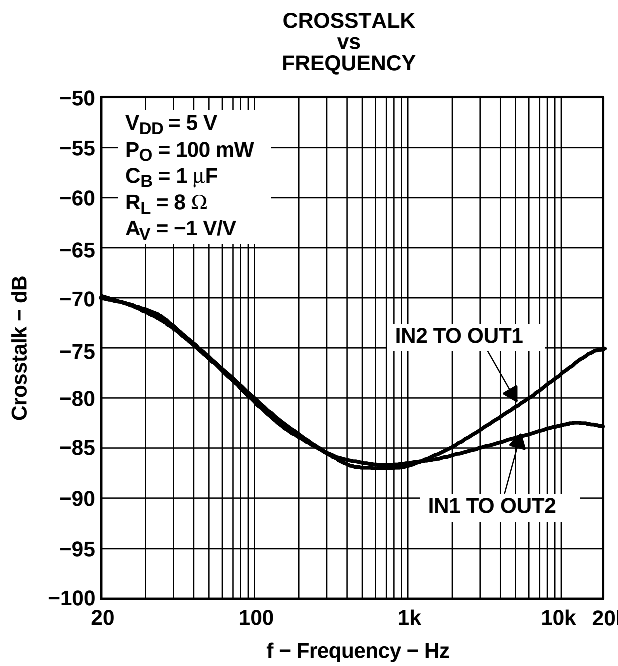



Figure 26.

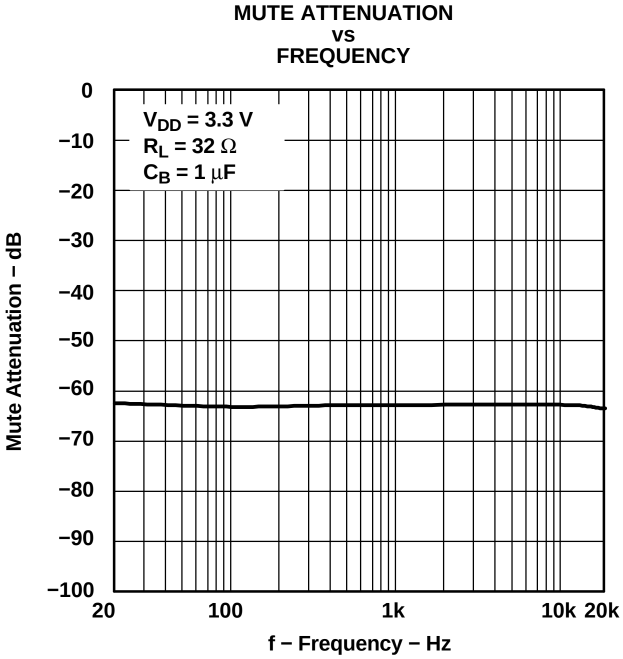
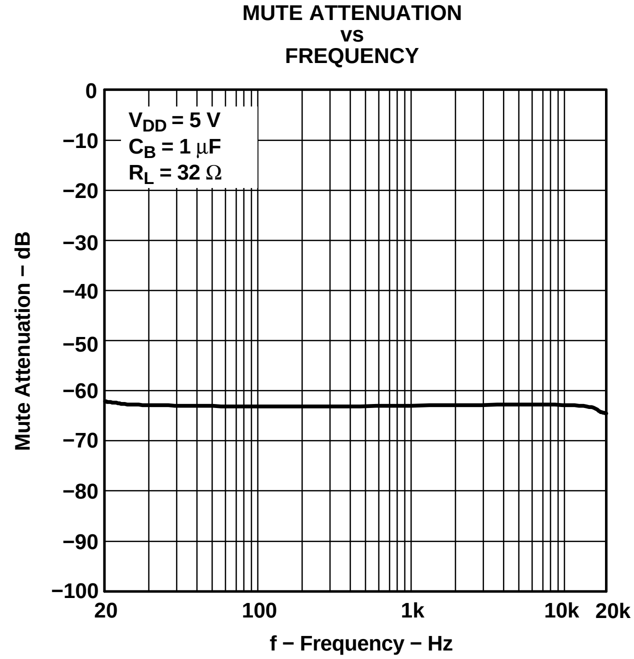



Figure 27.

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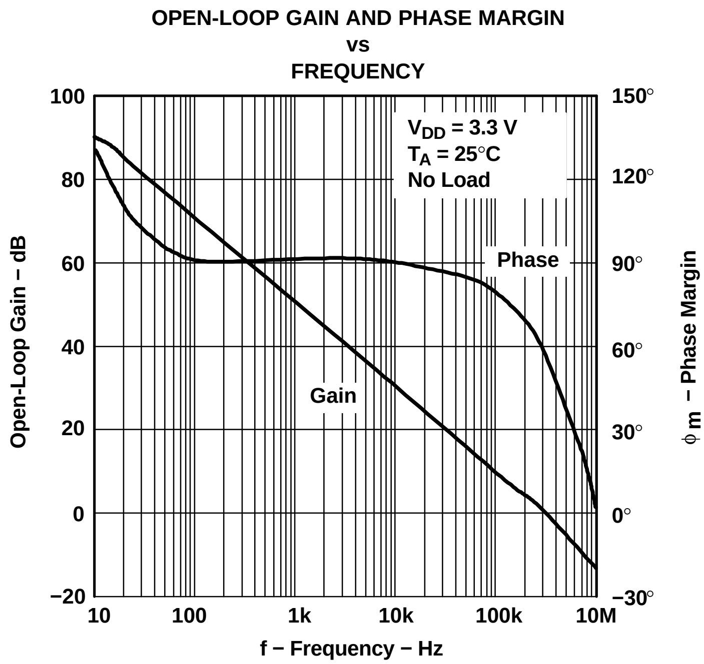



Figure 29.

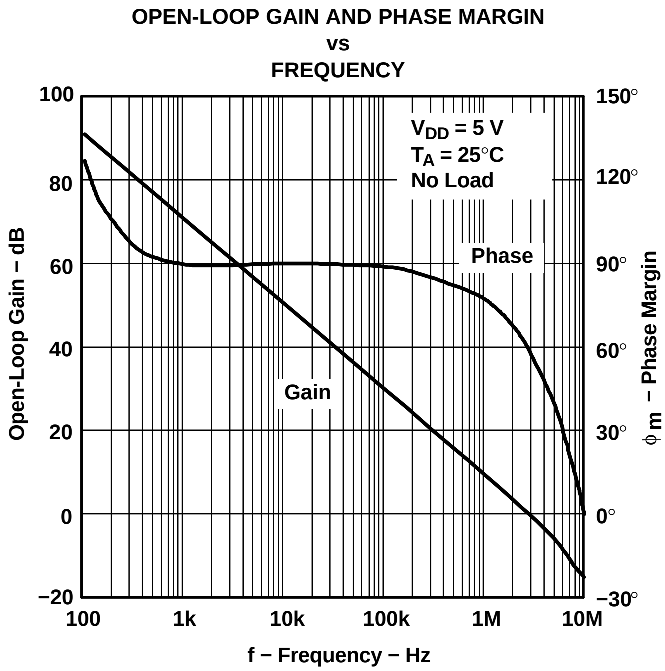



Figure 30.

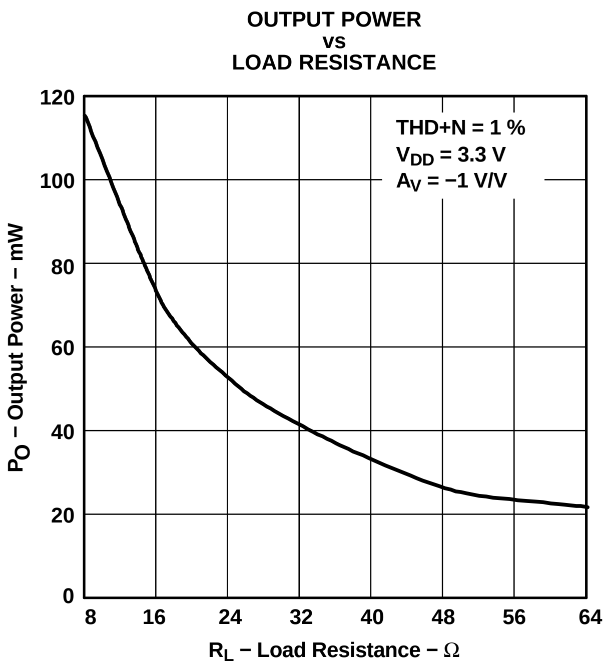



Figure 31.

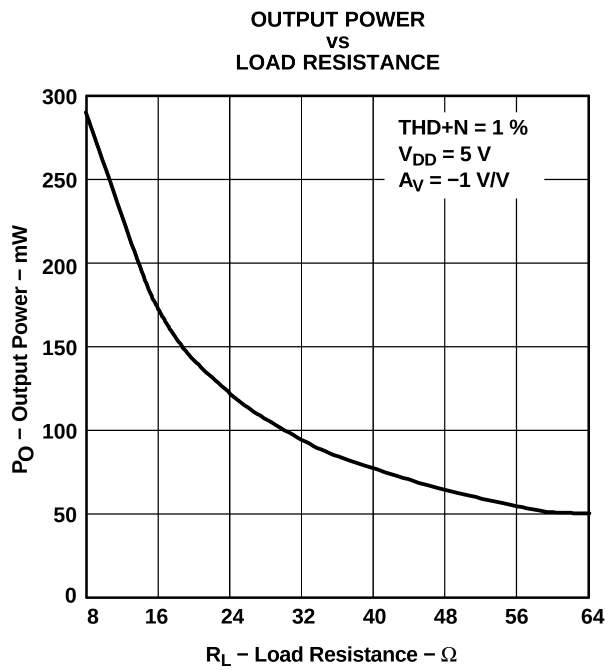



Figure 32.

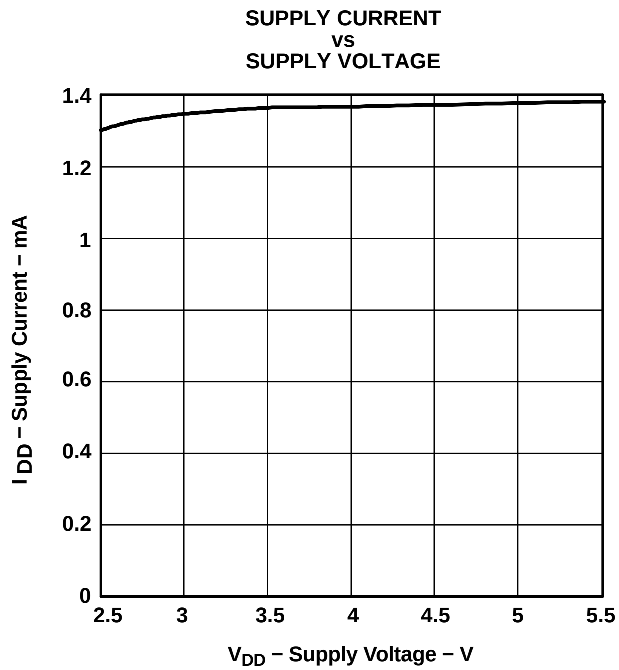



Figure 33.

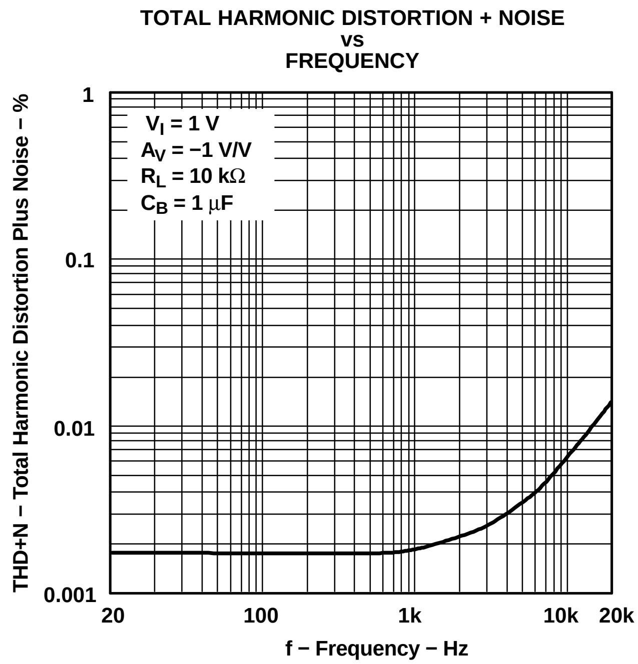



Figure 34.

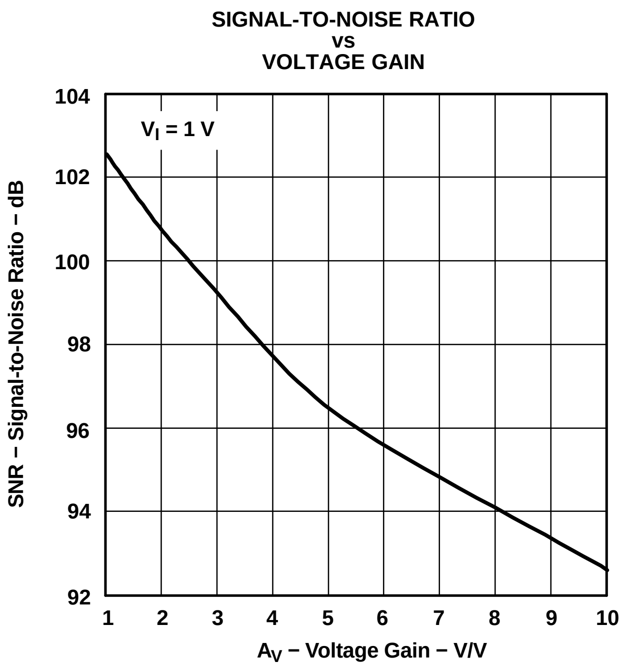



Figure 35.

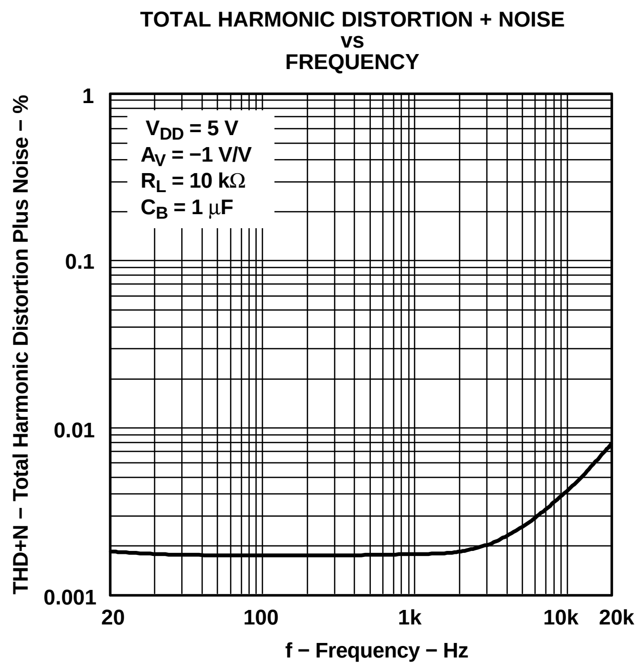
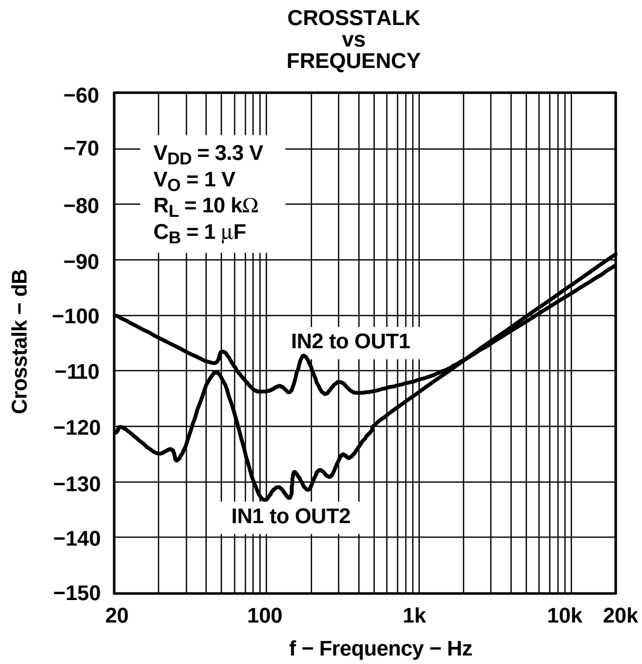



Figure 36.

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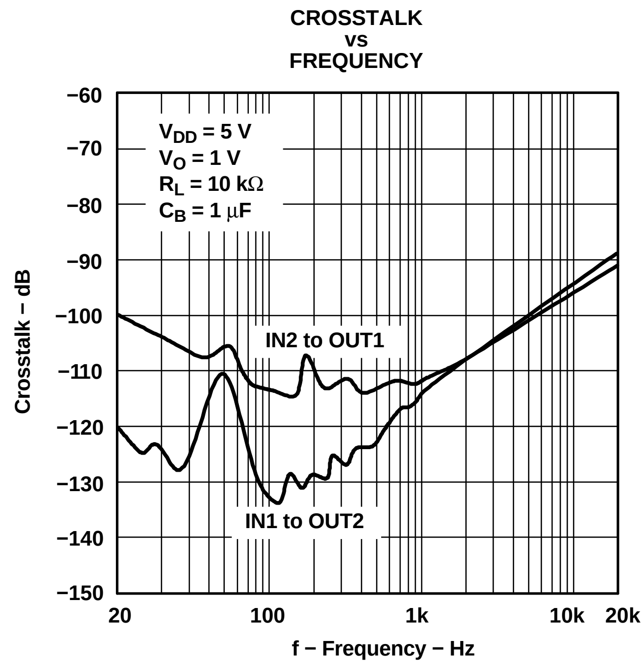


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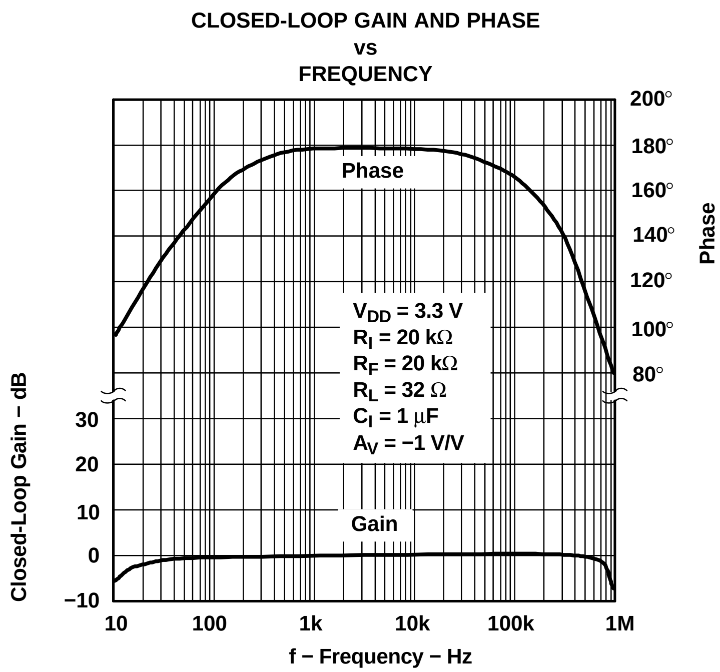


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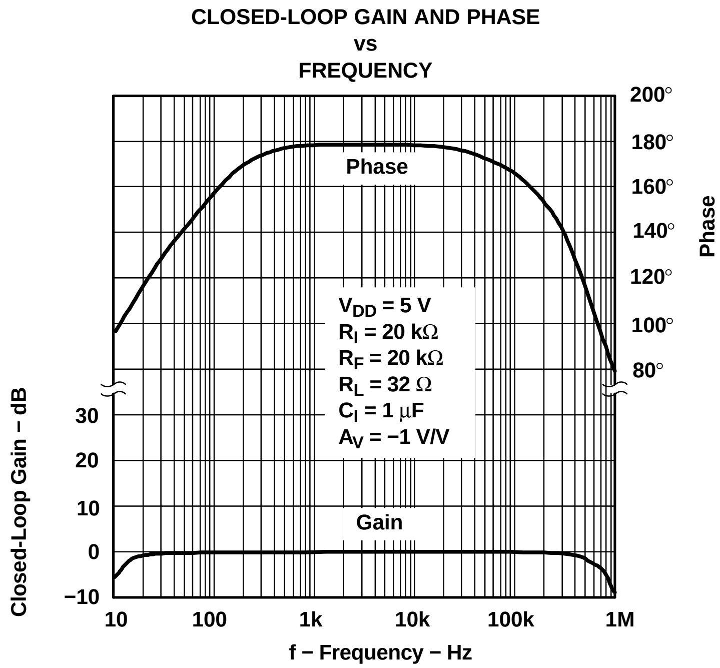


Figure 40.

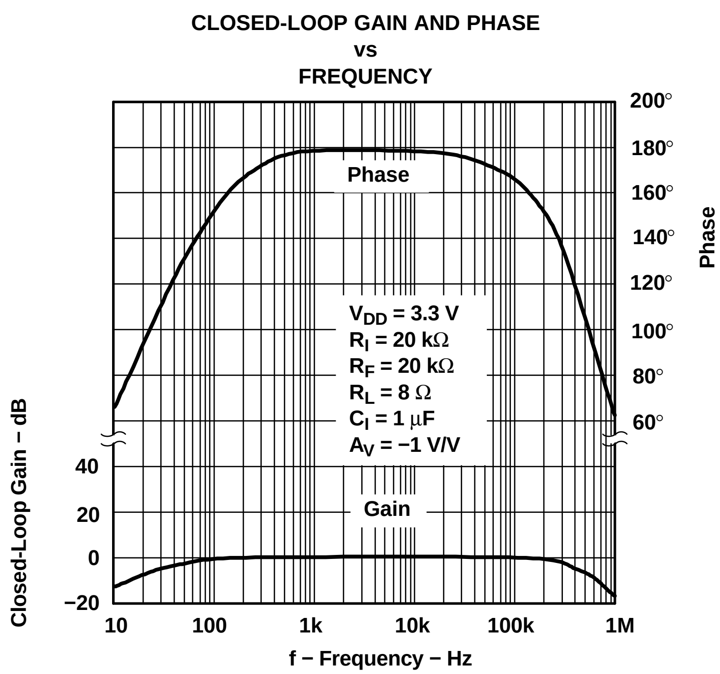


Figure 41.

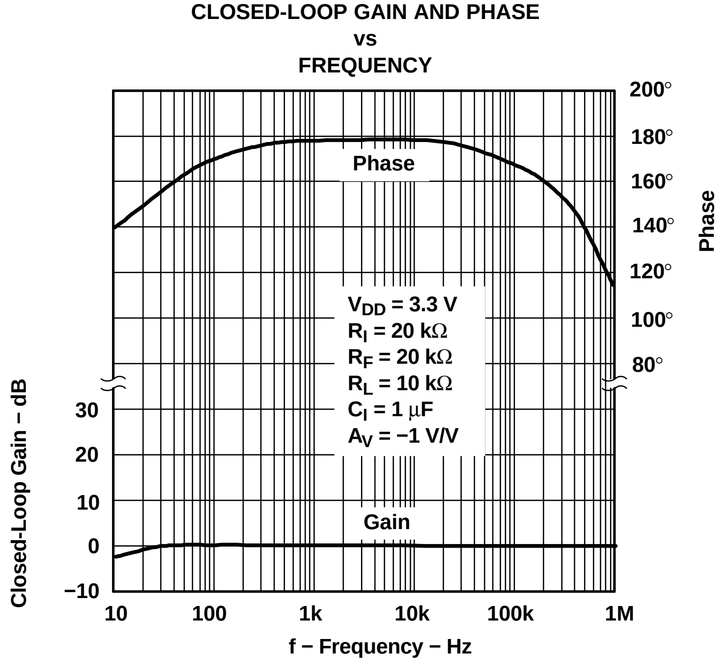


Figure 42.

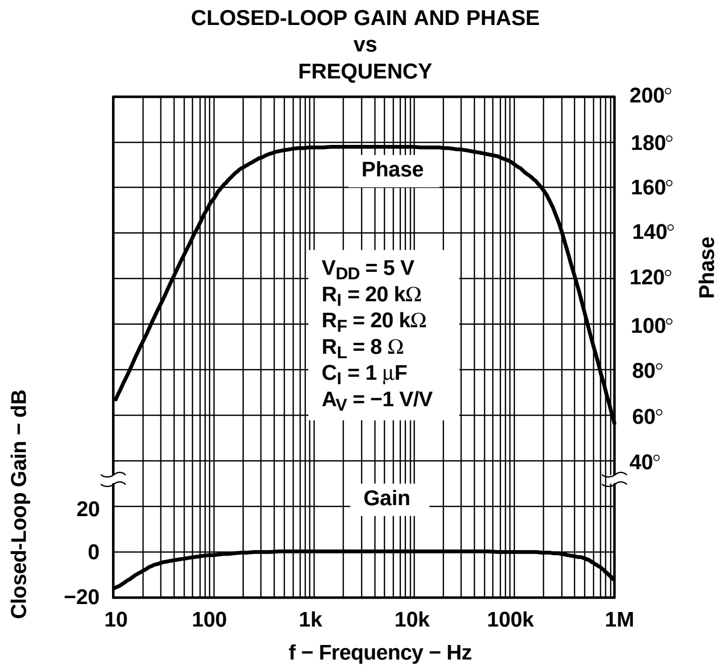


Figure 43.

**CLOSED-LOOP GAIN AND PHASE**
**vs**
**FREQUENCY**

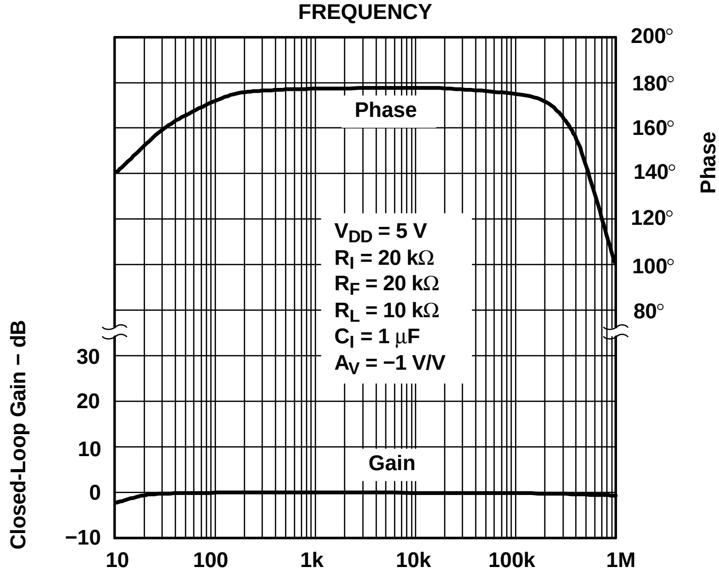


**Figure 44.**

**POWER DISSIPATION/AMPLIFIER**
**vs**
**OUTPUT POWER**

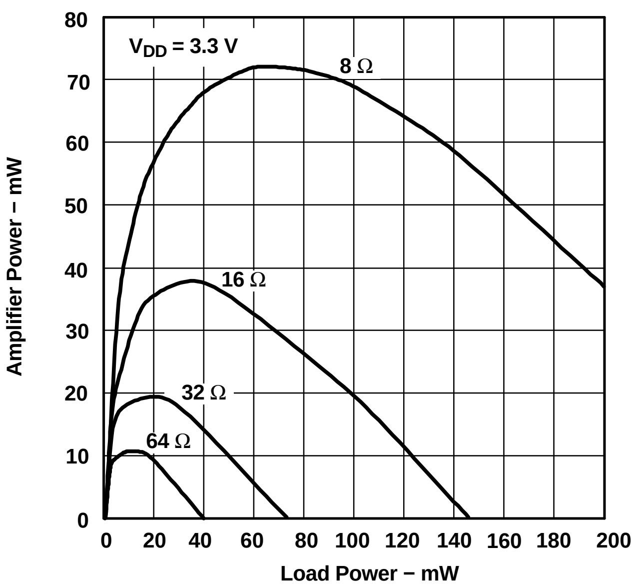


**Figure 45.**

**POWER DISSIPATION/AMPLIFIER**
**vs**
**OUTPUT POWER**

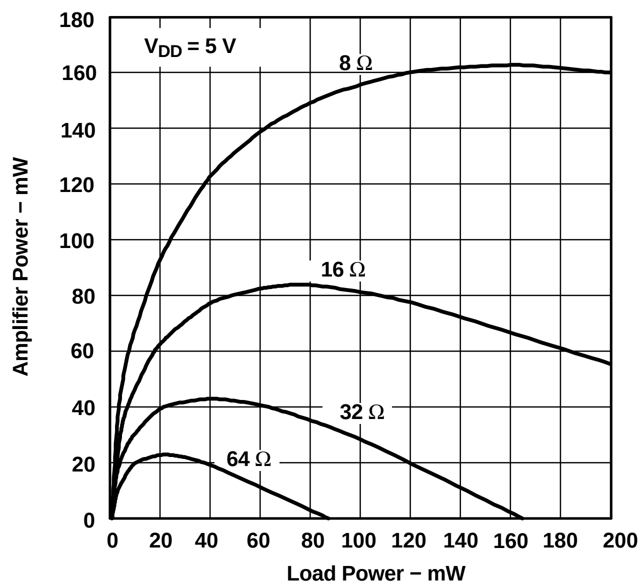


**Figure 46.**

## APPLICATION INFORMATION

### GAIN SETTING RESISTORS, $R_F$ and $R_I$

The gain for the TPA122 is set by resistors $R_F$ and $R_I$ according to Equation 1.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \quad (1)$$

Given that the TPA122 is an MOS amplifier, the input impedance is high. Consequently, input leakage currents are not generally a concern, although noise in the circuit increases as the value of $R_F$ increases. In addition, a certain range of $R_F$ values is required for proper start-up operation of the amplifier. Taken together, it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in Equation 2.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \quad (2)$$

As an example, consider an input resistance of 20 kΩ and a feedback resistor of 20 kΩ. The gain of the amplifier would be –1 and the effective impedance at the inverting terminal would be 10 kΩ, which is within the recommended range.

For high-performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of $R_F$ above 50 kΩ, the amplifier tends to become unstable due to a pole formed from $R_F$ and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with $R_F$. In effect, this creates a low-pass filter network with the cutoff frequency defined in Equation 3.

$$f_{c(lowpass)} = \frac{1}{2\pi R_F C_F} \quad (3)$$

For example, if $R_F$ is 100 kΩ and $C_F$ is 5 pF, then $f_{c(lowpass)}$ is 318 kHz, which is well outside the audio range.

### INPUT CAPACITOR $C_I$

In the typical application, an input capacitor, $C_I$, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, $C_I$ and $R_I$ form a high-pass filter with the corner frequency determined in Equation 4.

$$f_{c(highpass)} = \frac{1}{2\pi R_I C_I} \quad (4)$$

The value of $C_I$ is important to consider, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where $R_I$ is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as Equation 5.

$$C_I = \frac{1}{2\pi R_I f_{c(highpass)}} \quad (5)$$

In this example, $C_I$ is 0.4 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network ($R_I$, $C_I$) and the feedback resistor ($R_F$) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (> 10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

## APPLICATION INFORMATION (continued)

### POWER SUPPLY DECOUPLING, $C_S$

The TPA122 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device $V_{DD}$ lead, works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the power amplifier is recommended.

### MIDRAIL BYPASS CAPACITOR, $C_B$

The midrail bypass capacitor, $C_B$, serves several important functions. During start-up, $C_B$ determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 160-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in Equation 6 should be maintained.

$$\frac{1}{\left(C_B \times 160\ \text{k}\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \tag{6}$$

As an example, consider a circuit where $C_B$ is 1 µF, $C_I$ is 1 µF, and $R_I$ is 20 kΩ. Inserting these values into Equation 6 results in: 6.25 ≤ 50 which satisfies the rule. Bypass capacitor, $C_B$, values of 0.1-µF to 1-µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

### OUTPUT COUPLING CAPACITOR, $C_C$

In the typical single-supply, single-ended (SE) configuration, an output coupling capacitor ($C_C$) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 7.

$$f_C = \frac{1}{2\pi R_L C_C} \tag{7}$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of $C_C$ are required to pass low frequencies into the load. Consider the example where a $C_C$ of 68 µF is chosen and loads vary from 32 Ω to 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

**Table 1. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode**

| $R_L$ | $C_C$ | LOWEST FREQUENCY |
|---|---|---|
| 32 Ω | 68 µF | 73 Hz |
| 10,000 Ω | 68 µF | 0.23 Hz |
| 47,000 Ω | 68 µF | 0.05 Hz |

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is good.

The output coupling capacitor required in single-supply, SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{\left(C_B \times 160\ k\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \ll \frac{1}{R_L C_C} \quad (8)$$

## USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

## 5-V VERSUS 3.3-V OPERATION

The TPA122 was designed for operation over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation because these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in the TPA122 can produce a maximum voltage swing of $V_{DD}$ – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V, as opposed to $V_{O(PP)}$ = 4 V for 5-V operation. The reduced voltage swing subsequently reduces maximum output power into the load before distortion begins to become significant.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPA122D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TPA122 | Samples |
| TPA122DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TPA122 | Samples |
| TPA122DGN | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAE | Samples |
| TPA122DGNG4 | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAE | Samples |
| TPA122DGNR | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AAE | Samples |
| TPA122DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TPA122 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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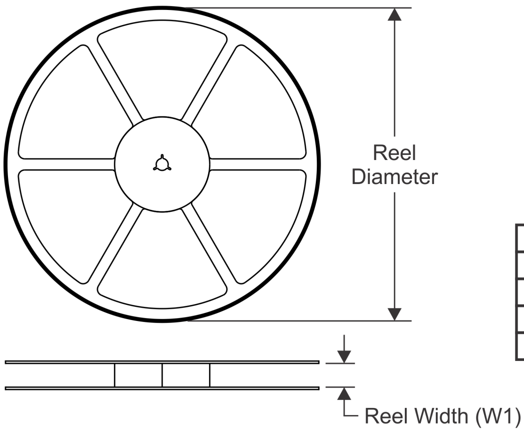
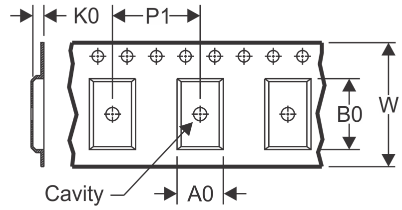
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

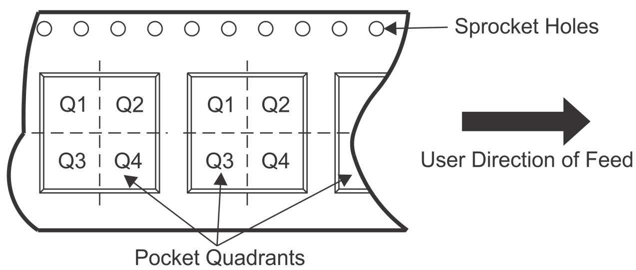



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

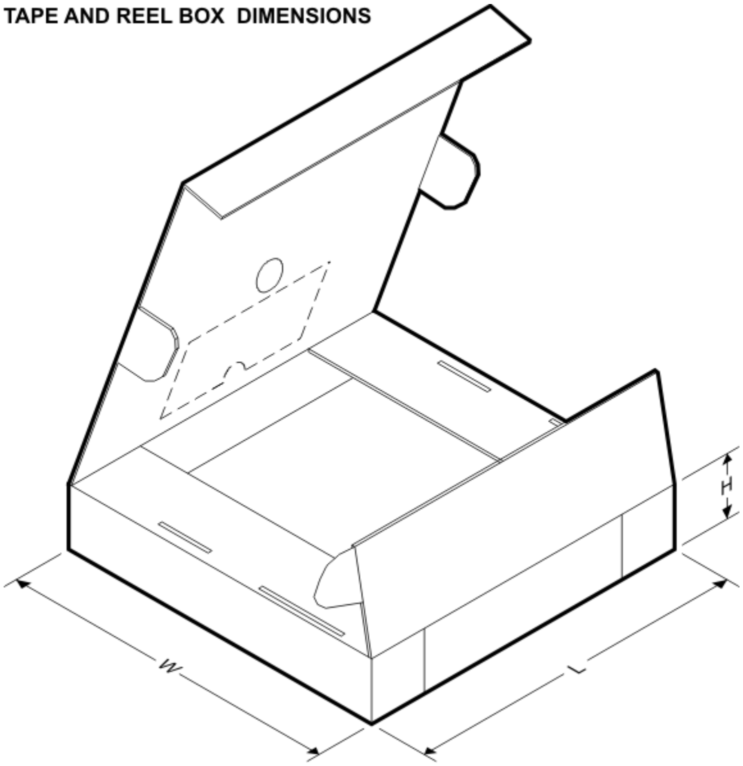
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPA122DGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPA122DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

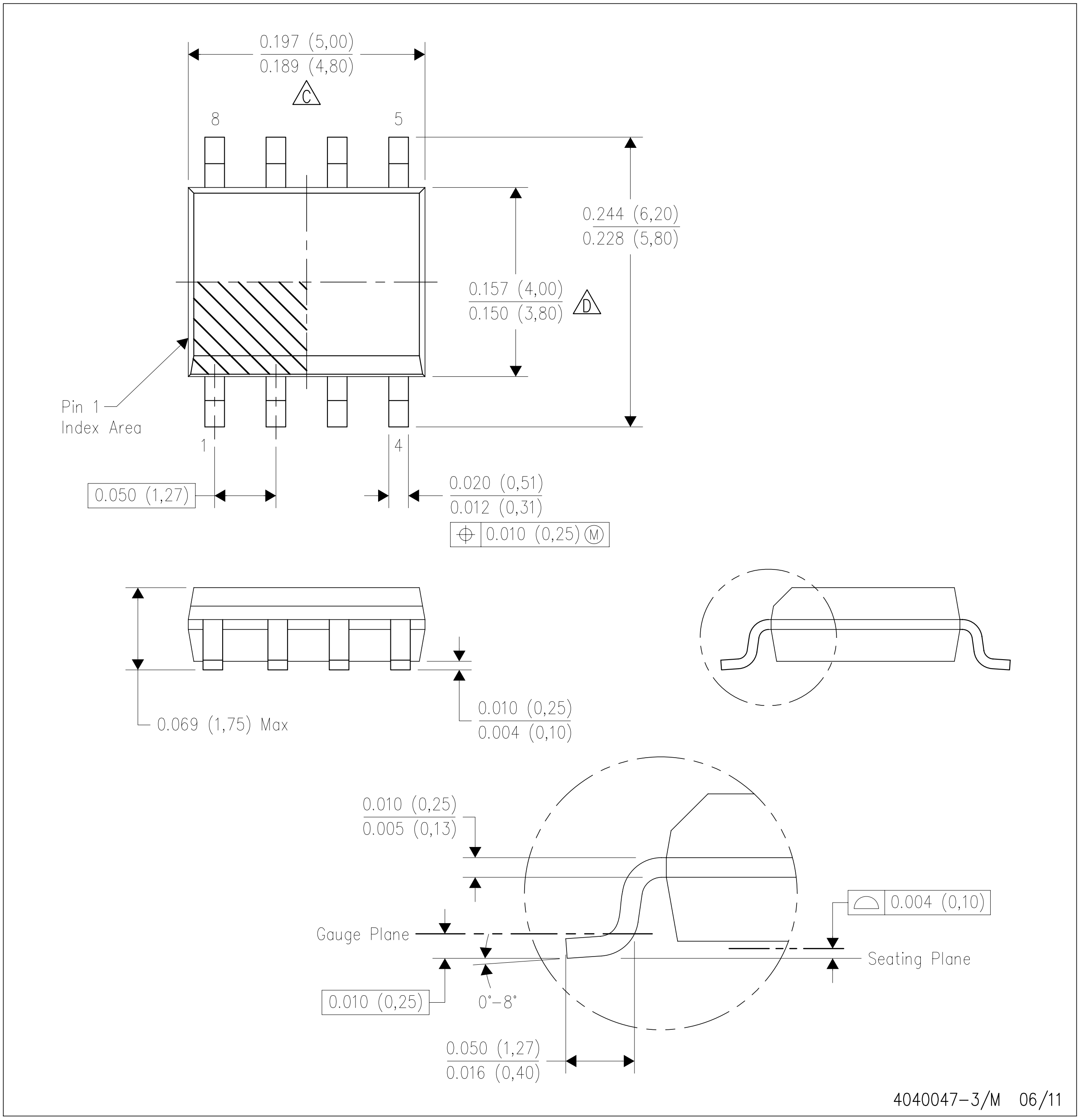
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

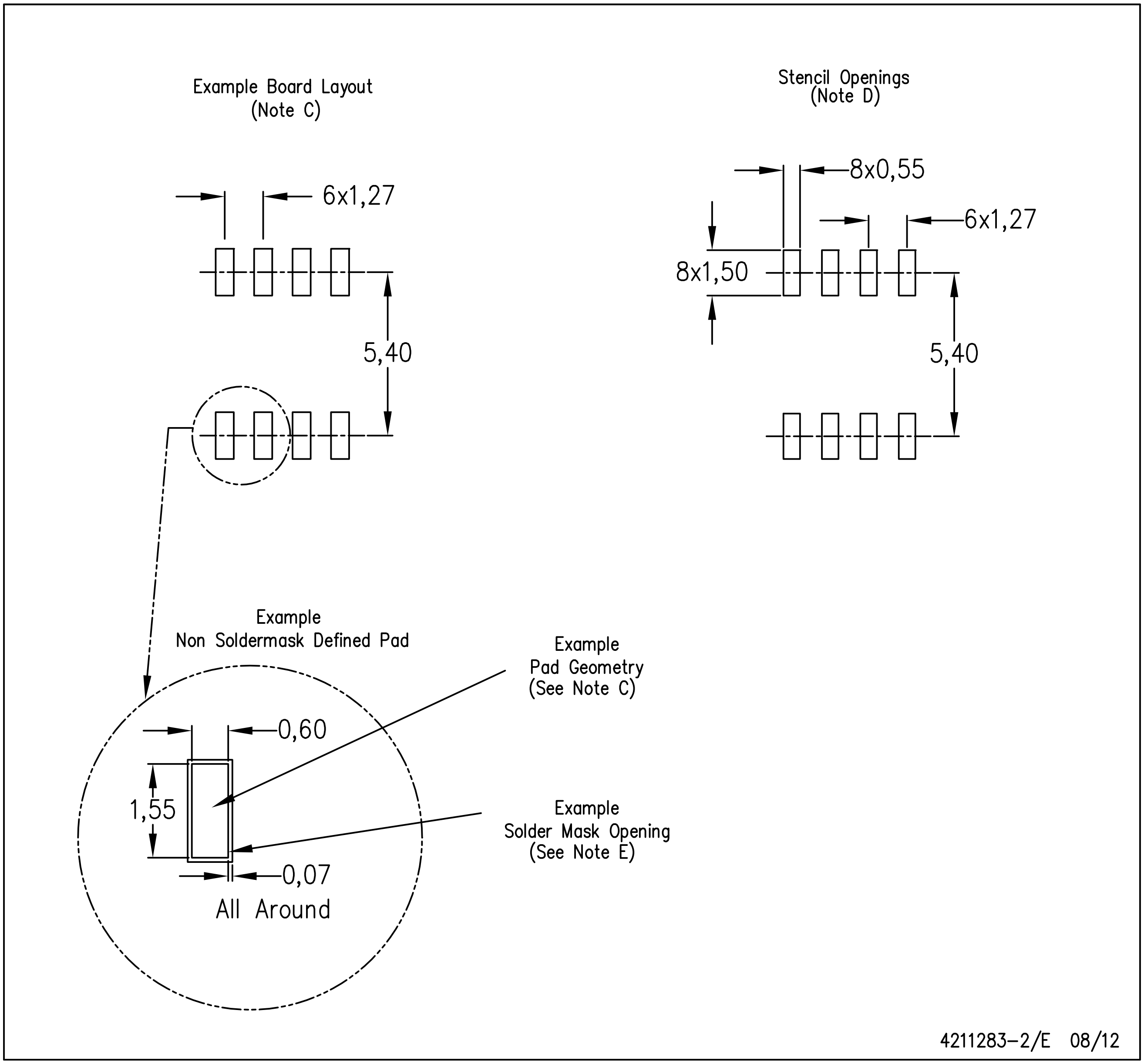
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPA122DGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPA122DR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 38.0 |

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



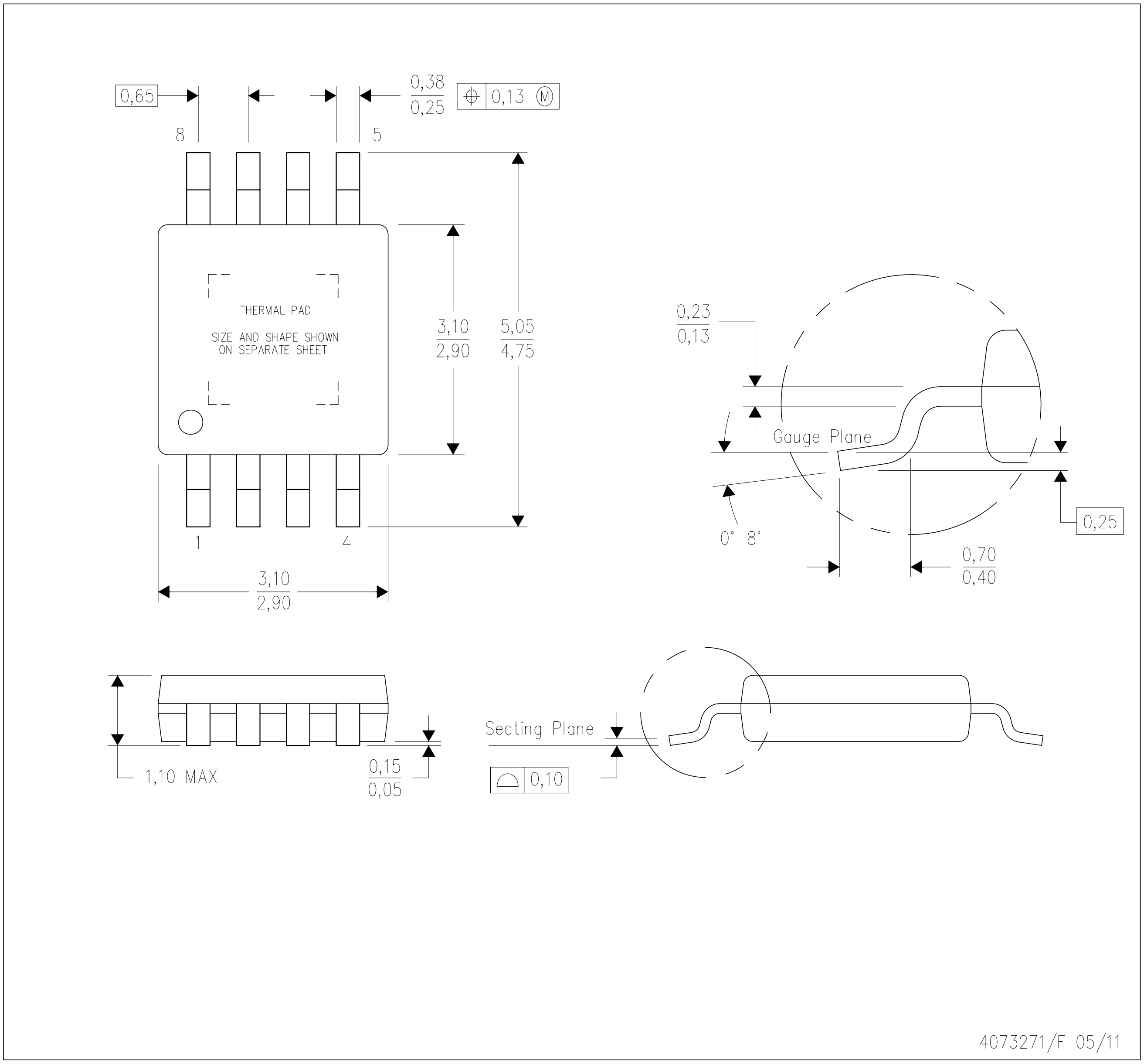

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–187 variation AA–T

**PowerPAD is a trademark of Texas Instruments.**

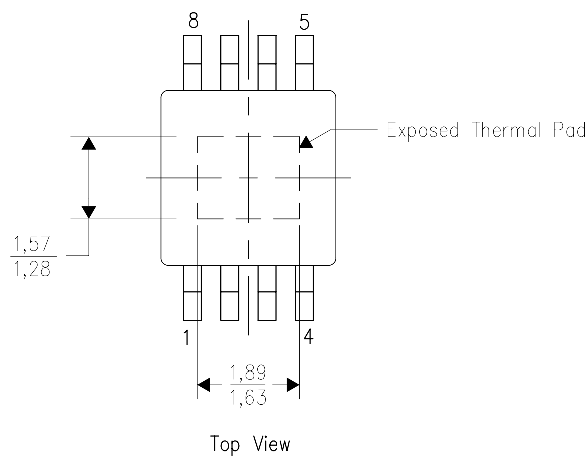
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



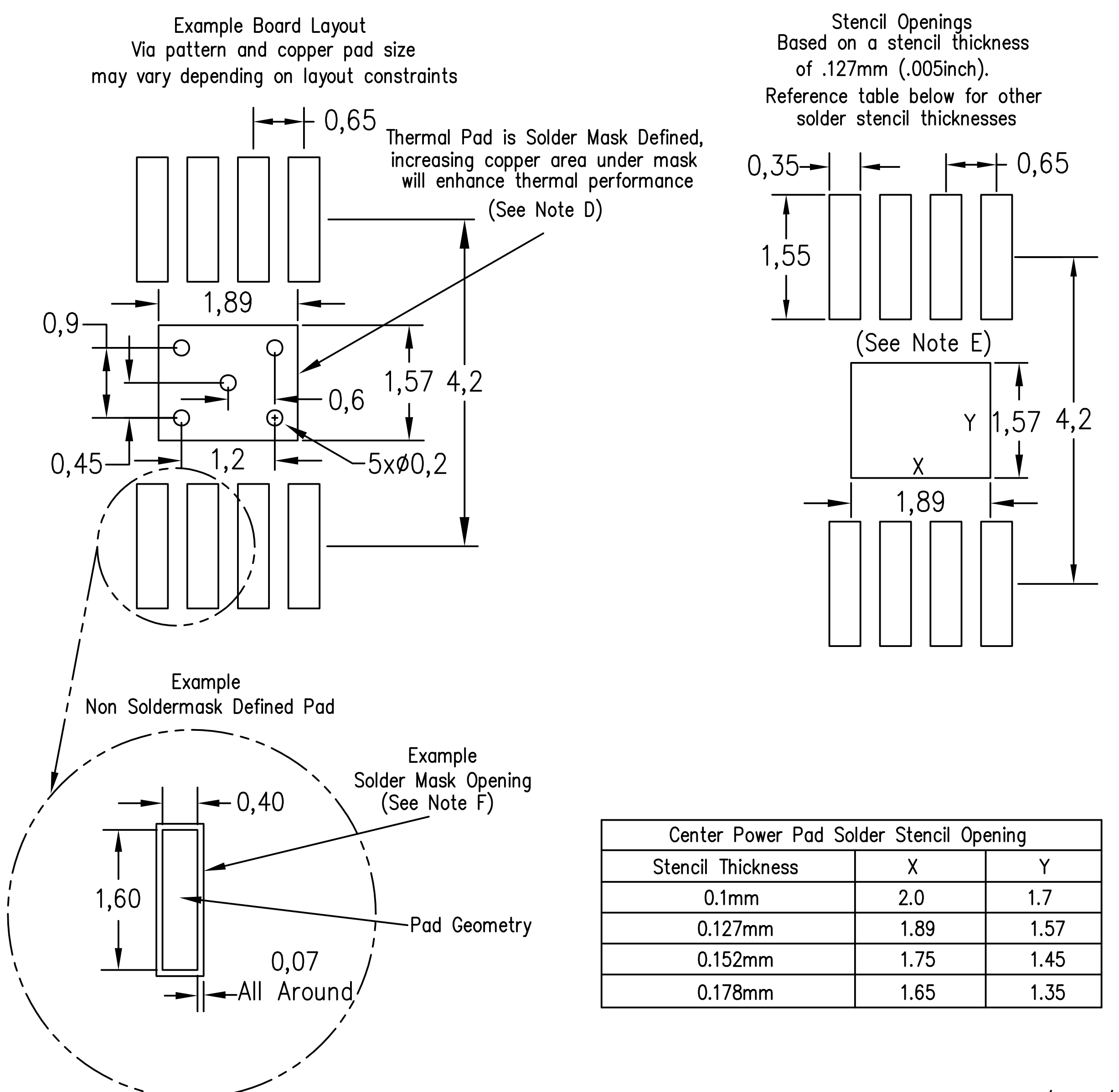

Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.0 | 1.7 |
| 0.127mm | 1.89 | 1.57 |
| 0.152mm | 1.75 | 1.45 |
| 0.178mm | 1.65 | 1.35 |

4207737-2/F 02/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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