



## 50-mW ULTRALOW VOLTAGE STEREO HEADPHONE AUDIO POWER AMPLIFIER

### FEATURES

- 50-mW Stereo Output
- Low Supply Current . . . 0.75 mA
- Low Shutdown Current . . . 50 nA
- Pin Compatible With LM4881 and TPA102 <sup>(1)</sup>
- Pop Reduction Circuitry
- Internal Midrail Generation
- Thermal and Short-Circuit Protection
- Surface-Mount Packaging
  - MSOP and SOIC
- 1.6-V to 3.6-V Supply Voltage Range

(1) The polarity of the  $\overline{\text{SHUTDOWN}}$  pin is reversed.

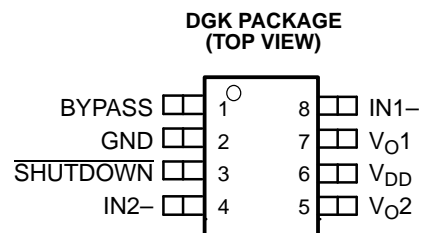
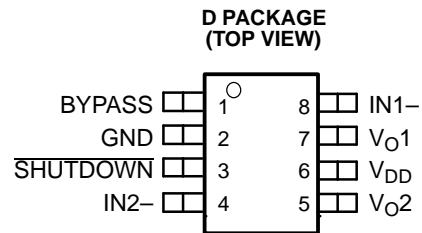
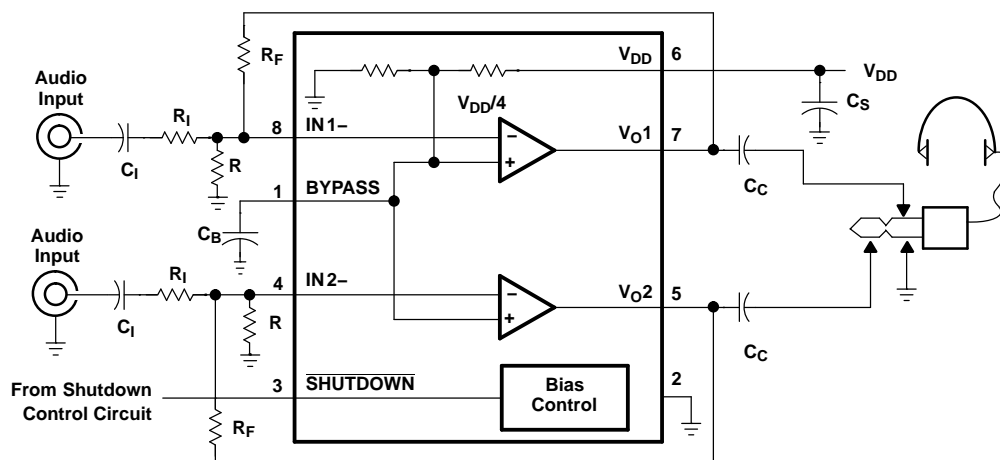
### DESCRIPTION

The TPA6100A2D is a stereo audio power amplifier packaged in either an 8-pin SOIC package or an 8-pin MSOP package capable of delivering 50 mW of continuous RMS power per channel into 16- $\Omega$  loads. Amplifier gain is externally configured by a means of three resistors per input channel and does not require external compensation for settings of 1 to 10.

The TPA6100A2D is optimized for battery applications because of its low supply current, shutdown current, and THD+N. To obtain the low-supply voltage range, the TPA6100A2D biases  $\overline{\text{BYPASS}}$  to  $V_{DD}/4$ . A resistor with a resistance equal to  $R_F$  must be added from the inputs to ground to allow the output to be biased at  $V_{DD}/2$ .

When driving a 16- $\Omega$  load with 45-mW output power from 3.3 V, THD+N is 0.04% at 1 kHz, and less than 0.2% across the audio band of 20 Hz to 20 kHz. For 28 mW into 32- $\Omega$  loads, the THD+N is reduced to less than 0.03% at 1 kHz, and is less than 0.2% across the audio band of 20 Hz to 20 kHz.

### TYPICAL APPLICATION CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**AVAILABLE OPTIONS**

T <sub>A</sub>	PACKAGED DEVICE		MSOP SYMBOLIZATION
	SMALL OUTLINE (D)	MSOP(DGK)	
–40°C to 85°C	TPA6100A2D	TPA6100A2DGK	AJL

**Terminal Functions**

TERMINAL NAME	NO.	I/O	DESCRIPTION
BYPASS	1	I	Tap to voltage divider for internal mid-supply bias supply. BYPASS is set at V <sub>DD</sub> /4. Connect to a 0.1-μF to 1-μF low-ESR capacitor for best performance.
GND	2	I	GND is the ground connection.
IN1-	8	I	IN1- is the inverting input for channel 1.
IN2-	4	I	IN2- is the inverting input for channel 2.
SHUTDOWN	3	I	Active-low input. When held low, the device is placed in a low supply current mode.
V <sub>DD</sub>	6	I	V <sub>DD</sub> is the supply voltage terminal.
V <sub>O1</sub>	7	O	V <sub>O1</sub> is the audio output for channel 1.
V <sub>O2</sub>	5	O	V <sub>O2</sub> is the audio output for channel 2.

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	UNIT
V <sub>DD</sub> Supply voltage	4 V
V <sub>I</sub> Input voltage	–0.3 V to V <sub>DD</sub> + 0.3 V
Continuous total power dissipation	Internally limited
T <sub>J</sub> Operating junction temperature range	–40°C to 150°C
T <sub>stg</sub> Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**DISSIPATION RATING TABLE**

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
D	710 mW	5.68 mW/°C	454 mW	369 mW
DGK	469 mW	3.75 mW/°C	300 mW	244 mW

**RECOMMENDED OPERATING CONDITIONS**

	MIN	MAX	UNIT
V <sub>DD</sub> Supply voltage	1.6	3.6	V
T <sub>A</sub> Operating free-air temperature	–40	85	°C
V <sub>IH</sub> High-level input voltage	SHUTDOWN		V
V <sub>IL</sub> Low-level input voltage	SHUTDOWN		
	0.6 x V <sub>DD</sub>		
	0.25 x V <sub>DD</sub>		

## DC ELECTRICAL CHARACTERISTICS

 at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.6\text{ V}$  (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OO}$	Output offset voltage	$A_V = 2\text{ V/V}$		5	40	mV
PSRR	Power supply rejection ratio	$V_{DD} = 3.0\text{ V to } 3.6\text{ V}$		72		dB
$I_{DD}$	Supply current	$\overline{\text{SHUTDOWN}} = 3.6\text{ V}$		0.75	2.0	mA
$I_{DD(\text{SD})}$	Supply current in $\overline{\text{SHUTDOWN}}$ mode	$\overline{\text{SHUTDOWN}} = 0\text{ V}$		50	250	nA
$ I_{IH} $	High-level input current ( $\overline{\text{SHUTDOWN}}$ )	$V_{DD} = 3.6\text{ V}$ , $V_I = V_{DD}$			1	$\mu\text{A}$
$ I_{IL} $	Low-level input current ( $\overline{\text{SHUTDOWN}}$ )	$V_{DD} = 3.6\text{ V}$ , $V_I = 0\text{ V}$			1	$\mu\text{A}$
$Z_I$	Input impedance (IN1-, IN2-)			> 1		M $\Omega$

## AC OPERATING CHARACTERISTICS

 $V_{DD} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 16\ \Omega$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_O$	Output power (each channel)	THD $\leq 0.1\%$ , $f = 1\text{ kHz}$		50		mW
THD+N	Total harmonic distortion + noise	$P_O = 45\text{ mW}$ , 20 Hz–20 kHz		0.2%		
$B_{OM}$	Maximum output power BW	$G = 1$ , THD $< 0.5\%$		> 20		kHz
$k_{SVR}$	Supply ripple rejection	$f = 1\text{ kHz}$		52		dB
SNR	Signal-to-noise ratio	$P_O = 50\text{ mW}$		90		dB
$V_n$	Noise output voltage (no noise-weighting filter)			28		$\mu\text{V(rms)}$

## AC OPERATING CHARACTERISTICS

 $V_{DD} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 32\ \Omega$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_O$	Output power (each channel)	THD $\leq 0.1\%$ , $f = 1\text{ kHz}$		35		mW
THD+N	Total harmonic distortion + noise	$P_O = 30\text{ mW}$ , 20 Hz–20 kHz		0.2%		
$B_{OM}$	Maximum output power BW	$G = 1$ , THD $< 0.2\%$		> 20		kHz
$k_{SVR}$	Supply ripple rejection	$f = 1\text{ kHz}$		52		dB
SNR	Signal-to-noise ratio	$P_O = 35\text{ mW}$		91		dB
$V_n$	Noise output voltage (no noise-weighting filter)			28		$\mu\text{V(rms)}$

**DC ELECTRICAL CHARACTERISTICS**at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 1.6\text{ V}$  (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OO}$	Output offset voltage	$A_V = 2\text{ V/V}$		5	40	mV
PSRR	Power supply rejection ratio	$V_{DD} = 1.5\text{ V to }1.7\text{ V}$		80		dB
$I_{DD}$	Supply current	SHUTDOWN = 1.6 V		1.2	1.5	mA
$I_{DD(SD)}$	Supply current in SHUTDOWN mode	SHUTDOWN = 0 V		50	250	nA
$ I_{IH} $	High-level input current (SHUTDOWN)	$V_{DD} = 1.6\text{ V}$ , $V_I = V_{DD}$			1	$\mu\text{A}$
$ I_{IL} $	Low-level input current (SHUTDOWN)	$V_{DD} = 1.6\text{ V}$ , $V_I = 0\text{ V}$			1	$\mu\text{A}$
$Z_I$	Input impedance (IN1-, IN2-)			> 1		M $\Omega$

**AC OPERATING CHARACTERISTICS** $V_{DD} = 1.6\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 16\ \Omega$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_O$	Output power (each channel)	THD $\leq 0.1\%$ , $f = 1\text{ kHz}$		9.5		mW
THD+N	Total harmonic distortion + noise	$P_O = 9.5\text{ mW}$ , 20 Hz–20 kHz		0.4%		
$B_{OM}$	Maximum output power BW	$G = 0\text{ dB}$ , THD $< 0.4\%$		> 20		kHz
$k_{SVR}$	Supply ripple rejection	$f = 1\text{ kHz}$		53		dB
SNR	Signal-to-noise ratio	$P_O = 9.5\text{ mW}$		86		dB
$V_n$	Noise output voltage (no noise-weighting filter)			18		$\mu\text{V(rms)}$

**AC OPERATING CHARACTERISTICS** $V_{DD} = 1.6\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 32\ \Omega$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_O$	Output power (each channel)	THD $\leq 0.1\%$ , $f = 1\text{ kHz}$		7.1		mW
THD+N	Total harmonic distortion + noise	$P_O = 6.5\text{ mW}$ , 20 Hz–20 kHz		0.3%		
$B_{OM}$	Maximum output power BW	$G = 0\text{ dB}$ , THD $< 0.3\%$		> 20		kHz
$k_{SVR}$	Supply ripple rejection	$f = 1\text{ kHz}$		53		dB
SNR	Signal-to-noise ratio	$P_O = 7.1\text{ mW}$		88		dB
$V_n$	Noise output voltage (no noise-weighting filter)			18		$\mu\text{V(rms)}$

## APPLICATION INFORMATION

### GAIN SETTING RESISTORS, $R_F$ , $R_I$ , and $R$

The voltage gain for the TPA6100A2D is set by resistors  $R_F$  and  $R_I$  according to Equation 1.

$$\text{Gain} = - \left( \frac{R_F}{R_I} \right) \text{ or Gain (dB)} = 20 \log \left( \frac{R_F}{R_I} \right) \quad (1)$$

Given that the TPA6100A2D is an MOS amplifier, the input impedance is high. Consequently, input leakage currents are not generally a concern, although noise in the circuit increases as the value of  $R_F$  increases. In addition, a certain range of  $R_F$  values is required for proper start-up operation of the amplifier. Taken together, it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 k $\Omega$  and 20 k $\Omega$ . The effective impedance is calculated in Equation 2.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \quad (2)$$

As an example, consider an input resistance of 20 k $\Omega$  and a feedback resistor of 20 k $\Omega$ . The gain of the amplifier would be  $-1$  and the effective impedance at the inverting terminal would be 10 k $\Omega$ , which is within the recommended range.

For high-performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of  $R_F$  above 50 k $\Omega$ , the amplifier tends to become unstable due to a pole formed from  $R_F$  and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with  $R_F$ . In effect, this creates a low-pass filter network with the cutoff frequency defined in Equation 3.

$$f_c = \frac{1}{2\pi R_F C_F} \quad (3)$$

For example, if  $R_F$  is 100 k $\Omega$  and  $C_F$  is 5 pF, then  $f_c$  is 318 kHz, which is well outside the audio range.

For maximum signal swing and output power at low supply voltages like 1.6 V to 3.3 V, BYPASS is biased to  $V_{DD}/4$ . However, to allow the output to be biased at  $V_{DD}/2$ , a resistor,  $R$ , equal to  $R_F$  must be placed from the negative input to ground.

### INPUT CAPACITOR, $C_I$

In the typical application, an input capacitor,  $C_I$ , is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case,  $C_I$  and  $R_I$  form a high-pass filter with the corner frequency determined in Equation 4.

$$f_c = \frac{1}{2\pi R_I C_I} \quad (4)$$

The value of  $C_I$  is important to consider, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where  $R_I$  is 20 k $\Omega$  and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as Equation 5.

$$C_I = \frac{1}{2\pi R_I f_c} \quad (5)$$

In this example,  $C_I$  is 0.4  $\mu\text{F}$ , so one would likely choose a value in the range of 0.47  $\mu\text{F}$  to 1  $\mu\text{F}$ . A further consideration for this capacitor is the leakage path from the input source through the input network ( $R_I$ ,  $C_I$ ) and the feedback resistor ( $R_F$ ) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications ( $>10$ ). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at  $V_{DD}/4$ , which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

## APPLICATION INFORMATION (continued)

### POWER SUPPLY DECOUPLING, $C_S$

The TPA6100A2D is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1  $\mu\text{F}$ , placed as close as possible to the device  $V_{DD}$  lead, works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 10  $\mu\text{F}$  or greater placed near the power amplifier is recommended.

### MIDRAIL BYPASS CAPACITOR, $C_B$

The midrail bypass capacitor ( $C_B$ ) serves several important functions. During start-up,  $C_B$  determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 55-k $\Omega$  source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in Equation 6 should be maintained.

$$\frac{1}{(C_B \times 55 \text{ k}\Omega)} \leq \frac{1}{(C_1 R_1)} \quad (6)$$

As an example, consider a circuit where  $C_B$  is 1  $\mu\text{F}$ ,  $C_1$  is 1  $\mu\text{F}$ , and  $R_1$  is 20 k $\Omega$ . Inserting these values into Equation 6 results in:  $18.18 \leq 50$  which satisfies the rule. Bypass capacitor ( $C_B$ ) values of 0.47- $\mu\text{F}$  to 1- $\mu\text{F}$  ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

### OUTPUT COUPLING CAPACITOR, $C_C$

In the typical single-supply, single-ended (SE) configuration, an output coupling capacitor ( $C_C$ ) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 7.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (7)$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of  $C_C$  are required to pass low frequencies into the load. Consider the example where a  $C_C$  of 68  $\mu\text{F}$  is chosen and loads vary from 32  $\Omega$  to 47 k $\Omega$ . Table 1 summarizes the frequency response characteristics of each configuration.

**Table 1. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode**

$R_L$	$C_C$	LOWEST FREQUENCY
32 $\Omega$	68 $\mu\text{F}$	73 Hz
10,000 $\Omega$	68 $\mu\text{F}$	0.23 Hz
47,000 $\Omega$	68 $\mu\text{F}$	0.05 Hz

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is good.

The output coupling capacitor required in single-supply, SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{(C_B \times 55 \text{ k}\Omega)} \leq \frac{1}{(C_I R_I)} \ll \frac{1}{R_L C_C} \quad (8)$$

### USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

### 3.3-V VERSUS 1.6-V OPERATION

The TPA6100A2D was designed for operation over a supply range of 1.6 V to 3.6 V. There are no special considerations for 1.6-V versus 3.3-V operation as far as supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier can produce a maximum output voltage swing within a few hundred millivolts of the rails with a 10-k $\Omega$  load. However, this voltage swing decreases as the load resistance decreases and the  $r_{DS(on)}$  as the output stage transistors becomes more significant. For example, for a 32- $\Omega$  load, the maximum peak output voltage with  $V_{DD} = 1.6$  V is approximately 0.7 V with no clipping distortion. This reduced voltage swing effectively reduces the maximum undistorted output power.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA6100A2D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6100A2	<a href="#">Samples</a>
TPA6100A2DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJL	<a href="#">Samples</a>
TPA6100A2DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJL	<a href="#">Samples</a>
TPA6100A2DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJL	<a href="#">Samples</a>
TPA6100A2DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJL	<a href="#">Samples</a>
TPA6100A2DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6100A2	<a href="#">Samples</a>
TPA6100A2DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6100A2	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

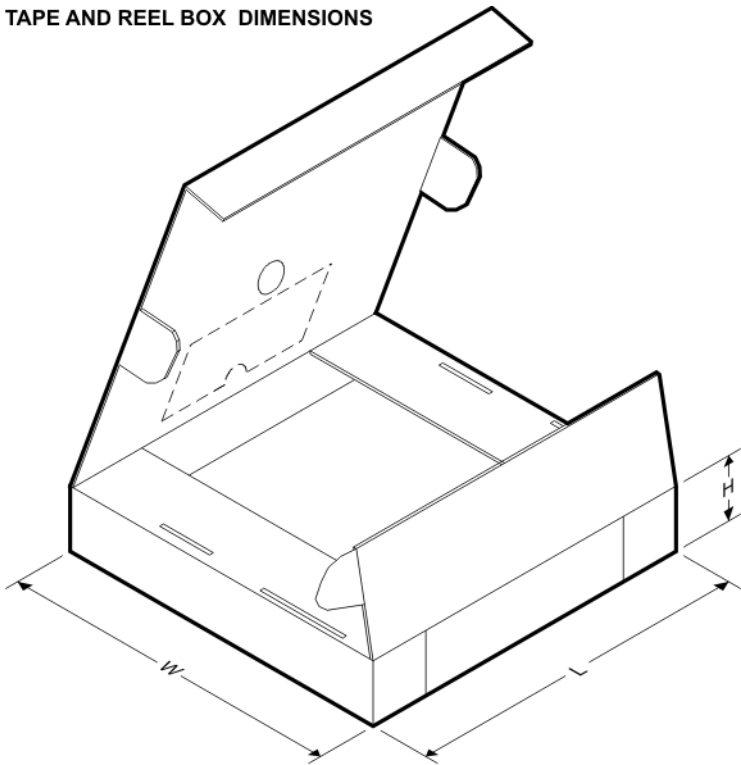


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6100A2DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA6100A2DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6100A2DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TPA6100A2DR	SOIC	D	8	2500	367.0	367.0	38.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.