TPD13S523 13-Channel ESD Protection Solution With Current-Limit Load Switch For HDMI Transmitter Ports

1 Features

- IEC 61000-4-2 Level 4 Contact ESD Protection
  - ±12-kV Contact Discharge on External Lines
- Single-Chip ESD Solution for HDMI 1.4 and HDMI 1.3 Interface
- On-Chip 5-V Load Switch With Current Limit and Reverse Current Protection
- Supports UTILITY Line Protection for HDMI 1.4 Audio Return Line
- <0.05-pF Differential Capacitance Between the TMDS Signal Pair
- Industry Standard 16-TSSOP and Space-Saving 16-RSV Package
- Supports Data Rates in Excess of 3.4 Gbps
- R_{DYN} = 0.5 Ω (Typical)
- Commercial Temperature Range: –40°C to 85°C

2 Applications

- End Equipment
  - Set Top Boxes
  - E-Books
  - Tablets
  - Smart Phones
  - Camcorders
- Interfaces
  - HDMI

3 Description

The TPD13S523 device is a single-chip integrated IEC 61000-4-2 ESD protection solution for HDMI 1.4 or HDMI 1.3 interfaces. This device offers 13 channels of TVS diodes with flow-through pin mapping that matches HDMI connector high-speed lines. While providing ESD protection, the TPD13S523 adds little to no additional distortion to the high-speed differential signals. The monolithic integrated circuit technology ensures that there is excellent matching between the two-signal pair of the differential line (< 0.05-pF differential matching between TMDS lines). This offers an advantage over discrete ESD solutions where variations between two different ESD protection circuits may significantly degrade the differential signal quality.

The TPD13S523 incorporates an on-chip current limited load switch that is compliant with HDMI 5-V out electrical specifications. The short-circuit protection at 5V_OUT ensures that the device is not damaged in case there is an accidental short to GND. The load switch also incorporates a reverse-current blocking feature which ensures that the HDMI driver side is not erroneously turned on when two HDMI drivers are connected together.

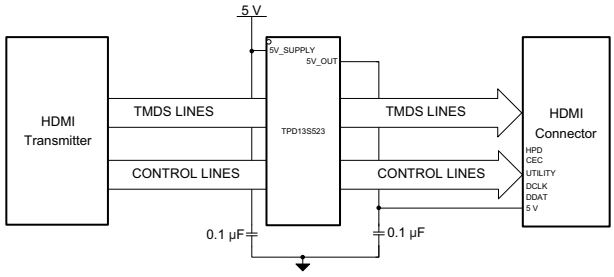
Typical applications for the TPD13S523 include set top boxes (STB), e-books, tablets, smart phones, and camcorders.

Device Information(1)

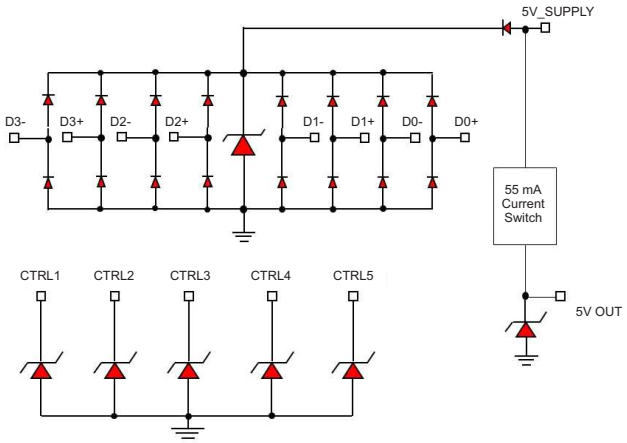
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD13S523	TSSOP (16)	5.00 mm × 4.40 mm
	UQFN (16)	2.60 mm × 1.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Schematic for HDMI Transmitter Port



Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2015) to Revision D — **Page**

- Added table note to *Absolute Maximum Ratings* ... 4
- Added test condition frequency to capacitance ... 5

Changes from Revision B (December 2012) to Revision C — **Page**

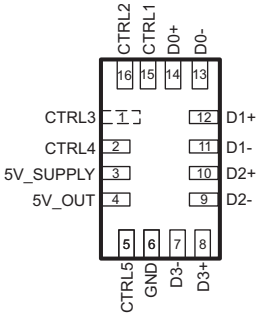
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (May 2012) to Revision B — **Page**

- Added RSV package to ORDERING INFORMATION table ... 1
- Removed PREVIEW status from RSV package ... 3

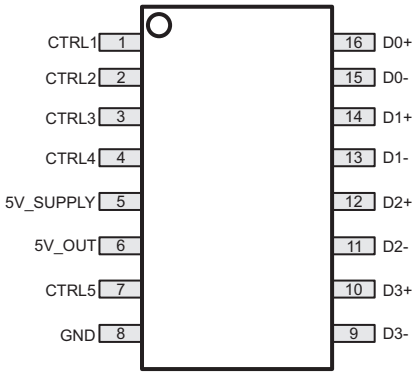
5 Pin Configuration and Functions

RSV Package
16-Pin UQFN
Top View



All the CTRLx pins have the same ESD circuit and are interchangeable.

PW Package
16-Pin TSSOP
Top View



All the CTRLx pins have the same ESD circuit and are interchangeable.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	UQFN	TSSOP		
CTRL1	15	1	I/O	ESD Clamp for Control Lines: provides ESD protection to HDMI control lines: CEC, SCL, SDA, HPD, and UTILITY. All the control pins have the same ESD circuit and are interchangeable.(1)
CTRL2	16	2	I/O	ESD Clamp for Control Lines: provides ESD protection to HDMI control lines: CEC, SCL, SDA, HPD, and UTILITY. All the control pins have the same ESD circuit and are interchangeable.(1)
CTRL3	1	3	I/O	ESD Clamp for Control Lines: provides ESD protection to HDMI control lines: CEC, SCL, SDA, HPD, and UTILITY. All the control pins have the same ESD circuit and are interchangeable.(1)
CTRL4	2	4	I/O	ESD Clamp for Control Lines: provides ESD protection to HDMI control lines: CEC, SCL, SDA, HPD, and UTILITY. All the control pins have the same ESD circuit and are interchangeable.(1)
CTRL5	5	7	I/O	ESD Clamp for Control Lines: provides ESD protection to HDMI control lines: CEC, SCL, SDA, HPD, and UTILITY. All the control pins have the same ESD circuit and are interchangeable.(1)
5V_SUPPLY	3	5	I	**Supply Pin for HDMI 5V_OUT** 5 V, connects to internal VCC plane on the PCB board; connect a 0.1 to 1-µF capacitor shunt to ground.
5V_OUT	4	6	O	**Current Limited HDMI 5V_OUT:** connect to HDMI 5V_OUT; offers IEC61000-4-2 ESD protection; connect a 0.1 to 1-µF capacitor shunt to ground.
GND	6	8	G	Ground
D0+	14	16	I/O	High-speed ESD Clamp: provides ESD protection for TMDS lines.(1)
D0–	13	15	I/O	High-speed ESD Clamp: provides ESD protection for TMDS lines.(1)
D1+	12	14	I/O	High-speed ESD Clamp: provides ESD protection for TMDS lines.(1)
D1–	11	13	I/O	High-speed ESD Clamp: provides ESD protection for TMDS lines.(1)
D2+	10	12	I/O	High-speed ESD Clamp: provides ESD protection for TMDS lines.(1)
D2–	9	11	I/O	High-speed ESD Clamp: provides ESD protection for TMDS lines.(1)
D3+	8	10	I/O	High-speed ESD Clamp: provides ESD protection for TMDS lines.(1)
D3–	7	9	I/O	High-speed ESD Clamp: provides ESD protection for TMDS lines.(1)

(1) Connector pins are Dx+, Dx–, CTRLx, and 5V_OUT

6 Specifications

6.1 Absolute Maximum Ratings

T_A = –40°C to 85°C (1)

		MIN	MAX	UNIT
V_{CC} voltage tolerance	5V_SUPPLY	–0.3	6	V
IO voltage tolerance	Connector pins(2)	–0.3	6	V
IEC 61000-4-5 peak current (8/20 µs)	Connector pins(2)		3	A
IEC 61000-4-5 peak power (8/20 µs)	Connector pins(2)		30	W
Storage temperature, T_{stg}		–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Connector pins are Dx+, Dx–, CTRLx, and 5V_OUT

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
		IEC 61000-4-2 Contact Discharge	±12000	
		IEC 61000-4-2 Air-gap Discharge	±14000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_A = –40°C to 85°C

		MIN	MAX	UNIT
VCC Voltage	5V_SUPPLY	4.5	5.5	V
IO voltage at external signal pins	Signal Pins(1)	–0.3	5.5	V
Operating free-air temperature		–40	85	°C

(1) External Signal pins are Dx+, Dx–, CTRLx, and 5V_OUT

6.4 Thermal Information

THERMAL METRIC(1)		TPD13S523		UNIT
		PW [TSSOP]	RSV [UQFN]	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.9	153.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.5	70.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.0	74.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.7	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	n/a	74.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOAD SWITCH						
I_{CC}	Supply current at 5V_SUPPLY	5V_SUPPLY =5V, 5V OUT = Open	6.5	7	10	µA
I_{SC}	Short-circuit current at 5V_OUT	5V_SUPPLY =5V, 5V_OUT = GND	100	116	147	mA
$I_{BACKDRIVE}$	Reverse leakage current at 5VOUT	5V_SUPPLY =0V, 5V_OUT = 5 V		0.01	0.69	µA
V_{DROP}	5V_OUT output voltage drop	5V_SUPPLY =5V, I_{5V_OUT} = 55 mA		170	205	mV
CONNECTOR PINS						
V_{RWM}	Reverse stand-off voltage				5.5	V
V_{CLAMP}	Clamp voltage with ESD strike	Ipp = 1 A, 8/20 µs(1)			13	V
		Ipp = 3 A, 8/20 µs(1)			15	
I_{IO}	Leakage current through external signal pins(2)	5V_SUPPLY =5V, V_{IO} = 5 V	2	7	65	nA
I_{OFF}	Current from IO Port to supply pins when powered down through signal pins(3)	5V_SUPPLY = 0 V, V_{IO} = 2.5 V	1	5	44	nA
V_F	Diode forward voltage through external signal pins(2); lower clamp diode	I_D = 8 mA	0.7	0.85	0.95	V
R_{DYN}	Dynamic resistance of ESD clamps external pins(3)	Pin to ground(2)		0.5		Ω
C_{IO_TMDS}	IO capacitance Dx+, Dx– pins to GND	5V_SUPPLY = 5 V, V_{IO} = 2.5 V; f = 1 MHz		1		pF
ΔC_{IO_TMDS}	Differential capacitance for the Dx+, Dx– lines	5V_SUPPLY = 5 V, V_{IO} = 2.5 V; f = 1 MHz		0.05		pF
$C_{IO\_CONTROL}$	CTRLx pin capacitance	5V_SUPPLY = 5 V, V_{IO} = 2.5 V; f = 1 MHz		1		pF
V_{BR}	Break-down voltage through signal pins(3)	I_{IO} = 1 mA	6			V

(1) Non-repetitive current pulse of an 8/20 µs exponentially decaying waveform according to IEC 61000-4-5.
(2) Extraction of R_{DYN} using least squares fit of TLP characteristics between I=1A AND I=10A.
(3) Signal pins are Dx+, Dx–, and CTRLx.

6.6 Typical Characteristics

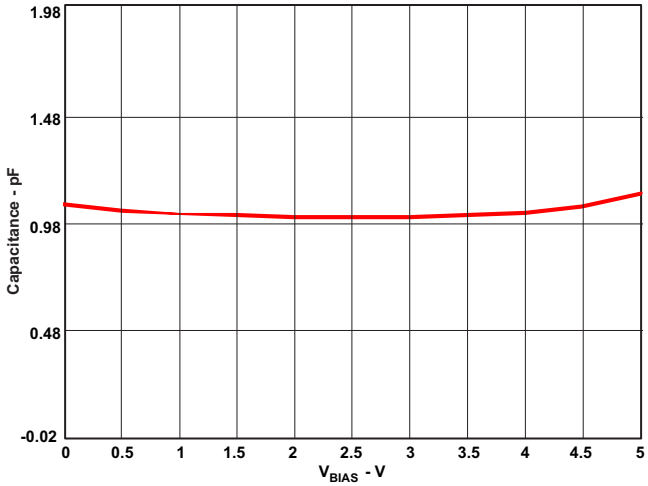


Figure 1. Pin Capacitance

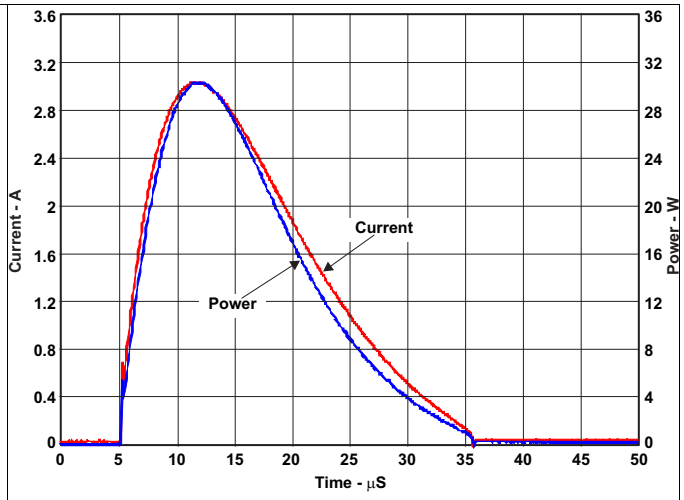


Figure 2. IEC 61000-4-5 (Surge) I_{PP} and P_{PP} Waveform

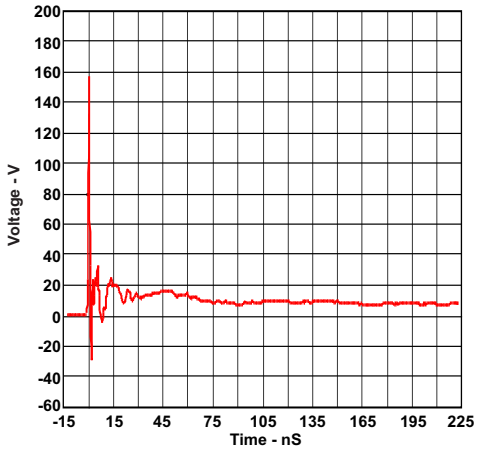


Figure 3. IEC Positive Clamping Waveform Using 8-kV Contact

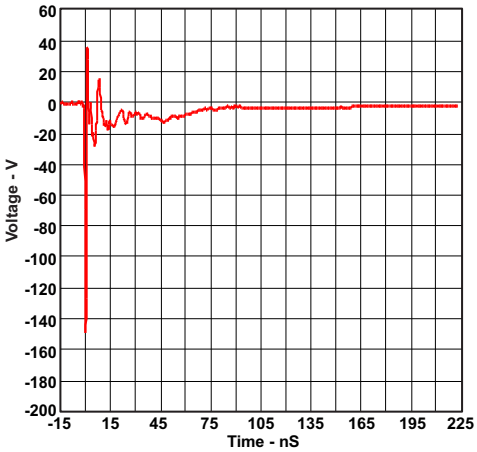


Figure 4. IEC Negative Clamping Waveform Using –8-kV Contact

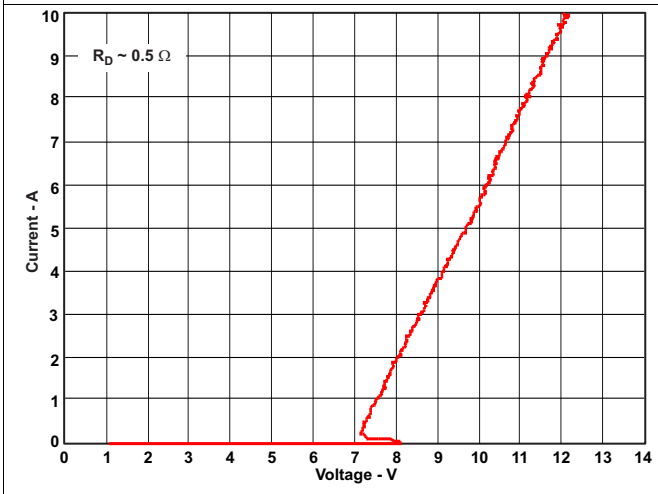


Figure 5. TLP Plot On Connector Pins

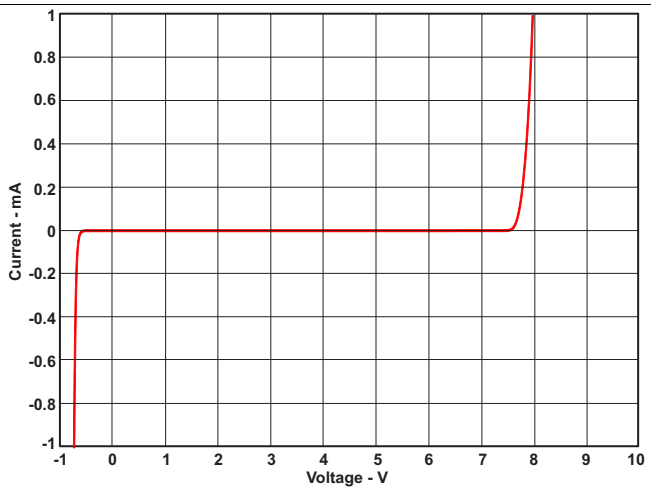
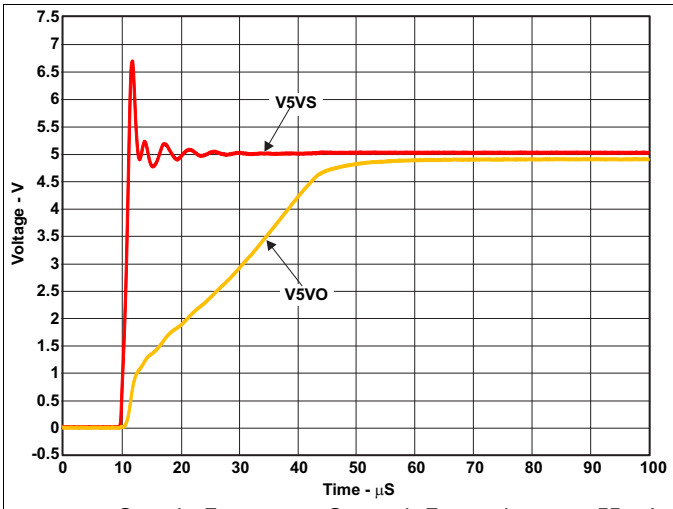


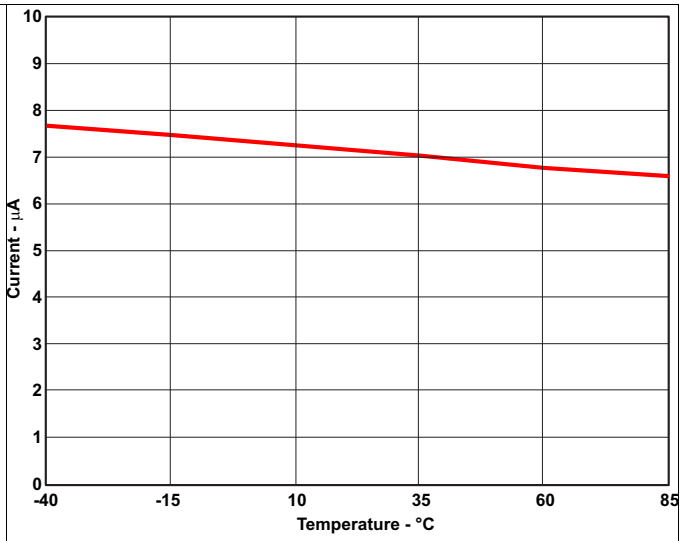
Figure 6. IV Curve On Signal Pins

Typical Characteristics (continued)



C_{IN} = 1 µF C_{OUT} = 1µF I_{SWITCH} = 55 mA
T_A = 25°C

Figure 7. Load Switch Start-Up Transient Waveform



5V_SUPPLY = 5 V 5V_OUT = Open

Figure 8. Load Switch Supply Current

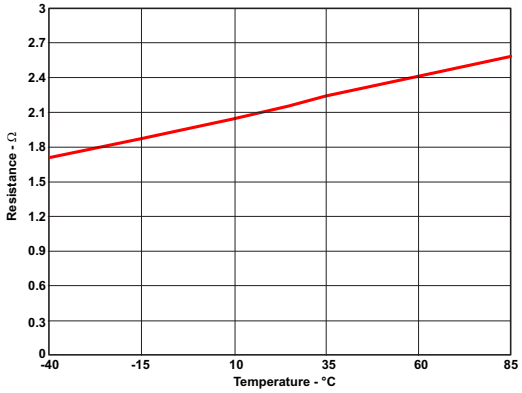


Figure 9. Load Switch Resistance vs Temperature

7 Detailed Description

7.1 Overview

The TPD13S523 device is a single-chip ESD solution for the HDMI transmitter port. By providing system-level ESD protection for a full HDMI port, the TPD13S523 can protect the core IC from ESD strikes and absorb the associated energy.

While providing the ESD protection, the TPD13S523 adds little-to-no signal distortion to the high-speed differential signals. In addition, the monolithic integrated circuit technology ensures that there is excellent matching between the two-signal pair of the differential line.

The TPD13S523 also provides an on-chip regulator with current output ratings of 55 mA at pin 38. This current enables HDMI receiver detection even when the receiver device is powered off.

7.2 Functional Block Diagram

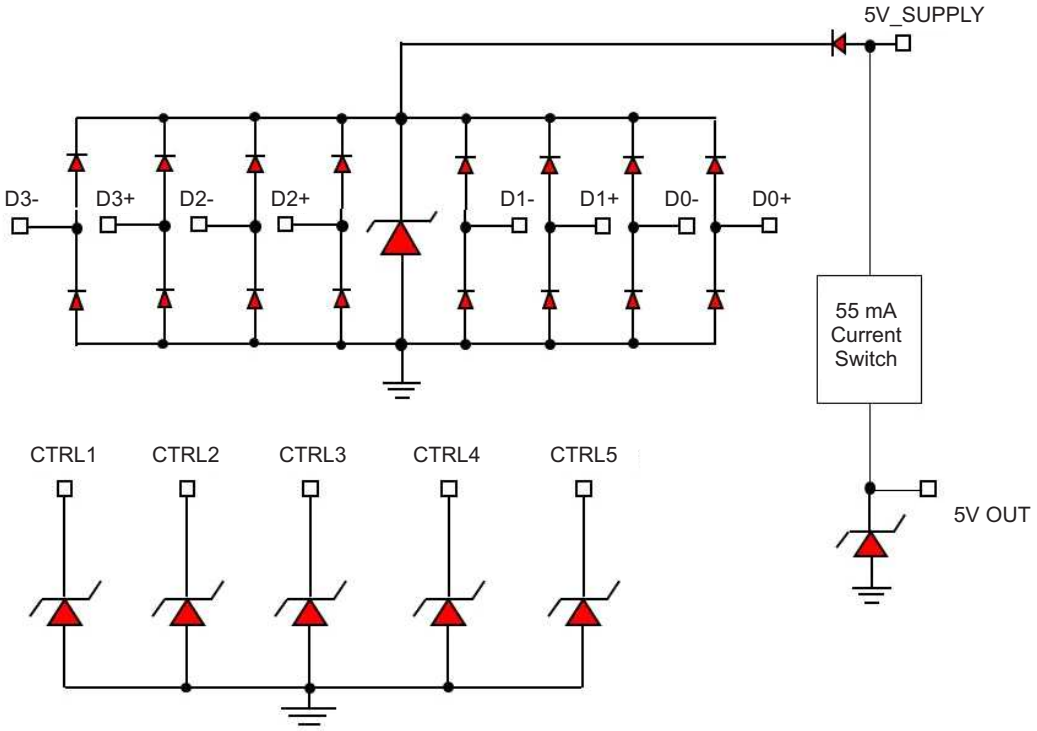


Figure 10. Electrical Equivalent Circuit Diagrams

7.3 Feature Description

7.3.1 IEC 61000-4-2 Protection

The connector-facing I/O pins can withstand ESD events up to ±12-kV contact and ±14-kV air. An ESD clamp diverts the current to ground.

7.3.2 Single-Chip ESD Solution

The TPD13S523 provides a complete ESD protection scheme for an HDMI 1.4 compliant port. No additional components are required for ESD protection and current-limiting besides this device.

Feature Description (continued)

7.3.3 On-Chip 5-V Load Switch

The TPD13S523 provides an on-chip regulator with a current output rating of 55-mA. This regulator also prevents reverse current flow from occurring, in compliance with the HDMI 5-V supply specification.

7.3.4 Supports UTILITY Line Protection

This device provides protection for all control lines in HDMI, including the UTILITY pin.

7.3.5 < 0.05-pF Differential Capacitance Between TMDS Pairs

The TPD13S523 has a very low capacitance variation (< 0.05 pF) between different TMDS ESD clamps. This provides excellent matching and does not degrade differential signal quality.

7.3.6 Industry Standard Package and Space-Saving Package

The TPD13S523 is offered in 2 different packages. A 16-pin industry standard TSSOP package is provided for ease of routing and easy layout. A 16-pin UQFN (RSV) is provided where small size is needed in the application.

7.3.7 Supports Data Rates in Excess of 3.4 Gbps

The TMDS ESD clamps have a very low capacitance that is capable of supporting HDMI data rates exceeding 3.4 Gbps.

7.3.8 R_{DYN} = 0.5 Ω

The TMDS ESD clamps have a very low R_{DYN} of 0.5Ω (typ) which provides excellent ESD protection clamping characteristics for the upstream core transmitter.

7.3.9 Commercial Temperature Range

The TPD13S523 is rated to operate from -40°C to 85°C.

7.4 Device Functional Modes

TPD13S523 is active with the conditions in the *Recommended Operating Conditions* met. Each connector side pin has an ESD clamp that triggers when voltages are greater than V_{BR} or less than the lower diode's V_f. During ESD events, voltages as high as ±12-kV contact ESD can be directed to ground through the internal diode network. Once the voltages on the protected line fall below these trigger levels (usually within 10's of nano-seconds), these pins revert to a nonconductive state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD13S523 provides IEC 61000-4-2 Level 4 Contact ESD protection for an HDMI 1.4 transmitter port. An integrated current limit switch ensures compliance with the HDMI 5-V power supply requirements. This section presents a simplified discussion of the design process for this protection device.

8.2 Typical Application

A typical application schematic for an HDMI 1.4 transmitter port protected by the TPD13S523 is shown in Figure 11. The eight TMDS lines and five control lines are connected to their respective pins for ESD protection. The 5-V power path is connected through the 55-mA current limit switch.

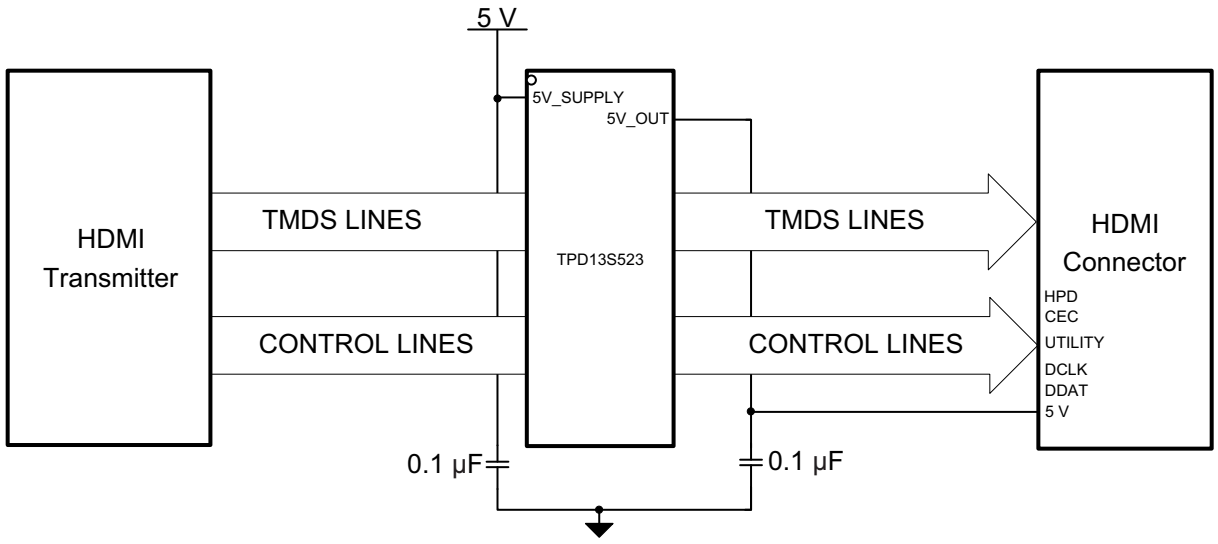


Figure 11. TPD13S523 Configured With an HDMI 1.4 Transmitter Port

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as input parameters.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Voltage on 5V_SUPPLY	4.8 V - 5.3 V
HDMI Data Rate	3.4 Gbps

8.2.2 Detailed Design Procedure

To begin the design process, the designer must know the following parameters:

- 5V_SUPPLY voltage range
- Maximum HDMI data rate

8.2.2.1 5V_SUPPLY Voltage Range

The TPD13S523 is capable of operating the 5V_SUPPLY up to 5.5 V, with recommended voltage from 4.5 V to 5.5 V. In this example, the supply range is 4.8 V to 5.3 V, which satisfies this requirement.

8.2.2.2 Maximum HDMI Data Rate

The TPD13S523 is capable of operating at HDMI data rates in excess of 3.4 Gbps, compliant to the HDMI 1.4 maximum data rate. In this example, the maximum HDMI 1.4 data rate of 3.4 Gbps has been chosen.

8.2.3 Application Curves

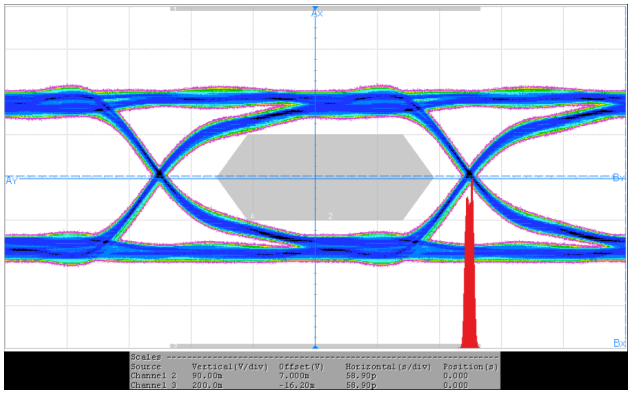


Figure 12. Eye Diagram Using EVM Without TPD13S523 for the TMDS Lines at 1080p, 340-MHz Pixel Clock, 3.4 Gbps

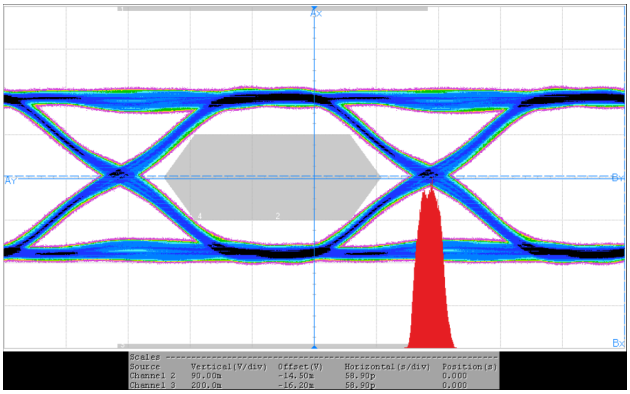


Figure 13. Eye Diagram Using EVM With TPD13S523 for the TMDS Lines at 1080p, 340-MHz Pixel Clock, 3.4 Gbps

9 Power Supply Recommendations

The designer must consider the requirement for the 5V_OUT voltage level. To ensure the voltage is within tolerance under load, set 5V_SUPPLY to at least 4.8 V + V_{DROP} (205 mV). Otherwise, TPD13S523 is a passive ESD protection device and there is no need to power it.

10 Layout

10.1 Layout Guidelines

The TPD13S523 device offers little or no signal distortion during normal operation due to low I/O capacitance and ultra-low leakage current specifications. In the event of an ESD stress, this device ensures that the core circuitry is protected and the system is functioning properly. For proper operation, the following layout and design guidelines should be followed:

1. Place the TPD13S523 as close to the connector as possible. This allows the TPD13S523 to remove the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place two 0.1-µF capacitors very close to the 5V_SUPPLY and 5V_OUT pins. These capacitors will help limit the noise at the 5V_OUT power line, and also help with system level ESD protection.
3. Ensure that there is enough metallization for the GND pad. During normal operation, the TPD13S523 ESD pins consume ultra-low leakage current. During the ESD event, GND pin will see multiple amps of current. A sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. The critical routing paths for HDMI interface are the high-speed TMDS lines. With the PW package, all the TMDS lines (pin Dxx) can be routed in a single signal plane and still maintain the differential coupling and trace symmetry. This helps reduce the overall board manufacturing cost. The slow speed control lines can be routed in another signal layer through vias.
5. If the UTILITY or any other pin is not utilizied, tie the pin to a ground rather than leave floating. Use a 75-Ω resistor to protect against shorts to ground.

10.2 Layout Examples

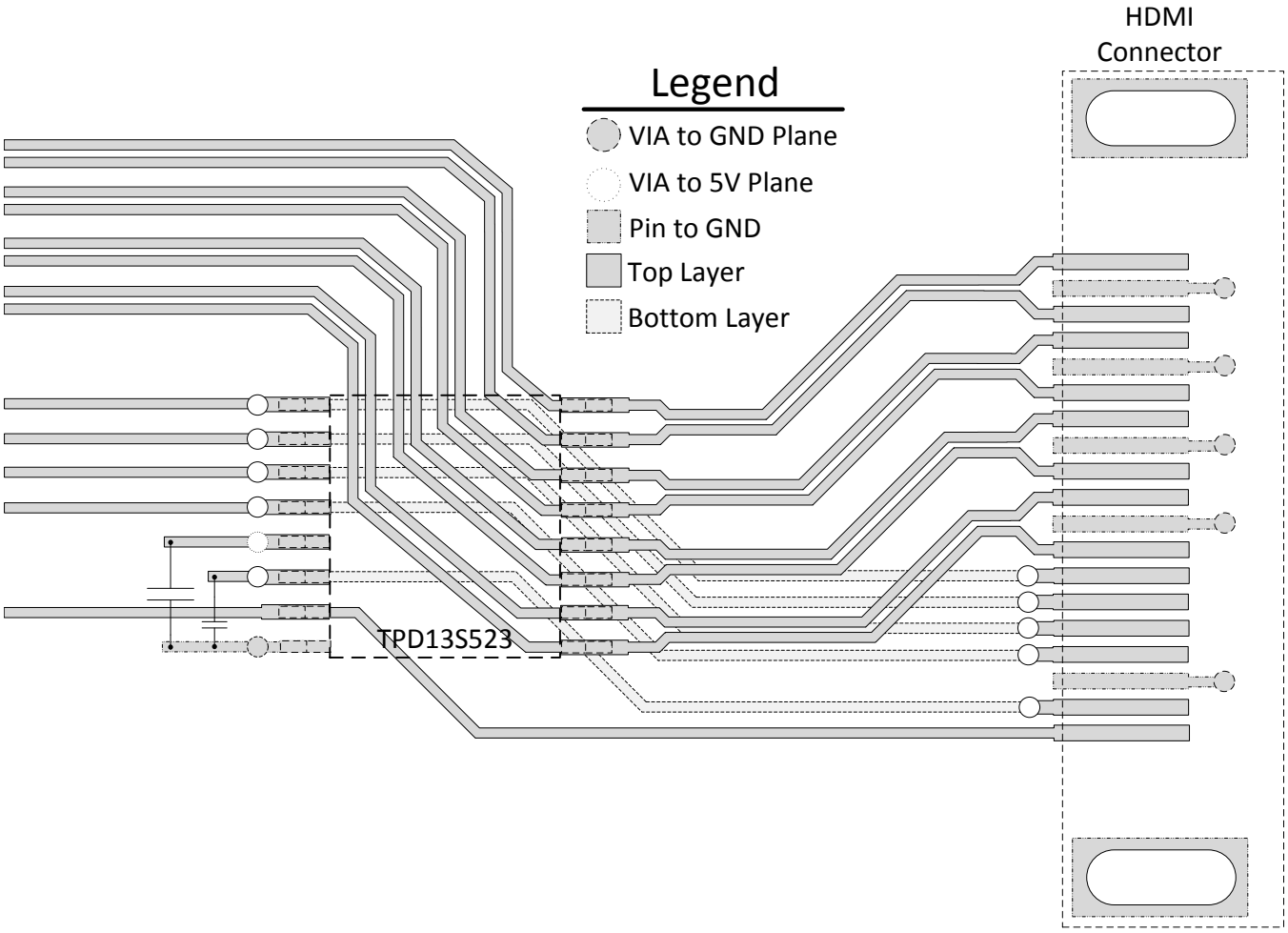


Figure 14. TPD13S523PWR Layout Example 13-Line HDMI Protection

Layout Examples (continued)

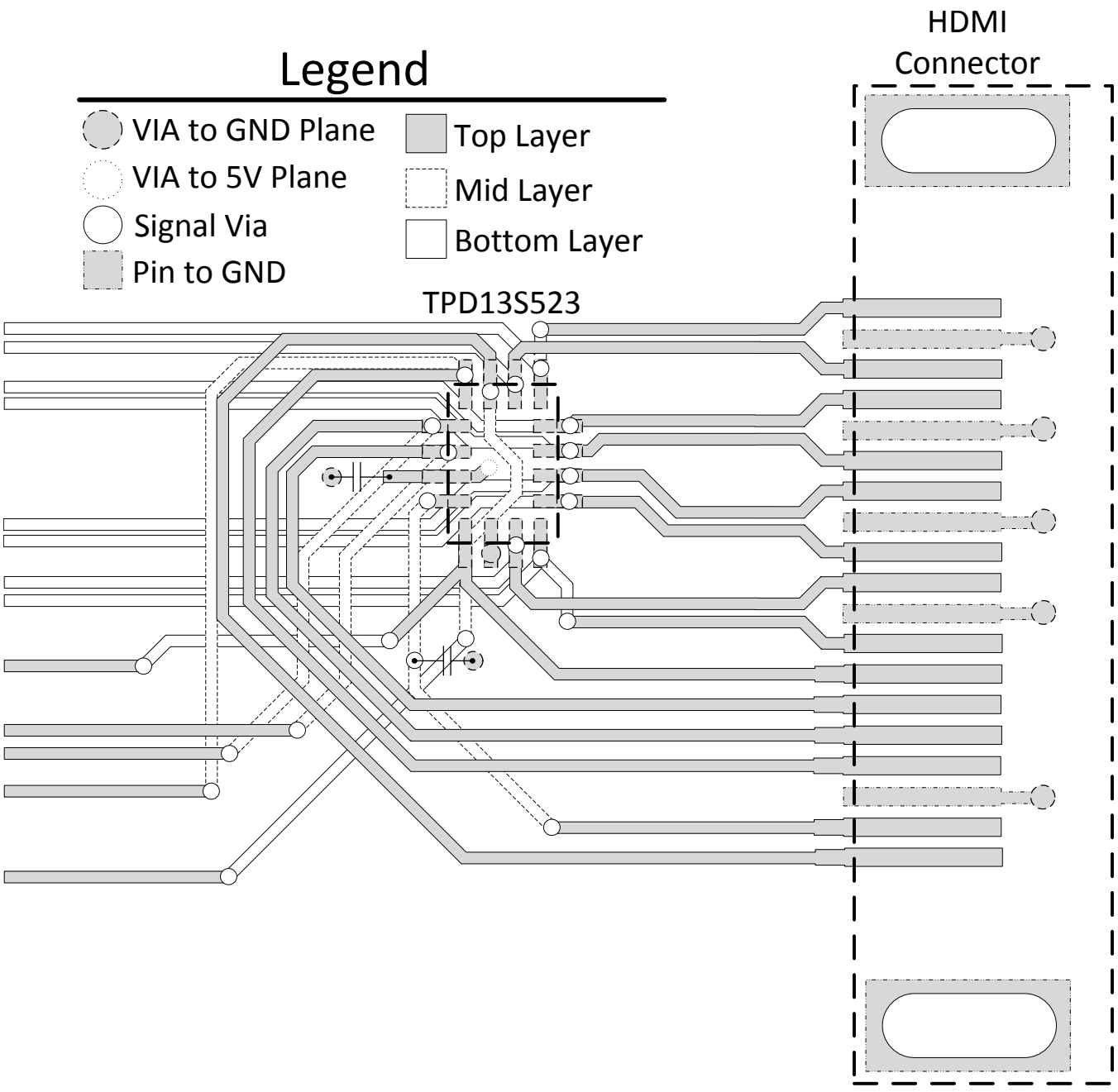


Figure 15. TPD13S523RSVR Layout Example 13-Line HDMI Protection

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

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All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD13S523PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RA523	Samples
TPD13S523RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

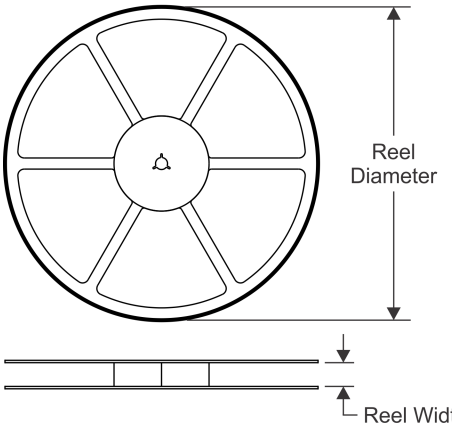
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

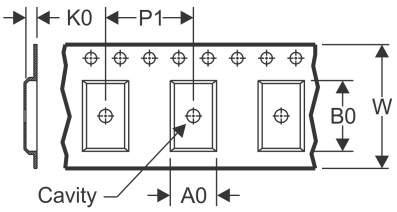
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

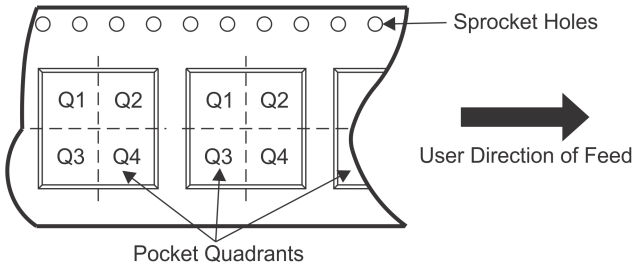


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

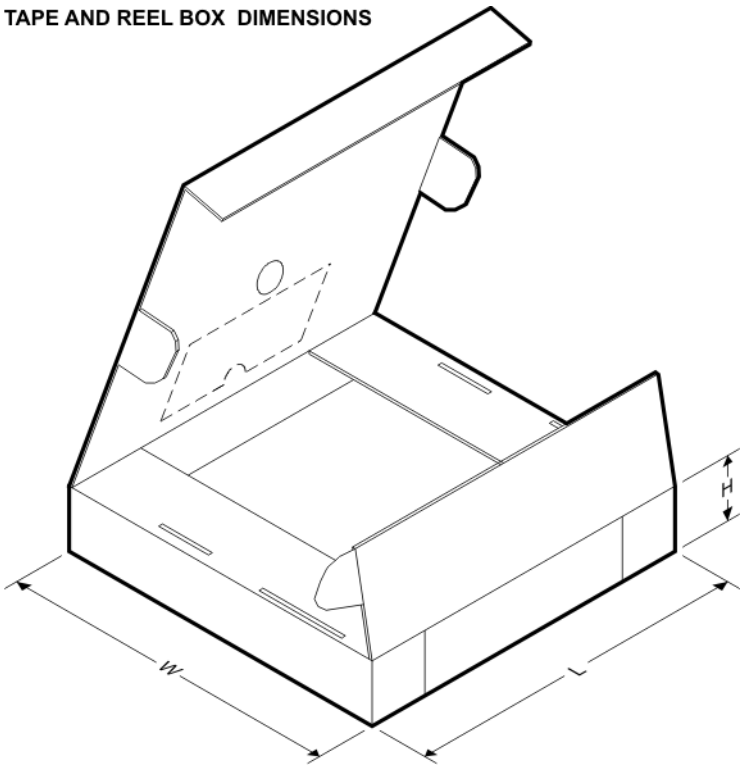
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD13S523PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPD13S523RSVR	UQFN	RSV	16	3000	330.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1
TPD13S523RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1

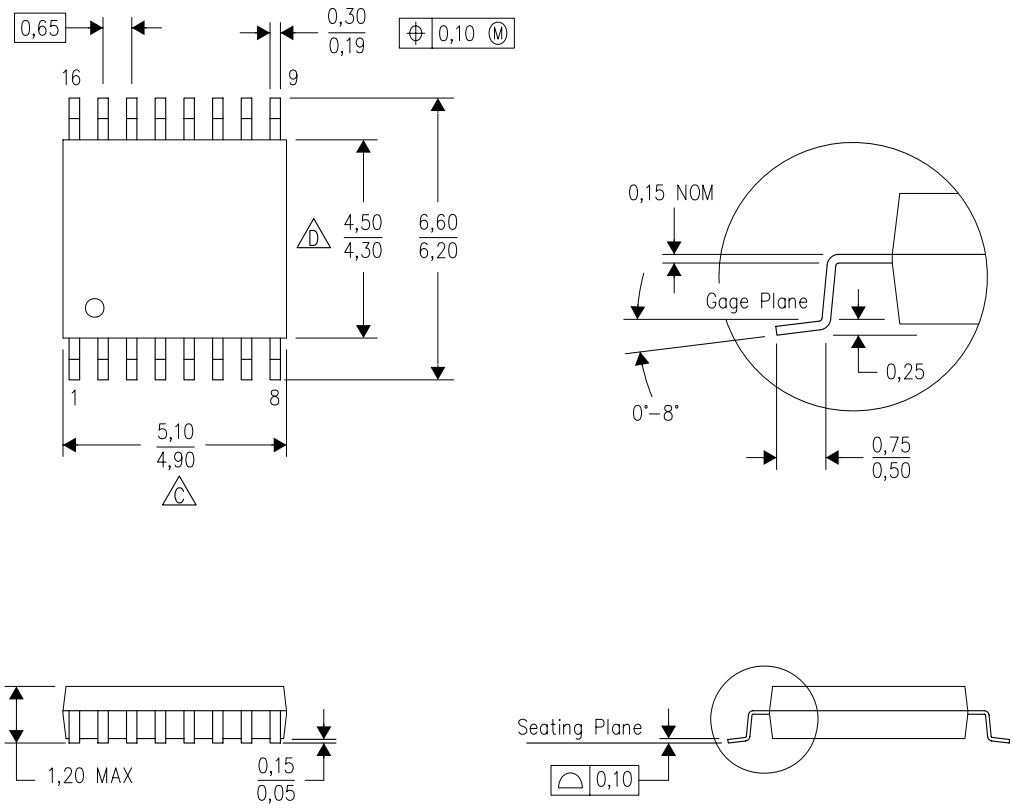
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD13S523PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TPD13S523RSVR	UQFN	RSV	16	3000	184.0	184.0	19.0
TPD13S523RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



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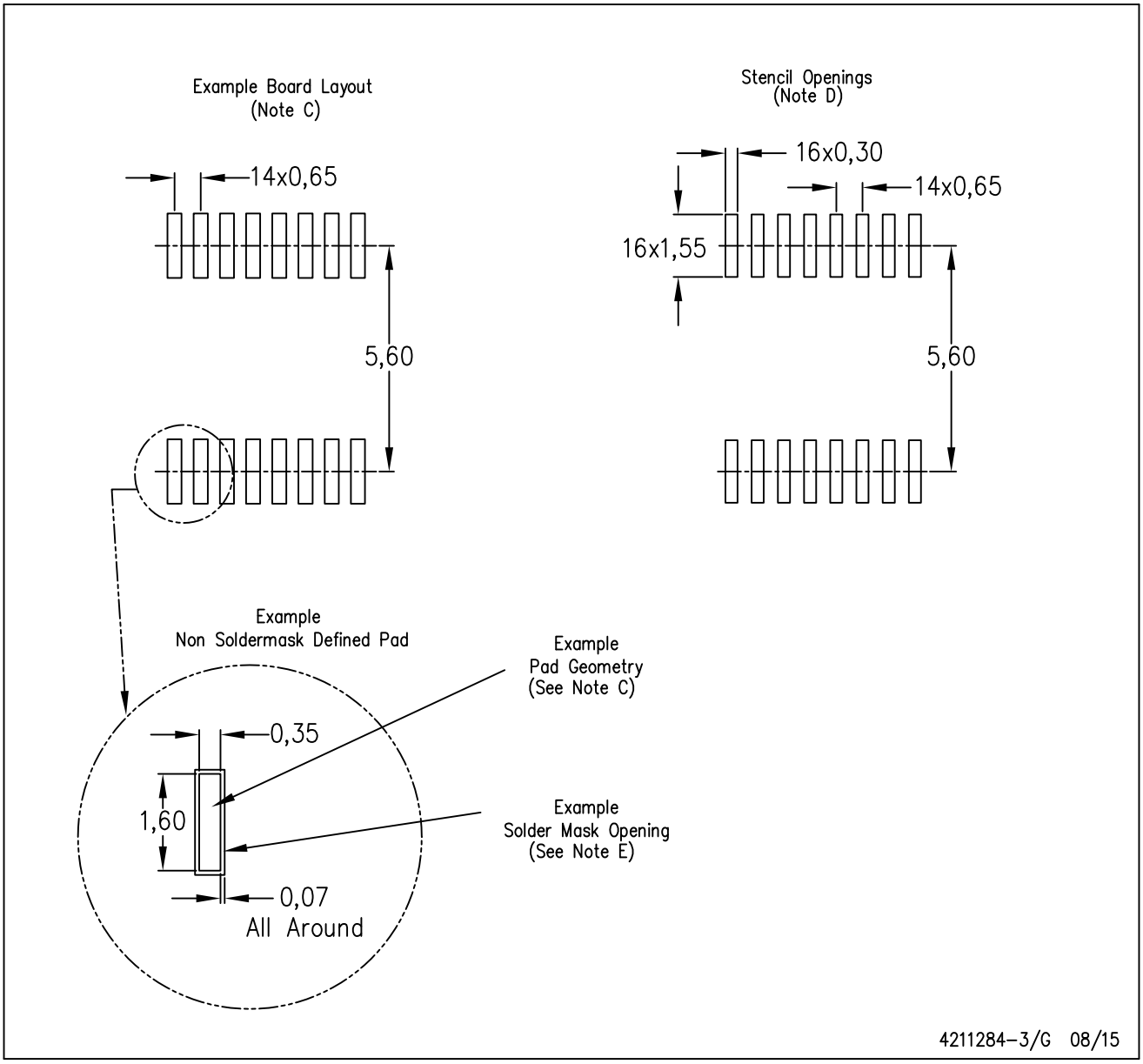
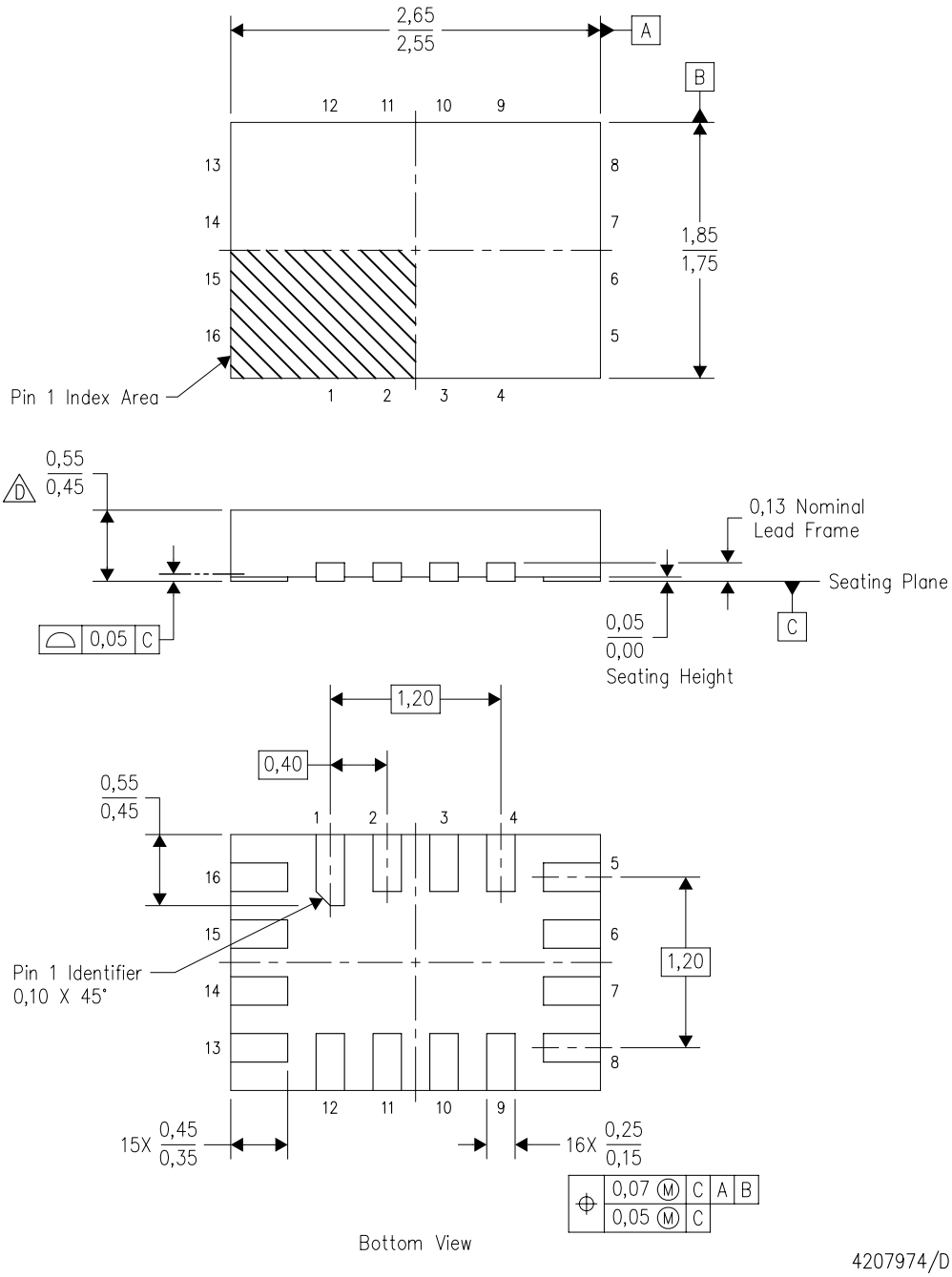
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



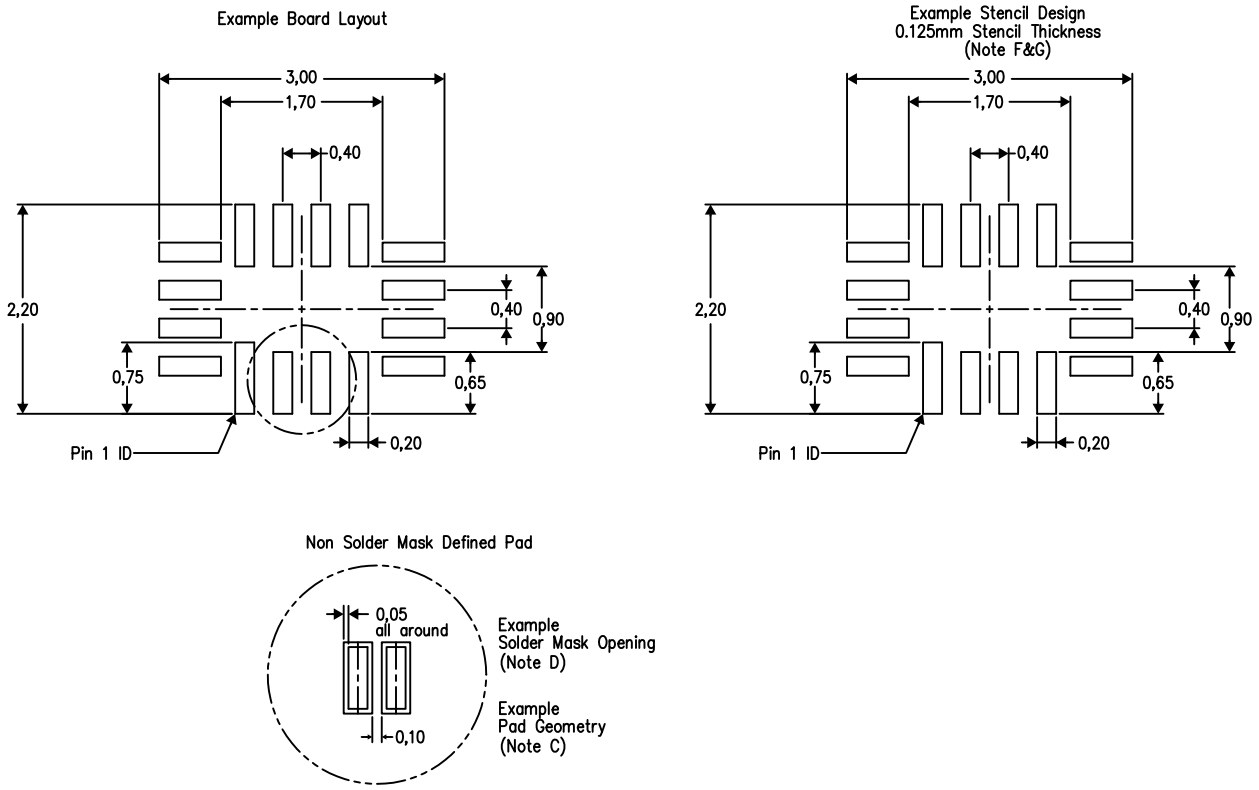
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UFHE, except minimum package thickness.

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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