TPD1S414 USB Charger Overvoltage, Surge, and ESD Protection for V_{BUS} Pin

1 Features

- Overvoltage Protection at V_{BUS_CON} Up to 30-V DC
- Low R_{ON} nFET Switch Supports Host and Charging Mode
- Internal 15-ms Start-Up Delay
- Internal 30-ms Soft-Start Delay to Minimize the USB Inrush Current
- Transient Protection for V_{BUS} Line:
  - IEC 61000-4-2 Contact Discharge ±15 kV
  - IEC 61000-4-2 Air Gap Discharge ±15 kV
  - IEC 61000-4-5 Open-Circuit Voltage 100 V
- Integrated Input Enable and Status Output Signal
- Thermal Shutdown (TSD) Feature
- Space-Saving DSBGA Package: (1.4 mm × 1.89 mm)

2 Applications

- End Equipment
  - Mobile Phones
  - Tablets
  - Wearables
  - Electronic-Point-of-Sale (EPOS)
- Interfaces
  - USB 2.0
  - USB 3.0
  - USB Type C

3 Description

The TPD1S414 device is a single-chip solution for a USB connector's V_{BUS} line protection. The bidirectional nFET switch ensures safe current flow in both charging and host mode while protecting the internal system circuits from any overvoltage conditions at the V_{BUS_CON} pin. On the V_{BUS_CON} pin, this device can handle overvoltage protection up to 30 V. After the $\overline{EN}$ pin toggles low, the TPD1S414 waits 20 ms before turning ON the nFET through a soft-start delay. $\overline{ACK}$ pin indicates the FET is completely turned ON.

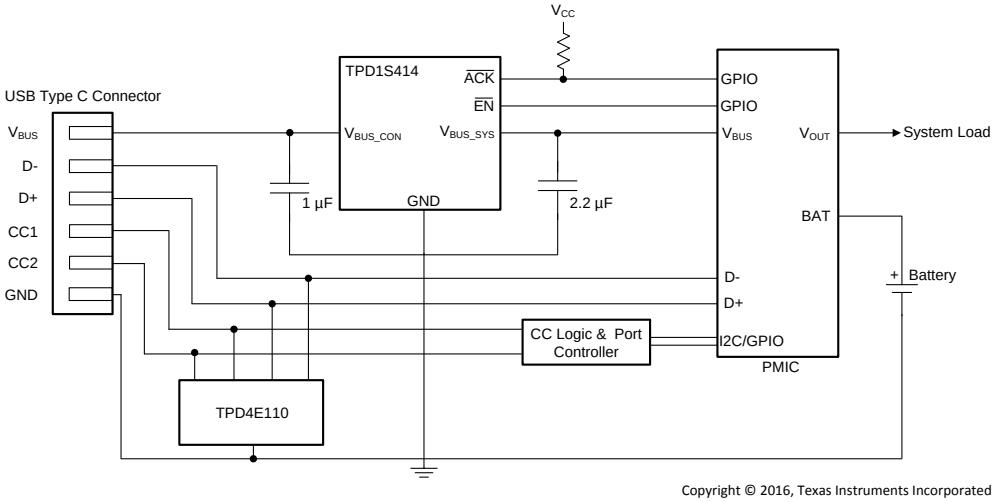
The typical application interface for the TPD1S414 is the V_{BUS} line in USB connectors. Typical end equipment for TPD1S414 are mobiles phones, tablets, wearables, and electronic-point-of-sale (EPOS). The TPD1S414 can also be applied to any system using an interface with a 5-V power rail.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD1S414	DSBGA (12)	1.40 mm × 1.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2013) to Revision B — **Page**

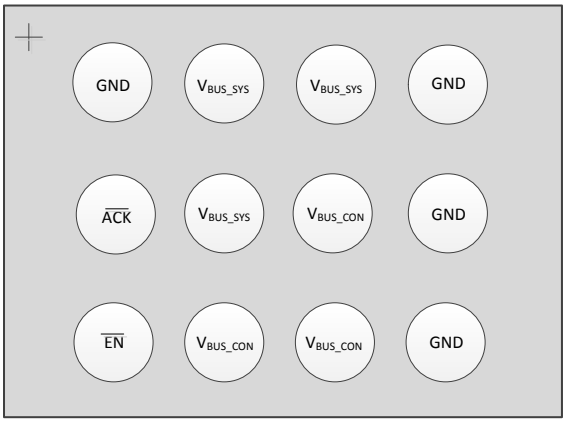
- Added *ESD Ratings* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (October 2013) to Revision A — **Page**

- Changed text in the DESCRIPTION From: TPD1S414 waits 15 ms before turning ON the nFET To: TPD1S414 waits 20 ms before turning ON the nFET ... 1
- Deleted Continuous forward current through the FET body diode, I_{DIODE} from the ABSOLUTE MAXIMUM RATINGS table ... 4
- Deleted Peak input current on V_{BUS_CON} pin, I_{BUS} from the ABSOLUTE MAXIMUM RATINGS table ... 4
- Added Voltage on $\overline{ACK}$ pin to the ABSOLUTE MAXIMUM RATINGS table ... 4
- Added Continuous current on V_{BUS_CON} and V_{BUS_SYS} pins to the RECOMMENDED OPERATING CONDITIONS table ... 4
- Added Continuous forward current through the FET body diode, I_{DIODE} to the RECOMMENDED OPERATING CONDITIONS table ... 4
- Added values to the THERMAL INFORMATION table ... 5
- Changed the I_{HOST_LEAK} MAX value From: 160 To: 200 µA in the SUPPLY CURRENT CONSUMPTION table ... 6
- Deleted graphs: Enabling the Load Switch, Connecting V_{BUS_CON}, and OVP Operation from the TIMING DIAGRAMS section ... 7
- Changed horizontal axis labeling on Figure 7 ... 8
- Changed Figure 10 ... 14
- Added text to the APPLICATION INFORMATION section ... 14

5 Pin Configuration and Functions

YZ Package
12-Pin DSBGA
Top View - See Through



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
$\overline{ACK}$	B1	O	Open-Drain Acknowledge pin. See *Table 2*.
$\overline{EN}$	C1	I	Enable Active-Low Input. Drive $\overline{EN}$ low to enable the switch. Drive $\overline{EN}$ high to disable the switch.
V_{BUS_CON}	B3, C2, C3	I/O	Connect to USB connector V_{BUS} pin; IEC61000-4-2 ESD protection IEC61000-4-5 Surge protection
V_{BUS_SYS}	A2, A3, B2	I/O	Connect to internal V_{BUS} plane
GND	A1, A4, B4, C4	Ground	Connect to PCB ground plane

Table 1. 12-YZ Pin Mapping

	1	2	3	4
A	GND	V_{BUS_SYS}	V_{BUS_SYS}	GND
B	$\overline{ACK}$	V_{BUS_SYS}	V_{BUS_CON}	GND
C	$\overline{EN}$	V_{BUS_CON}	V_{BUS_CON}	GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage from USB connector, V_{BUS_CON}		–0.3	30	V
Internal supply DC voltage rail on the PCB, V_{BUS_SYS}		–0.5	7	V
Voltage on $\overline{EN}$ pin		–0.5	7	V
Voltage on $\overline{ACK}$ pin		–0.5	7	V
Output load capacitance, C_{LOAD}	V_{BUS_SYS} pin	0.1	50	µF
Input capacitance, C_{ON}	V_{BUS_CON} pin	0.1	50	µF
Operating free-air temperature, T_A		–40	85	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	
		IEC 61000-4-2 contact discharge		±15000	V
		IEC 61000-4-2 air-gap discharge		±15000	V
		IEC 61000-4-5 Peak Pulse Current (t_p = 8/20 µs)	V_{BUS_CON} pin	21	A
		IEC 61000-4-5 Peak Pulse Power (t_p = 8/20 µs)	V_{BUS_CON} pin	700	W
		IEC 61000-4-5 Open circuit voltage (t_p = 1.2/50 µs)	V_{BUS_CON} pin	100	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_{BUS_CON}	Supply voltage from USB connector				5.9	V
V_{BUS_SYS}	Internal supply DC voltage rail on the PCB				5.9	V
C_{LOAD}	Output load capacitance	V_{BUS_SYS} pin		2.2		µF
C_{IN}	Input capacitance	V_{BUS_CON} pin		1		µF
R_{PULLUP}	Pullup resistor	$\overline{ACK}$ pin		4.3	100	kΩ
I_{VBUS}	Continuous current on V_{BUS_CON} and V_{BUS_SYS} pins	V_{BUS_CON} V_{BUS_SYS}			3.5	A
I_{DIODE}	Continuous current through the FET body diode				1	A

6.4 Thermal Information

THERMAL METRIC(1)		TPD1S414 YZ (DSBGA) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	89	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	n/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics ($\overline{EN}$, $\overline{ACK}$ Pins)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage, $\overline{EN}$		1.2		6	V
V_{IL}	Low-level input voltage, $\overline{EN}$				0.8	V
I_{IL}	Input leakage current $\overline{EN}$	V_I = 3.3 V			1	µA
V_{OL}	Low-level output voltage, $\overline{ACK}$	I_{OL} = 3 mA			0.4	V

6.6 Electrical Characteristics (OVP Circuit)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP_RISING}	Input overvoltage protection threshold, V_{BUS_CON}	V_{BUS_CON} increasing from 5 V	6	6.2	6.4	V
V_{HYS_OVP}	Hysteresis on OVP, V_{BUS_CON}	V_{BUS_CON} decreasing from 7 V to 5 V		50		mV
$V_{OVP\_FALLING}$	Input overvoltage protection threshold, V_{BUS_CON}	V_{BUS_CON} decreasing from 7 V to 5 V	5.93		6.37	V
V_{UVLO}	Input undervoltage lockout, V_{BUS_CON}	V_{BUS_CON} voltage rising from 0 V to 5 V	3.1	3.3	3.5	V
V_{HYS_UVLO}	Hysteresis on UVLO, V_{BUS_CON}	Difference between rising and falling UVLO thresholds		100		mV
$V_{UVLO\_FALLING}$	Input undervoltage lockout, V_{BUS_CON}	V_{BUS_CON} voltage rising from 5 V to 0 V	3	3.2	3.4	V
V_{UVLO_SYS}	V_{BUS_SYS} undervoltage lockout, V_{BUS_SYS}	V_{BUS_SYS} voltage rising from 0 V to 5 V	3.1	3.6	4.3	V
$V_{HYS\_UVLO\_SYS}$	V_{BUS_SYS} UVLO Hysteresis, V_{BUS_SYS}	Difference between rising and falling UVLO thresholds on V_{BUS_SYS}		480		mV
$V_{UVLO\_SYS\_FALL}$	V_{BUS_SYS} undervoltage lockout, V_{BUS_SYS}	V_{BUS_SYS} voltage falling from 7 V to 5 V	3	3.2	3.4	V

6.7 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{DELAY}	USB charging turnon delay	Measured from $\overline{EN}$ asserted LOW to nFET beginning to Turn ON(1) excluding soft-start time		20		ms
t_{SS}	USB charging rise time (soft-start delay)	Measure from V_{BUS_SYS} rises above 25% (with 1-MΩ load/ NO C_{LOAD}) until $\overline{ACK}$ goes Low (10%)		25		ms
t_{OFF_DELAY}	USB charging turnoff time	Measured from $\overline{EN}$ asserted High to V_{BUS_SYS} falling to 10% with R_{LOAD} = 10 Ω and No C_{LOAD} on V_{BUS_SYS}		4		µs
OVERVOLTAGE PROTECTION						
$t_{OVP\_response}$	OVP response time	Measured from OVP Condition to FET Turn OFF(2). V_{BUS_CON} rises at 1V / 100 ns			100	ns
t_{OVP_Recov}	Recovery time	Measured from OVP Clear to FET Turn ON(3)		20		ms

(1) Shown in Figure 1.
(2) Parameters provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.
(3) Excludes soft-start time

6.8 Switching Characteristics (nFET)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(on)}$	Switch ON-resistance	V_{BUS_CON} = 5 V, I_{OUT} = 1 A, T_A = 25°C		39	50	mΩ

6.9 Supply Current Consumption

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBUS_SLEEP}	V_{BUS_CON} operating current consumption	Measured at V_{BUS_CON} pin, V_{BUS_CON} = 5 V, $\overline{EN}$ =5V		30	70	µA
I_{VBUS}		Measured at V_{BUS_CON} pin, V_{BUS_CON} = 5 V, $\overline{EN}$ 0 V and no load		175	373	µA
I_{VBUS_SYS}	V_{BUS_CON} operating current consumption	Measured at V_{BUS_SYS} pin, V_{BUS_SYS} = 5 V, $\overline{EN}$ = 0 V and V_{BUS_CON} = Hi Z		175	373	µA
I_{HOST_LEAK}	Host mode leakage current	Measured at V_{BUS_SYS}, V_{BUS_CON} = Hi Z, $\overline{EN}$ = 5 V, V_{BUS_SYS} = 5 V	90		200	µA

6.10 Thermal Shutdown Feature

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SHDN}	Thermal shutdown	Junction temperature		145		°C
	Thermal-shutdown hysteresis	Junction temperature		35		°C

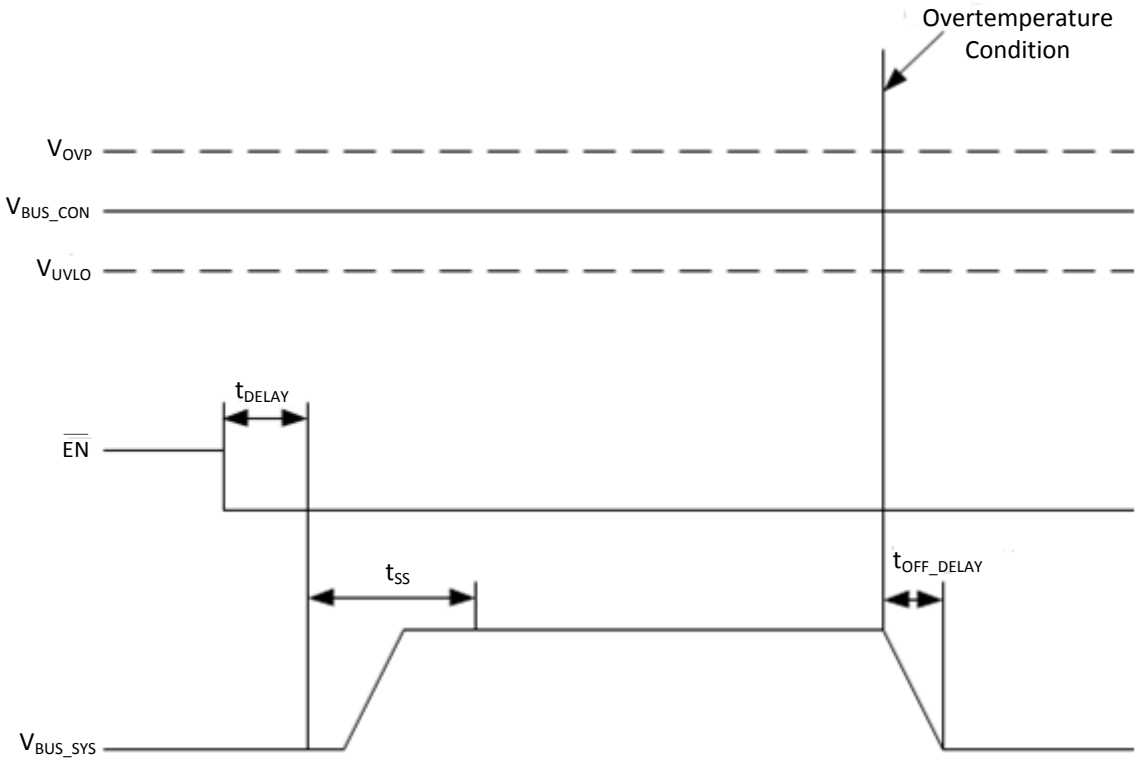


Figure 1. Thermal Shutdown Operation

6.11 Typical Characteristics

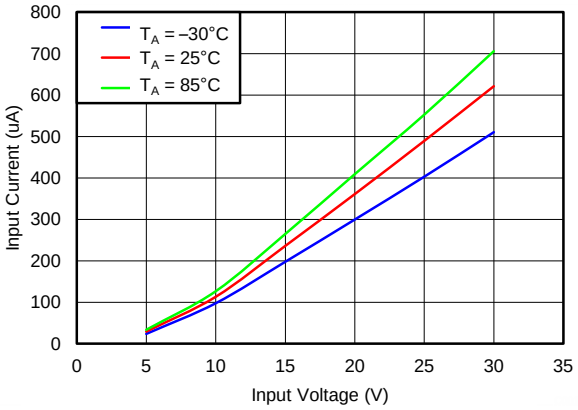


Figure 2. Input Supply Current vs Supply Voltage

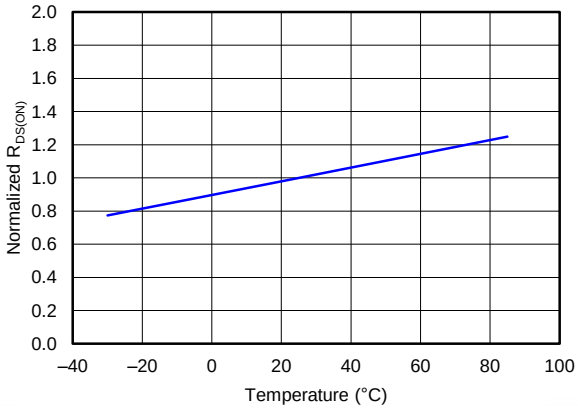


Figure 3. Normalized $R_{DS(ON)}$ vs Temperature

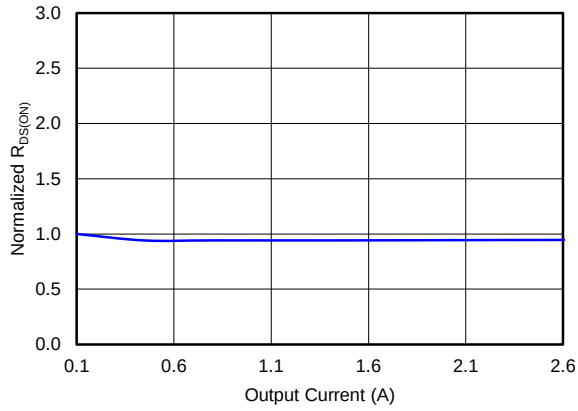


Figure 4. Normalized $R_{DS(ON)}$ vs Output Current

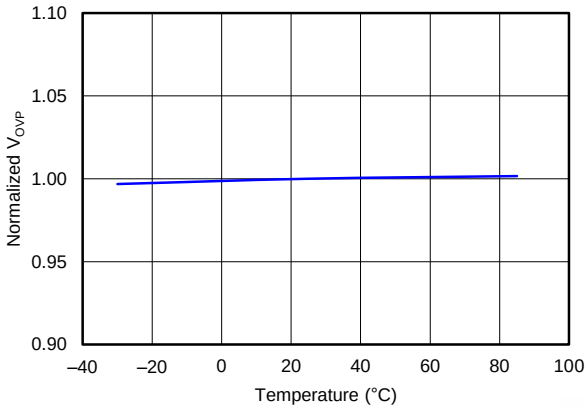


Figure 5. Normalized V_{OVP}

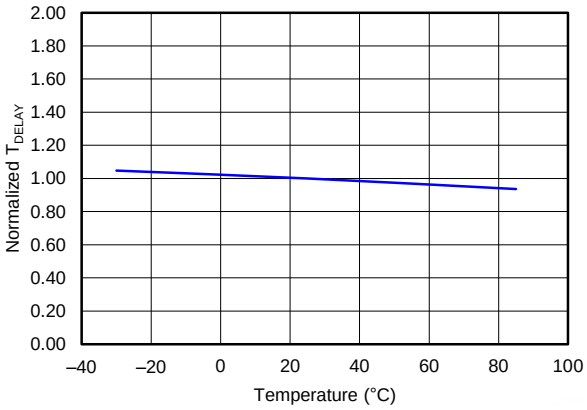


Figure 6. Normalized T_{DELAY}

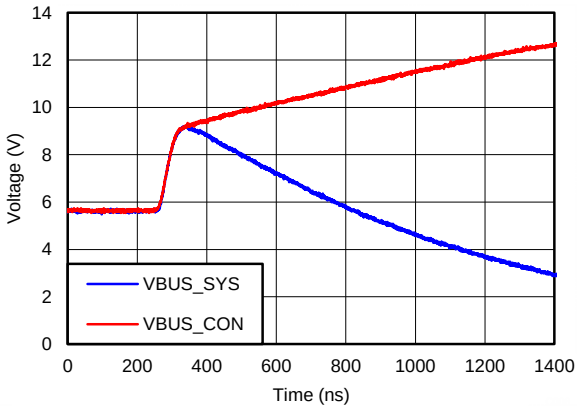


Figure 7. V_{OVP} Response Time

Typical Characteristics (continued)

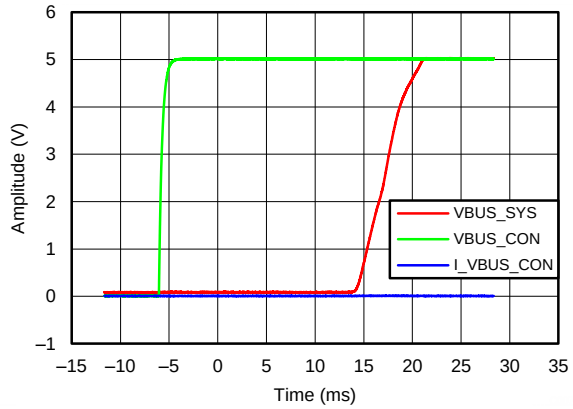


Figure 8. Power Up With 2.2 µF on V_{BUS_SYS}

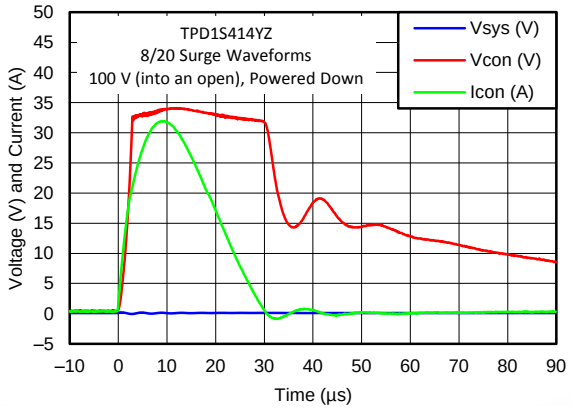


Figure 9. Response to a 100-V Surge

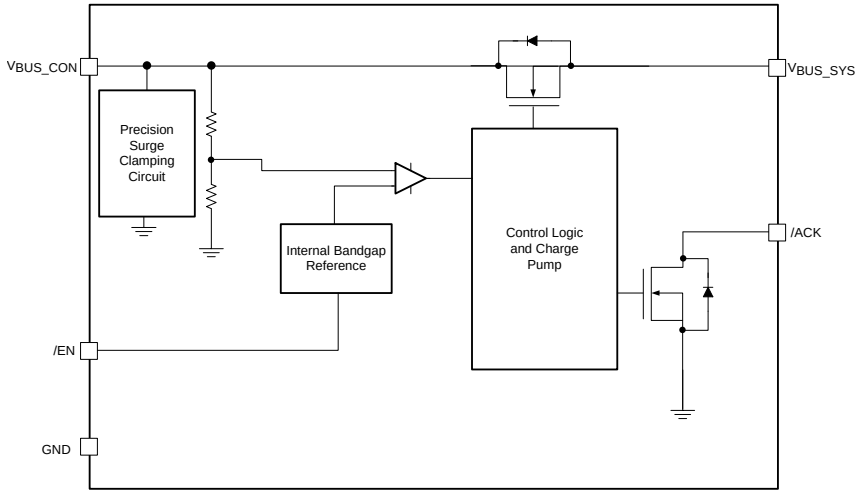
7 Detailed Description

7.1 Overview

The TPD1S414 provides a single-chip ESD protection, surge protection, and overvoltage protection solution for portable USB charging and Host interfaces. It offers overvoltage protection at the V_{BUS_CON} pin up to 30 V. The TPD1S414 also provides a $\overline{ACK}$ pin that indicates to the system if a fault condition has occurred. The TPD1S414 offers an ESD clamp and a surge clamp for V_{BUS_CON} pin, thus eliminating the need for external TVS clamp circuits in the application.

The TPD1S414 has an internal oscillator and charge pump that controls the turnon of the internal nFET switch. The internal oscillator controls the timers that enable the charge pump and resets the open-drain $\overline{ACK}$ output. If V_{BUS_CON} is less than V_{OVP}, the internal charge pump is enabled. After a 15-ms internal delay, the charge-pump starts up, and turns on the internal nFET switch through a soft start. Once the nFET is completely turned ON, TPD1S414 asserts $\overline{ACK}$ pin LOW. At any time, if V_{BUS_CON} rises above V_{OVP}, the $\overline{ACK}$ pin is in High-Z and is pulled HIGH through external resistors. The nFET switch is turned OFF.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Overvoltage Protection on V_{BUS_CON} up to 30-V DC

When the V_{BUS_CON} voltage rises above V_{OVP}, the internal nFET switch is turned off, removing power from the system side. V_{BUS_CON} can tolerate up to 30-V DC. The response to overvoltage is very rapid, with the nFET switch turning off in less than 100 ns. When the V_{BUS_CON} voltage returns back to below $V_{OVP} - V_{HYS\_OVP}$, the nFET switch is turned on again after an internal delay of t_{OVP_RECOV} (t_{DELAY}). This time delay ensures that the V_{BUS_CON} supply has stabilized before turning the switch back on. After t_{OVP_RECOV}, the TPD1S414 turns on the nFET through a soft start. Once the OVP condition is cleared the nFET is turned completely on.

7.3.2 Low R_{ON} nFET Switch Supports Host and Charging Mode

The nFET switch has a total ON-resistance (R_{ON}) of 39 mΩ. This equates to a voltage drop of less than 140 mV when charging at the maximum 3.5-A current level. Such low R_{ON} helps provide maximum potential to the system as provided by an external charger or by the system when in host mode.

7.3.3 ±15-kV IEC 61000-4-2 Level 4 ESD Protection

The V_{BUS_CON} pin can withstand ESD events up to ±15-kV Contact and Air-Gap. An ESD clamp diverts the current to ground.

Feature Description (continued)

7.3.4 100-V IEC 61000-4-5 µs Surge Protection

The V_{BUS_CON} pin can withstand surge events up to 100-V open-circuit voltage (V_{PP}), and 700 W. A precision clamp diverts the current to ground and active circuitry switches OFF the nFET earlier than 100 ns before an overvoltage can get through to V_{BUS_SYS}.

7.3.5 Start-Up and OVP Recovery Delay

The TPD1S414 has a built-in start-up delay. Once the device has been enabled, a time t_{DELAY} elapses before the charge pump is enabled which turns on the nFET. A manufactured preprogrammed soft start, t_{SS}, is used when turning on the nFET with the charge pump. Once the device is enabled, these start delays, t_{DELAY} + t_{SS}, work together to meet the USB inrush current compliance. Similarly, after an OVP event has occurred, the device waits a time t_{OVP_RECOV} before enabling the charge pump to turn on the nFET. The soft-start, t_{SS}, is still used when turning on the nFET with the charge pump after an OVP event, making the total time for the nFET switch to turn on after the OVP event t_{OVP_RECOV} + t_{SS}.

7.3.6 Integrated Input Enable and Status Output Signal

The TPD1S414 integrates an enable signal to control the ON and OFF state of its nFET. The device also integrates an status output signal through the $\overline{ACK}$ pin which indicates whether or not a fault is occurring on the device. See the Table 2 table to understand the functionality of these pins in all of the TPD1S414's states.

7.3.7 Thermal Shutdown

The TPD1S414 family has an overtemperature protection circuit to protect against system faults or improper use. The basic function of the thermal shutdown (TSD) circuit is to sense when the junction temperature has exceeded the absolute maximum rating and shuts down the device until the junction temperature has cooled to a safe level. When in the thermal shutdown condition, the device asserts a fault by setting the $\overline{ACK}$ pin to High-Z.

7.4 Device Functional Modes

7.4.1 $V_{BUS\_CON} < V_{UVLO}$

When V_{BUS_CON} is less than V_{UVLO}, the device is in its unpowered state. The nFET is OFF and the $\overline{ACK}$ pin is High-Z. In this state, TPD1S414 still provides IEC 61000-4-2 ±15-kV Contact/±15-kV air-gap protection and IEC 61000-4-5 100-V open-circuit surge protection.

7.4.2 $V_{UVLO} < V_{BUS\_CON} < V_{OVP}$

When V_{BUS_CON} is greater than V_{UVLO} and less than V_{OVP}, the device is in its powered state. In this state, the nFET can be controlled ON and OFF through the enable pin. When the $\overline{EN}$ pin is Low, the nFET is ON and can be used for both charging and host or OTG mode. While the nFET switch is ON, the $\overline{ACK}$ pin is held Low. When the enable pin is high, the nFET switch is held OFF and the $\overline{ACK}$ pin is High-Z. In both the enable and disabled states, the TPD1S414 provides IEC 61000-4-2 ±15-kV contact/±15-kV air-gap protection and IEC 61000-4-5 100-V open-circuit surge protection.

7.4.3 $V_{BUS\_CON} > V_{OVP}$

When V_{BUS_CON} is greater than V_{OVP}, the device is in the overvoltage protection sate. In this state, the nFET switch is forced OFF regardless of the state of the enable pin and $\overline{ACK}$ is set High-Z. V_{BUS_CON} can handle overvoltage protection up to 30 V.

7.4.4 OVP Operation

When the V_{BUS_CON} voltage rises above V_{OVP}, the internal nFET switch is turned off, removing power from the system. The response is rapid, with the FET switch turning off in less than 100 ns. The $\overline{ACK}$ pin is set to High-Z when an overvoltage condition is detected and the nFET is turned OFF. This pin can be pulled up through external resistors to indicate an OVP condition. When the V_{BUS_CON} voltage returns below V_{OVP} – $V_{HYS-OVP}$, the nFET switch is turned on again after the internal delay of t_{OVP_Recov}. This delay time ensures that the V_{BUS_CON} supply has stabilized before turning the switch back on. After t_{OVP_Recov}, the TPD1S414 turns on the nFET through a soft start to ensure that the USB Inrush current compliance is met. When the OVP condition is cleared and the nFET is completely turned on, the $\overline{ACK}$ is reset LOW.

Device Functional Modes (continued)

7.4.5 Host/OTG Mode

The TPD1S414's UVLO and OVP voltages are referenced to V_{BUS_CON} voltage. In OTG mode, V_{BUS_SYS} is driving the V_{BUS_CON}. Under this situation, initially V_{BUS_CON} is powered through the body diode of the nFET by V_{BUS_SYS}. Once the UVLO threshold on V_{BUS_CON} is met, the nFET turns on. If there is a short to ground on V_{BUS_CON} the OTG supply is expected to limit the current.

Table 2. Device Operation

VOLTAGE CONDITION			CURRENT CONDITION		
V_{BUS_CON}	V_{BUS_SYS}	$\overline{EN}$	CURRENT FLOW	COMMENT	$\overline{ACK}$ PIN
X	$<V_{BUS\_CON}$	High	No Flow	Switch off	High-Z
X	$>V_{BUS\_CON}$	High	V_{BUS_SYS} to V_{BUS_CON}	Switch off, current flows through the body diode	High-Z
<OVP	$<V_{BUS\_CON}$	Low	V_{BUS_CON} to V_{BUS_SYS}	Current flows through the switch, normal device charging mode	Low
<OVP	$>V_{BUS\_CON}$	Low	V_{BUS_SYS} to V_{BUS_CON}	Current flows through the switch, normal host mode	Low
>OVP	$<V_{BUS\_CON}$	Low	No Flow	Switch off due to OVP	High-Z
>OVP	$>V_{BUS\_CON}$	Low	V_{BUS_SYS} to V_{BUS_CON}	Switch off, current flows through the body diode	High-Z
X	X	X	No Flow/ Current through Body Diode	Thermal shutdown condition	High-Z
$<V_{UVLO}$	$<V_{BUS\_CON}$	Low	No Flow	Switch off, undervoltage lockout condition	High-Z

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD1S414 device is added to a USB system to provide 30-V overvoltage protection, IEC 61000-4-2 ±15-kV contact/±15-kV air-gap protection, and IEC61000-4-5 100-V open-circuit surge protection. This protection is essential for USB systems as many USB charging PMICs cannot tolerate the high voltages that can occur in a USB system due to lightening surge, cable ringing, and ESD strikes. The following application example shows the typical system set-up used for TPD1S414.

8.2 Typical Application

Figure 10 shows the typical system setup for TPD1S414, including external components required for proper functioning of the device.

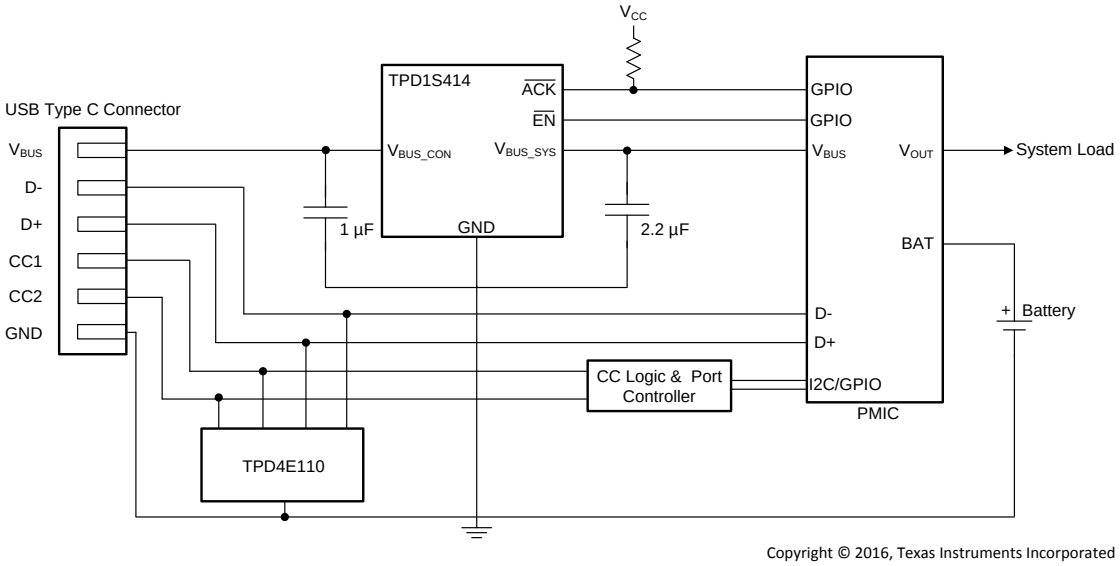


Figure 10. Typical Application Configuration for TPD1S414

8.2.1 Design Requirements

Table 3 lists the typical voltage values and external components used to operate the TPD1S414.

Table 3. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
USB Signal range on V_{BUS_CON}, V_{BUS_SYS}	4.4 V to 5.5 V
Operating current through V_{BUS}	3 A
Typical V_{BUS_CON} Capacitance	1 µF
Typical V_{BUS_SYS} Capacitance	2.2 µF
Drive $\overline{EN}$ low (enabled)	0 V to 0.8 V
Drive $\overline{EN}$ high (disabled)	1.2 V to 6 V

8.2.2 Detailed Design Procedure

8.2.2.1 USB V_{BUS} Voltage Range

The USB V_{BUS} voltage range for a USB device operates between a minimum of 4.4 V and a maximum of 5.5 V (Legacy USB has a maximum of 5.25 V, but the new USB Type C standard raised the maximum to 5.5 V). The TPD1S414 is designed to operate with a V_{BUS_CON}, V_{BUS_SYS} voltage between 3.5 V and 5.9 V. This range exceeds the requirements for USB V_{BUS}, allowing this device to be used in any USB system. Therefore, no special voltage precautions are necessary when adding TPD1S414 to a USB system.

8.2.2.2 USB V_{BUS} Operating Current

In this application example, a V_{BUS} current of 3 A is required. With the addition of the new USB Type C Standard, the VBUS operating current can vary anywhere from 0.5 A to 3 A, depending on the current capability advertised by the source on the CC pin. TPD1S414 is designed to operate up to a maximum of 3.5 A of current, allowing it to be used with the new USB Type C connector. TPD1S414 also has a low RON of 39 mΩ (typical), 50 mΩ (maximum), allowing for excellent thermal performance and low voltage drop across the switch at 3 A.

8.2.2.3 V_{BUS_CON} and V_{BUS_SYS} Capacitance

The USB standard requires a minimum capacitance of 1 µF on V_{BUS} and allows for a maximum capacitance of 10 µF on a USB device. The minimum capacitance is to reduce inductive spiking on V_{BUS} when disconnecting the charging cable, and the maximum capacitance is to put a limit on how much a device can drop the V_{BUS} rail of its host when being hot-plugged into the system. This corresponds to having a typical capacitance of 1 µF on V_{BUS_CON} for a USB system, but higher capacitance up to 10 µF can be used. No more than 10 µF must be put on V_{BUS_CON} to ensure the USB specification is not violated. If more capacitance is required, place this on the V_{BUS_SYS} pin. TPD1S414 turns on its nFET switch with a soft start to help pass USB in-rush compliance, so it is recommended to place bulk capacitance on the V_{BUS_SYS} pin. External capacitors added to the V_{BUS_CON} pin must be placed as close to the V_{BUS_CON} pin as possible, and likewise external capacitors added to the V_{BUS_SYS} pin must be placed as close to the V_{BUS_SYS} pin as possible.

8.2.2.4 IEC 61000-4-5 100-V Open-Circuit Surge

The IEC 61000-4-5 standard specifies the lightning and industrial surge model. Power lines like the V_{BUS} line on the USB port are subject to switching and lightning transients. Power supply switching transients can enter the system due to capacitor bank switching on the rail, minor load switching on the system and various system faults like arcing to the grounding system of the installation. Direct lightning to the outer installations cause an overvoltage condition on the V_{BUS} line. In the event of an overvoltage condition, the OVP block of the processor or the protection circuitry turns off isolating the system from these transients. Abruptly turning off the load, causes a further ripple due to the inductive nature of the charging cable. End systems require protection against these transients. These transients have greater energy than the ESD events. Systems cannot be protected from these transients using simple ESD diodes. The TPD1S414 has a precision trigger and precision clamping circuit that ensures a DC tolerance of 30 V while suppressing surge voltage up to 100 V under 35 V. Figure 11 shows the performance of TPD1S414 in the powered-down state under an 100-V surge pulse.

8.2.3 Application Curve

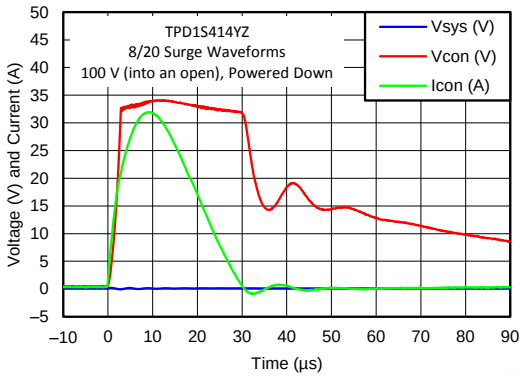


Figure 11. TPD1S414 Response to an 100-V Surge

9 Power Supply Recommendations

The TPD1S414 is designed to receive power from a USB V_{BUS} rail. It can operate normally (nFET ON) between a minimum of 3.5 V and a maximum of 5.9 V, well exceeding the USB device V_{BUS} voltage range of 4.4 V to 5.5 V. Place a capacitor with a minimum capacitance of 1 µF across system voltage range, system temperature range, and capacitor variation as close as possible to the V_{BUS_CON} pin on the PCB.

10 Layout

10.1 Layout Guidelines

TPD1S414 can be routed in a single-layer PCB. PCB traces to V_{BUS_SYS}, V_{BUS_CON}, and GND can be routed in the fashion shown in Figure 12.

Shorting all of the V_{BUS_SYS} pins together, all the V_{BUS_CON} pins together, and all the GND pins together helps provide the lowest resistance between the USB connector and the PMIC. For this example, the trace widths to V_{BUS_SYS}, V_{BUS_CON} are 25 mils (0.635 mm) under TPD1S414. There are no VIAs required within the SMD pads in this design. Stitching VIAs for GND can be placed near the component instead.

The decoupling capacitors per the *Recommended Operating Conditions* must be placed as close as possible to the TPD1S414. There must be a short path from the device ground pins to the system ground plane. This ensures best protection under ESD and surge transients.

10.2 Layout Example

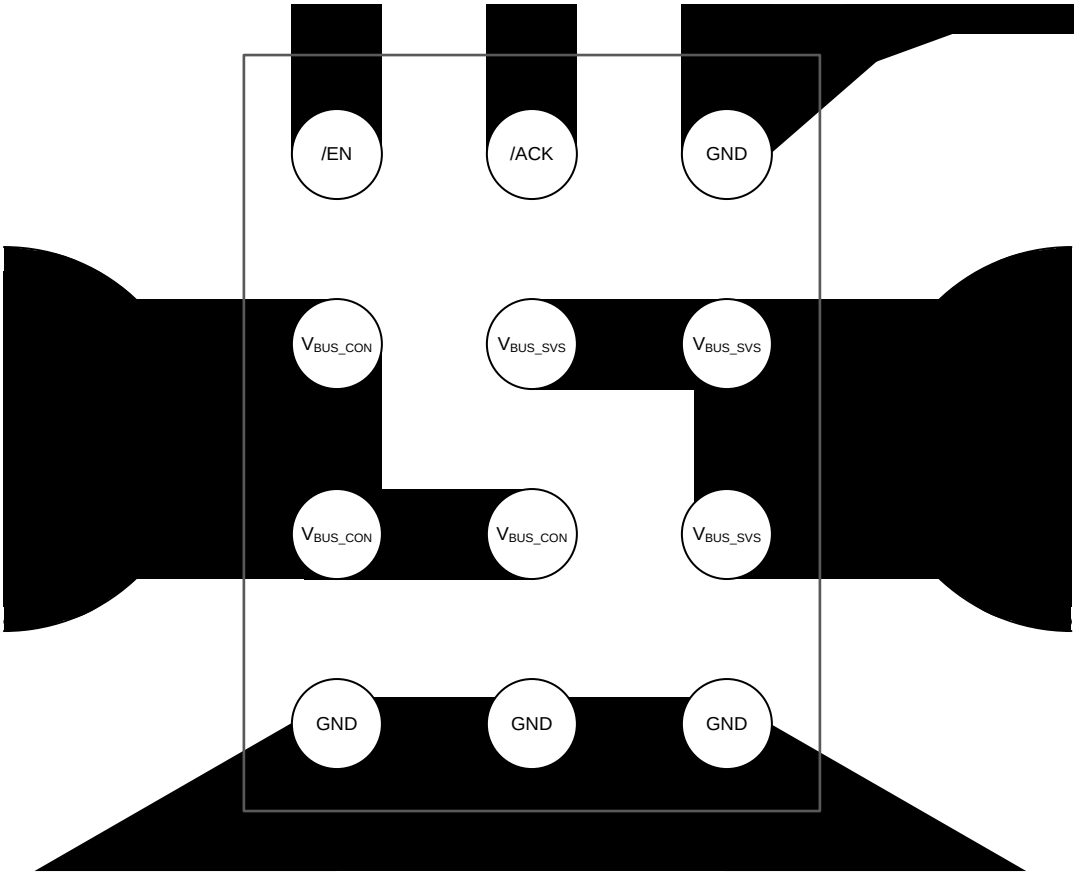


Figure 12. TPD1S414 Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

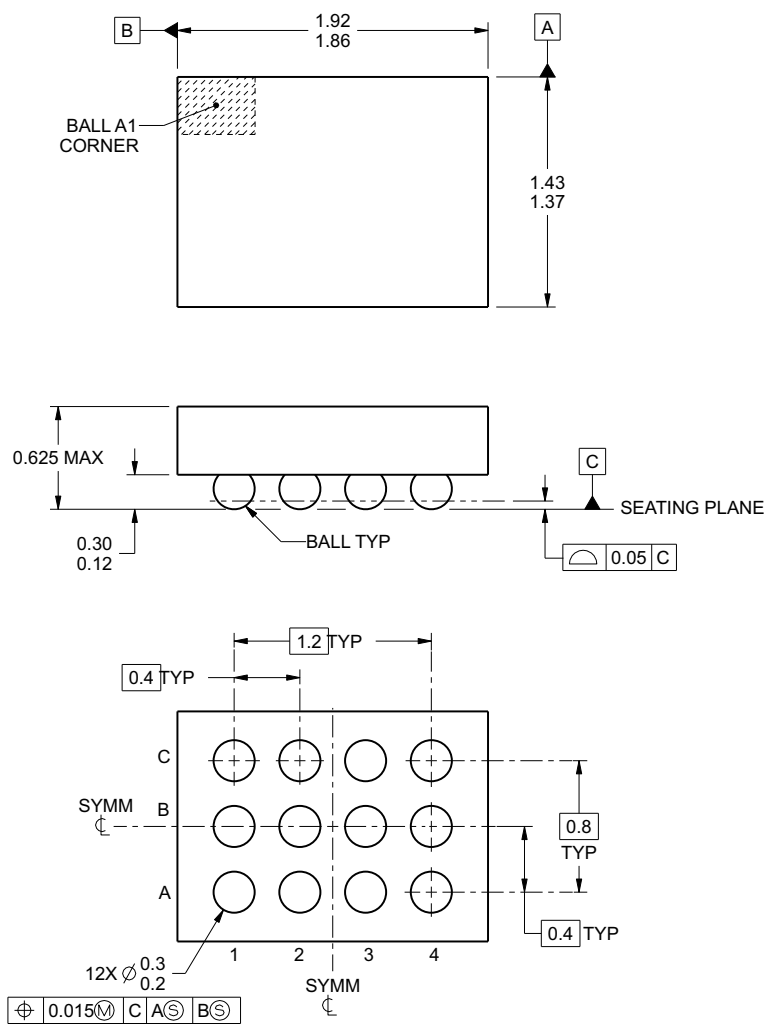
TPD1S414-xYZ

YZ0012-C02

PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

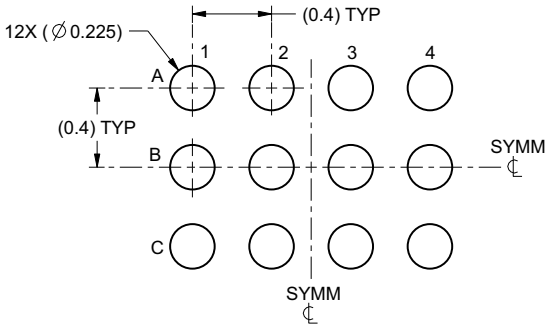
TPD1S414-xYZ

EXAMPLE BOARD LAYOUT

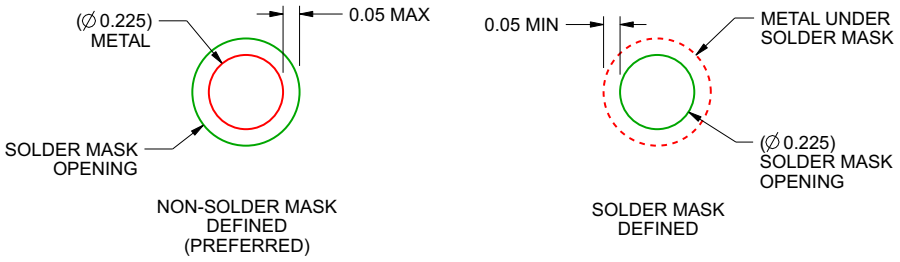
YZ0012-C02

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4222200/A 12/2015

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

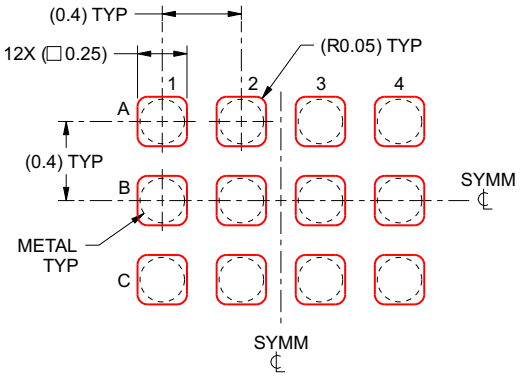
TPD1S414-xYZ

EXAMPLE STENCIL DESIGN

YZ0012-C02

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4222200/A 12/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1S414YZR	ACTIVE	DSBGA	YZ	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RH414	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

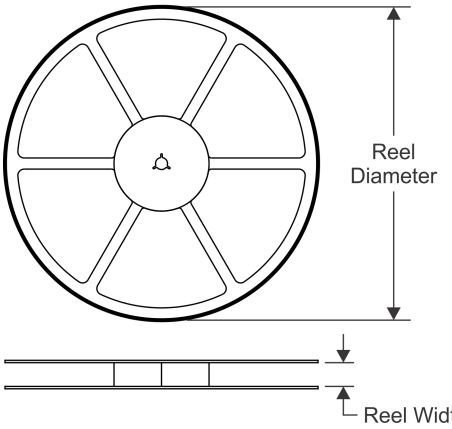
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

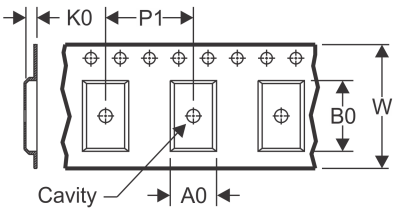
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

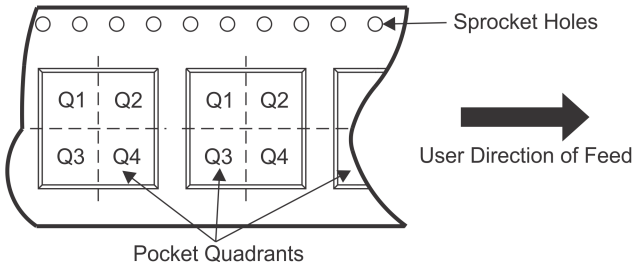


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

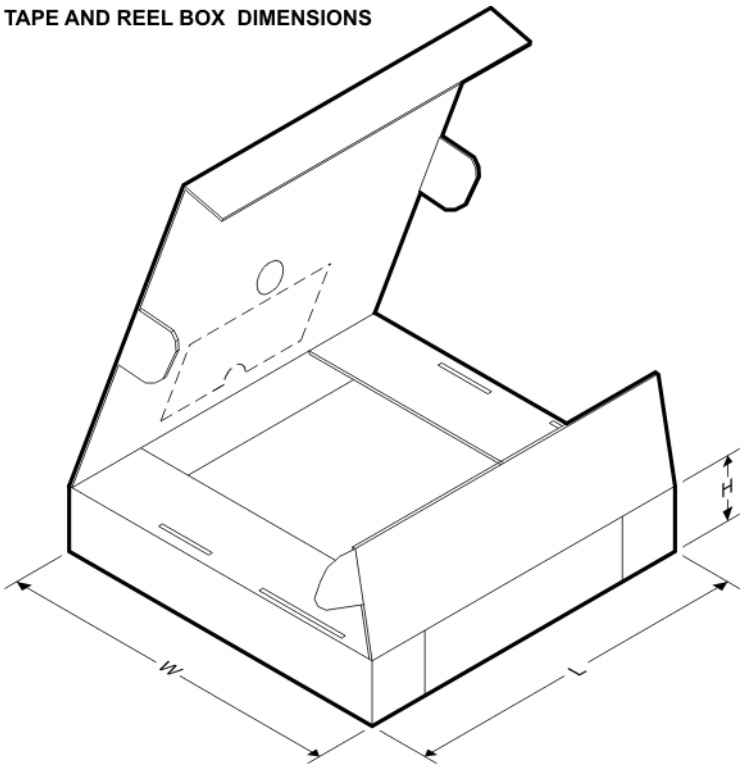
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1S414YZR	DSBGA	YZ	12	3000	180.0	8.4	1.5	1.99	0.75	4.0	8.0	Q2
TPD1S414YZR	DSBGA	YZ	12	3000	178.0	9.2	1.49	1.99	0.75	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1S414YZR	DSBGA	YZ	12	3000	182.0	182.0	20.0
TPD1S414YZR	DSBGA	YZ	12	3000	220.0	220.0	35.0

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