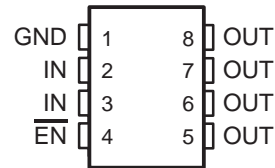
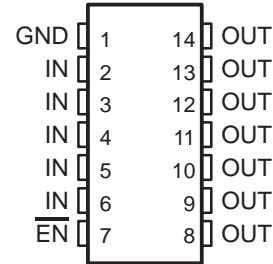


- **95-mΩ Max (5.5-V Input) High-Side MOSFET Switch With Logic Compatible Enable Input**
- **Short-Circuit and Thermal Protection**
- **Typical Short-Circuit Current Limits:**
0.4 A, TPS2010; 1.2 A, TPS2011;
2 A, TPS2012; 2.6 A, TPS2013
- **Electrostatic-Discharge Protection, 12-kV Output, 6-kV All Other Terminals**
- **Controlled Rise and Fall Times to Limit Current Surges and Minimize EMI**
- **SOIC-8 Package Pin Compatible With the Popular Littlefoot™ Series When GND Is Connected**
- **2.7-V to 5.5-V Operating Range**
- **10-μA Maximum Standby Current**
- **Surface-Mount SOIC-8 and TSSOP-14 Packages**
- **–40°C to 125°C Operating Junction Temperature Range**

**D PACKAGE
(TOP VIEW)**



**PW PACKAGE
(TOP VIEW)**



description

The TPS201x family of power-distribution switches is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The high-side switch is a 95-mΩ N-channel MOSFET. Gate drive is provided by an internal driver and charge pump designed to control the power switch rise times and fall times to minimize current surges during switching. The charge pump operates at 100 kHz, requires no external components, and allows operation from supplies as low as 2.7 V. When the output load exceeds the current-limit threshold or a short circuit is present, the TPS201x limits the output current to a safe level by switching into a constant-current mode. Continuous heavy overloads and short circuits increase power dissipation in the switch and cause the junction temperature to rise. If the junction temperature reaches approximately 180°C, a thermal protection circuit shuts the switch off to prevent damage. Recovery from thermal shutdown is automatic once the device has cooled sufficiently.

The members of the TPS201x family differ only in short-circuit current threshold. The TPS2010 is designed to limit at 0.4-A load; the other members of the family limit at 1.2 A, 2 A, and 2.6 A (see the available options table). The TPS201x family is available in 8-pin small-outline integrated circuit (SOIC) and 14-pin thin shink small-outline (TSSOP) packages and operates over a junction temperature range of –40°C to 125°C. Versions in the 8-pin SOIC package are drop-in replacements for Siliconix's Littlefoot™ power PMOS switches, except that GND must be connected.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1995, Texas Instruments Incorporated

detailed description (continued)**driver**

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range instead of the microsecond or nanosecond range for a standard FET.

enable ($\overline{\text{EN}}$)

A logic high on the $\overline{\text{EN}}$ input turns off the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μA . A logic zero input restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

current sense

A sense FET monitors the current supplied to the load. The sense FET is a much more efficient way to measure current than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its linear region, which switches the output into a constant current mode and simply holds the current constant while varying the voltage on the load.

thermal sense

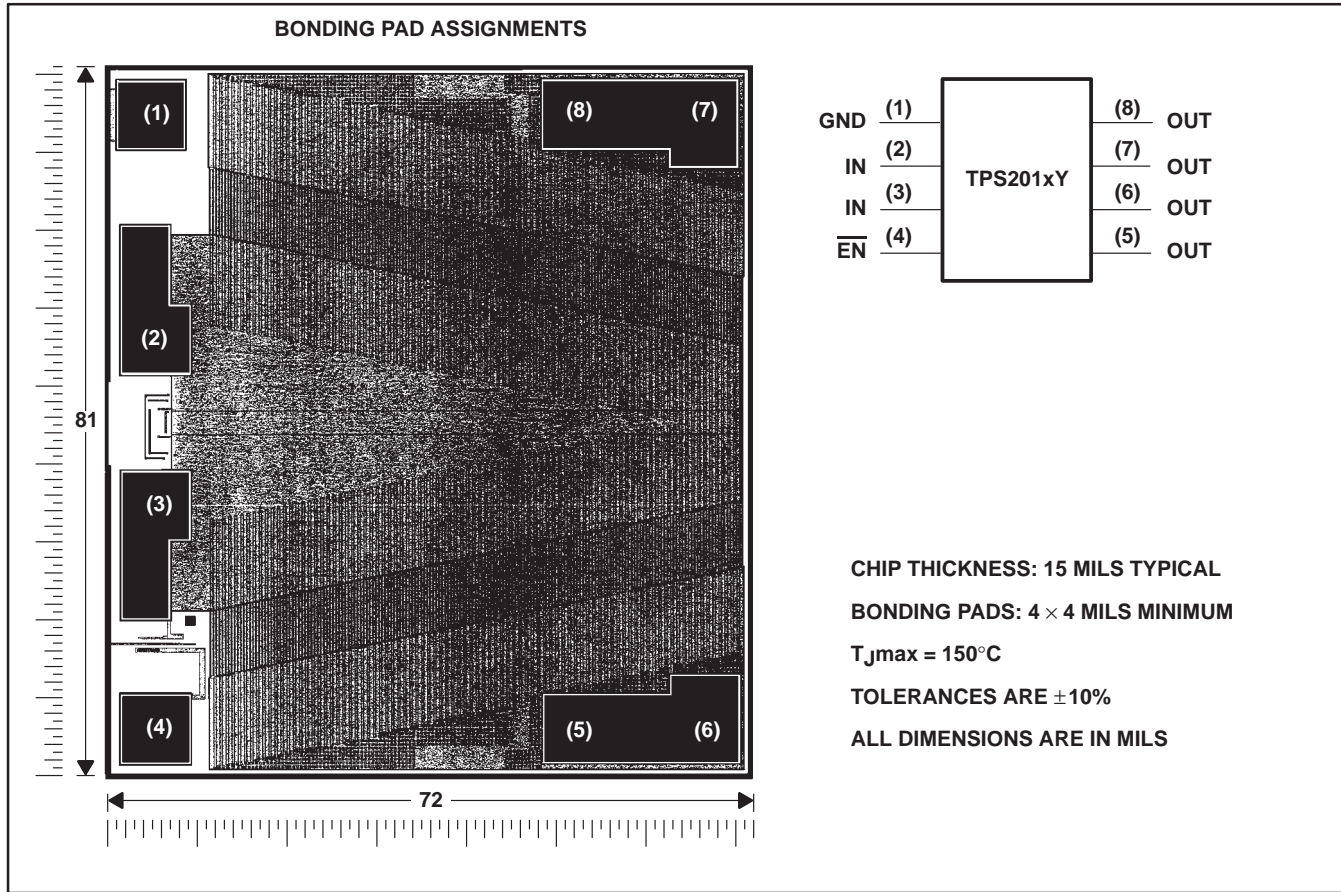
An internal thermal-sense circuit shuts the power switch off when the junction temperature rises to approximately 180°C. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

TPS201xY chip information

This chip, when properly assembled, displays characteristics similar to the TPS201xC. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

TPS2010, TPS2011, TPS2012, TPS2013 POWER-DISTRIBUTION

SLVS097A – DECEMBER 1994 – REVISED AUGUST 1995



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note 1)	−0.3 V to 7 V
Output voltage range, V_O (see Note 1)	−0.3 V to $V_{I(IN)} + 0.3$ V
Input voltage range, V_I at $\overline{\text{EN}}$	−0.3 V to 7 V
Continuous output current, I_O	internally limited
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
PW	700 mW	5.6 mW/°C	448 mW	140 mW



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, $V_{I(IN)}$		2.7	5.5	V
Input voltage, V_I at \overline{EN}		0	5.5	V
Continuous output current, I_O	TPS2010	0	0.2	A
	TPS2011	0	0.6	
	TPS2012	0	1	
	TPS2013	0	1.5	
Operating virtual junction temperature, T_J		-40	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)} = 5.5$ V, $I_O =$ rated current, $\overline{EN} = 0$ V (unless otherwise noted)

power switch

PARAMETER	TEST CONDITIONS†	TPS2010, TPS2011 TPS2012, TPS2013			UNIT
		MIN	TYP	MAX	
On-state resistance	$V_{I(IN)} = 5.5$ V, $T_J = 25^\circ\text{C}$		75	95	mΩ
	$V_{I(IN)} = 4.5$ V, $T_J = 25^\circ\text{C}$		80	110	
	$V_{I(IN)} = 3$ V, $T_J = 25^\circ\text{C}$		120	175	
	$V_{I(IN)} = 2.7$ V, $T_J = 25^\circ\text{C}$		140	215	
Output leakage current	$\overline{EN} = V_{I(IN)}$, $T_J = 25^\circ\text{C}$		0.001	1	μA
	$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			10	
t_r Output rise time	$V_{I(IN)} = 5.5$ V, $T_J = 25^\circ\text{C}$, $C_L = 1$ μF		4		ms
	$V_{I(IN)} = 2.7$ V, $T_J = 25^\circ\text{C}$, $C_L = 1$ μF		3.8		
t_f Output fall time	$V_{I(IN)} = 5.5$ V, $T_J = 25^\circ\text{C}$, $C_L = 1$ μF		3.9		ms
	$V_{I(IN)} = 2.7$ V, $T_J = 25^\circ\text{C}$, $C_L = 1$ μF		3.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input (\overline{EN})

PARAMETER	TEST CONDITIONS	TPS2010, TPS2011 TPS2012, TPS2013			UNIT
		MIN	TYP	MAX	
High-level input voltage	$2.7 \text{ V} \leq V_{I(IN)} \leq 5.5 \text{ V}$	2			V
Low-level input voltage	$4.5 \text{ V} \leq V_{I(IN)} \leq 5.5 \text{ V}$			0.8	V
	$2.7 \text{ V} \leq V_{I(IN)} < 4.5 \text{ V}$			0.4	
Input current	$\overline{EN} = 0$ V or $\overline{EN} = V_{I(IN)}$	-0.5		0.5	μA
t_{PLH} Propagation (delay) time, low-to-high-level output	$C_L = 1$ μF			20	ms
t_{PHL} Propagation (delay) time, high-to-low-level output	$C_L = 1$ μF			40	

current limit

PARAMETER	TEST CONDITIONS†	TPS2010, TPS2011 TPS2012, TPS2013			UNIT	
		MIN	TYP	MAX		
Short-circuit current	$T_J = 25^\circ\text{C}$, $V_{I(IN)} = 5.5$ V, OUT connected to GND, device enabled into short circuit	TPS2010	0.22	0.4	0.6	A
		TPS2011	0.66	1.2	1.8	
		TPS2012	1.1	2	3	
		TPS2013	1.65	2.6	4.5	

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

TPS2010, TPS2011, TPS2012, TPS2013 POWER-DISTRIBUTION

SLVS097A – DECEMBER 1994 – REVISED AUGUST 1995

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)} = 5.5\text{ V}$, $I_O = \text{rated current}$, $\overline{EN} = 0\text{ V}$ (unless otherwise noted) (continued)

supply current

PARAMETER	TEST CONDITIONS	TPS2010, TPS2011 TPS2012, TPS2013			UNIT
		MIN	TYP	MAX	
Supply current, low-level output	$\overline{EN} = V_{I(IN)}$	$T_J = 25^\circ\text{C}$	0.015	1	μA
		$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		10	
Supply current, high-level output	$\overline{EN} = 0\text{ V}$	$T_J = 25^\circ\text{C}$	73	100	μA
		$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		100	

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)} = 5.5\text{ V}$, $I_O = \text{rated current}$, $\overline{EN} = 0\text{ V}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

power switch

PARAMETER	TEST CONDITIONST	TPS2010Y, TPS2011Y TPS2012Y, TPS2013Y			UNIT
		MIN	TYP	MAX	
On-state resistance	$V_{I(IN)} = 5.5\text{ V}$,		75		$\text{m}\Omega$
	$V_{I(IN)} = 4.5\text{ V}$,		80		
	$V_{I(IN)} = 3\text{ V}$,		120		
	$V_{I(IN)} = 2.7\text{ V}$,		140		
Output leakage current	$\overline{EN} = V_{I(IN)}$		0.001		μA
Output rise time	$V_{I(IN)} = 5.5\text{ V}$, $C_L = 1\text{ }\mu\text{F}$		4		ms
	$V_{I(IN)} = 2.7\text{ V}$, $C_L = 1\text{ }\mu\text{F}$		3.8		
Output fall time	$V_{I(IN)} = 5.5\text{ V}$, $C_L = 1\text{ }\mu\text{F}$		3.9		ms
	$V_{I(IN)} = 2.7\text{ V}$, $C_L = 1\text{ }\mu\text{F}$		3.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

current limit

PARAMETER	TEST CONDITIONST	TPS2010Y, TPS2011Y TPS2012Y, TPS2013Y			UNIT
		MIN	TYP	MAX	
Short-circuit current	$V_{I(IN)} = 5.5\text{ V}$, OUT connected to GND, Device enabled into short circuit		0.4		A

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

supply current

PARAMETER	TEST CONDITIONS	TPS2010Y, TPS2011Y TPS2012Y, TPS2013Y			UNIT
		MIN	TYP	MAX	
Supply current, low-level output	$\overline{EN} = V_{I(IN)}$		0.015		μA
Supply current, high-level output	$\overline{EN} = 0\text{ V}$		73		μA



PARAMETER MEASUREMENT INFORMATION

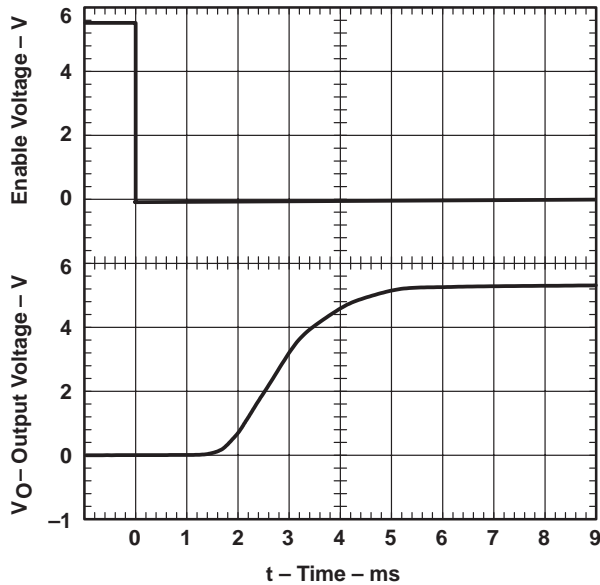


Figure 1. Propagation Delay and Rise Time With 1- μ F Load, $V_{I(IN)} = 5.5$ V

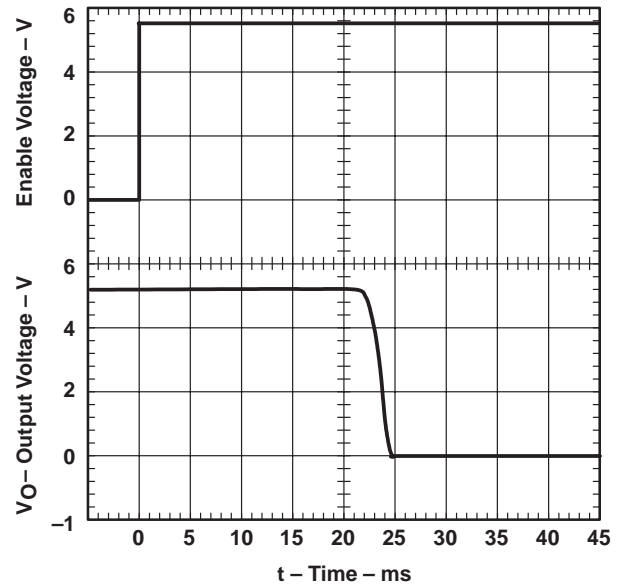


Figure 2. Propagation Delay and Fall Time With 1- μ F Load, $V_{I(IN)} = 5.5$ V

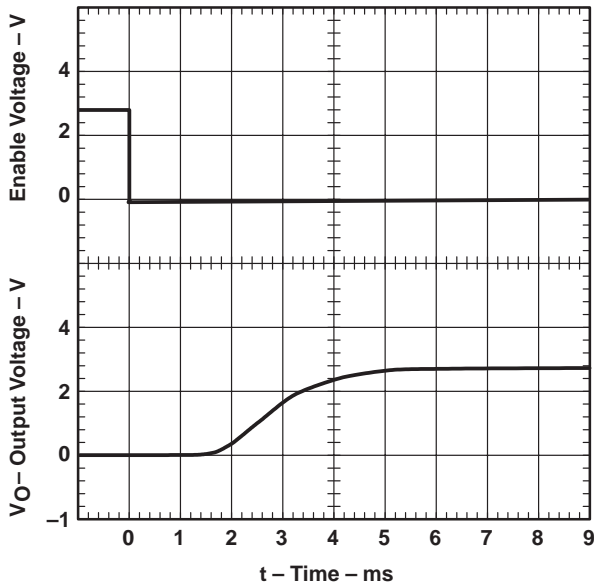


Figure 3. Propagation Delay and Rise Time With 1- μ F Load, $V_{I(IN)} = 2.7$ V

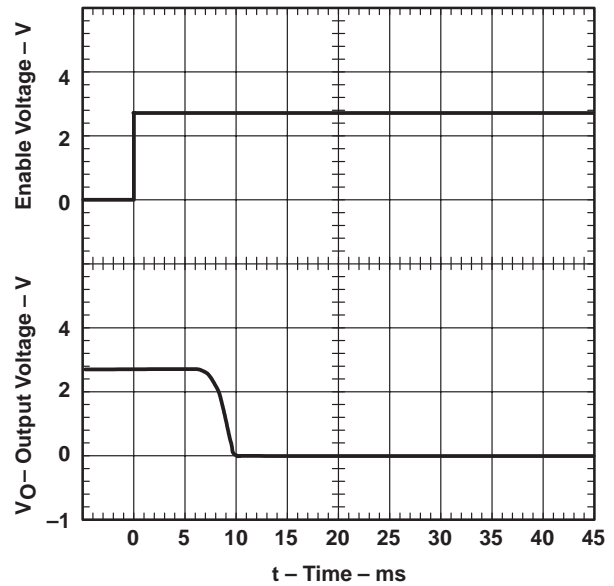


Figure 4. Propagation Delay and Fall Time With 1- μ F Load, $V_{I(IN)} = 2.7$ V

PARAMETER MEASUREMENT INFORMATION

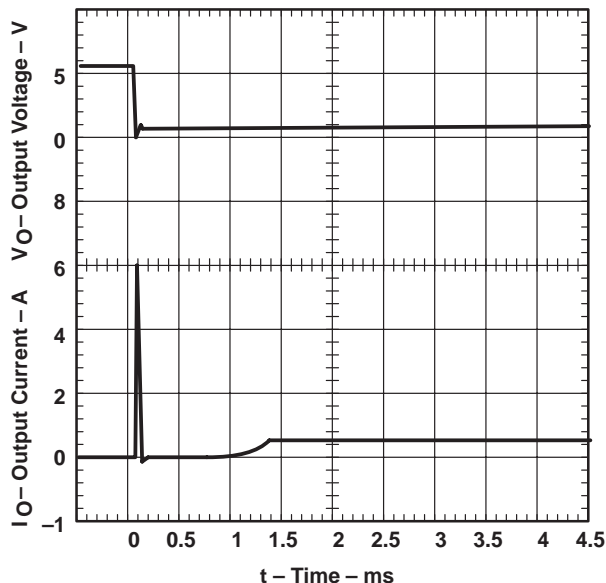


Figure 5. TPS2010, Short-Circuit Current.
Short is Applied to Enabled Device, $V_{I(IN)} = 5.5\text{ V}$

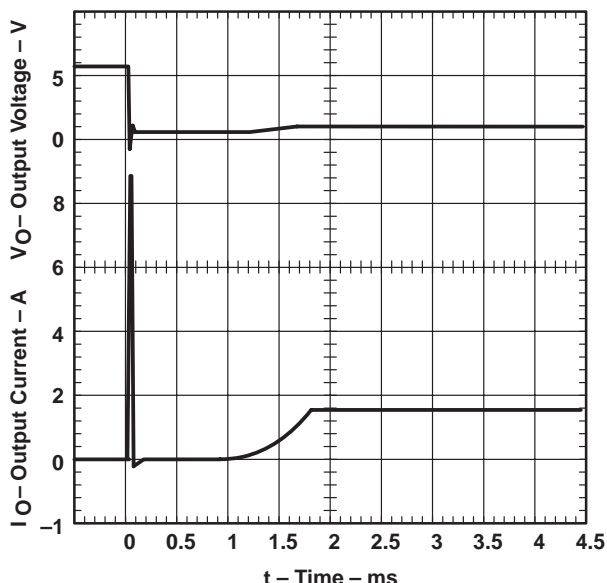


Figure 6. TPS2011, Short-Circuit Current.
Short is Applied to Enabled Device, $V_{I(IN)} = 5.5\text{ V}$

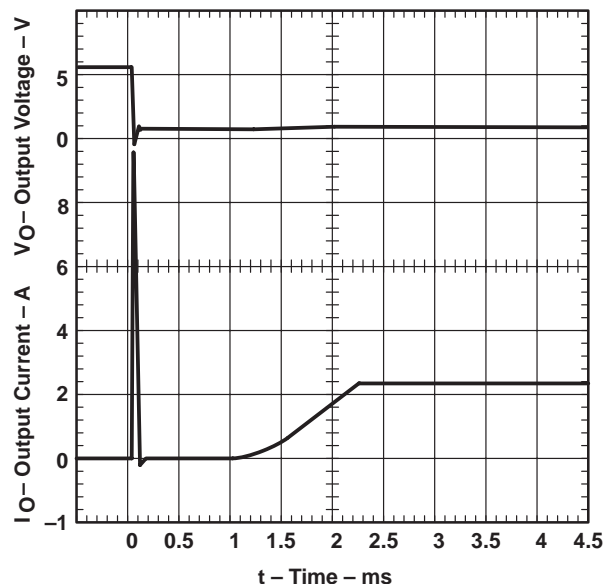


Figure 7. TPS2012, Short-Circuit Current.
Short is Applied to Enabled Device, $V_{I(IN)} = 5.5\text{ V}$

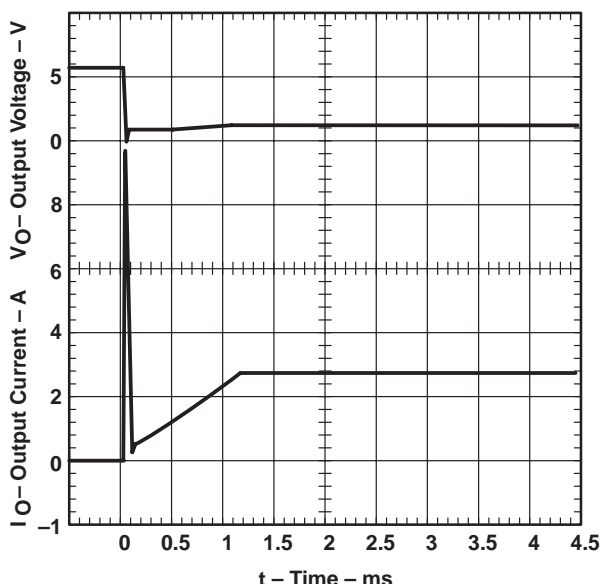


Figure 8. TPS2013 – Short-Circuit Current.
Short is Applied to Enabled Device, $V_{I(IN)} = 5.5\text{ V}$

PARAMETER MEASUREMENT INFORMATION

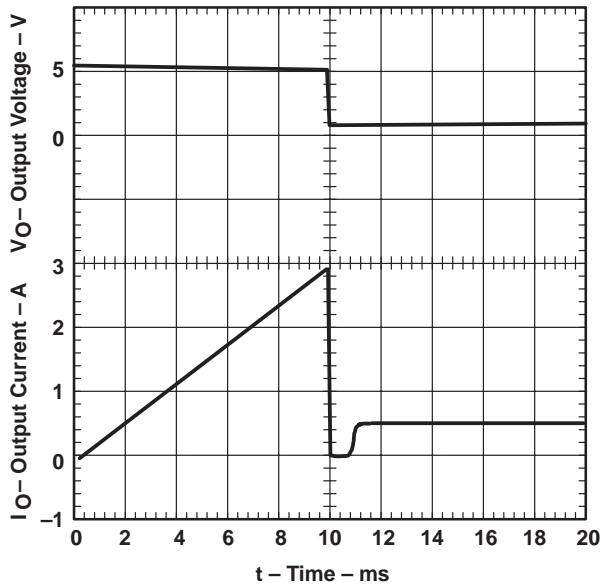


Figure 9. TPS2010 – Threshold Current,
 $V_{I(IN)} = 5.5\text{ V}$

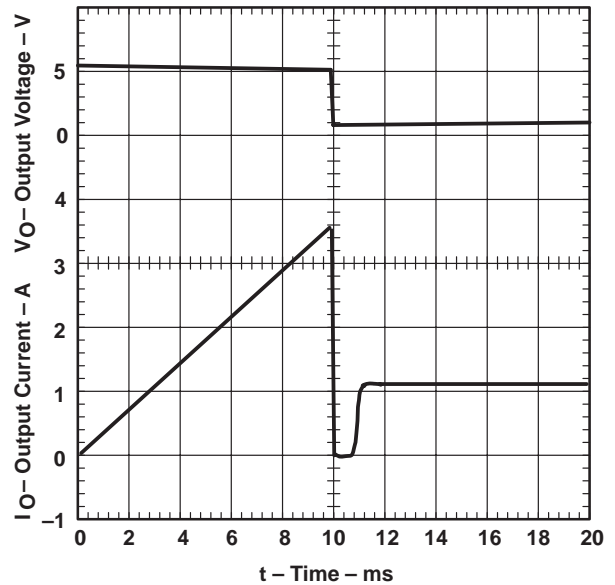


Figure 10. TPS2011 – Threshold Current,
 $V_{I(IN)} = 5.5\text{ V}$

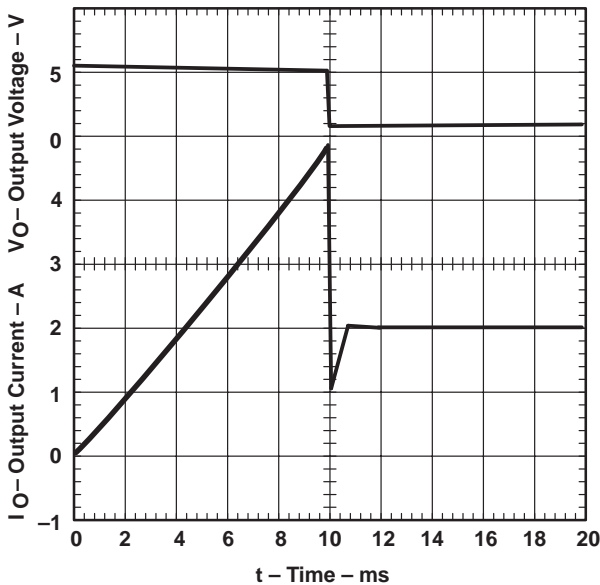


Figure 11. TPS2012 – Threshold Current,
 $V_{I(IN)} = 5.5\text{ V}$

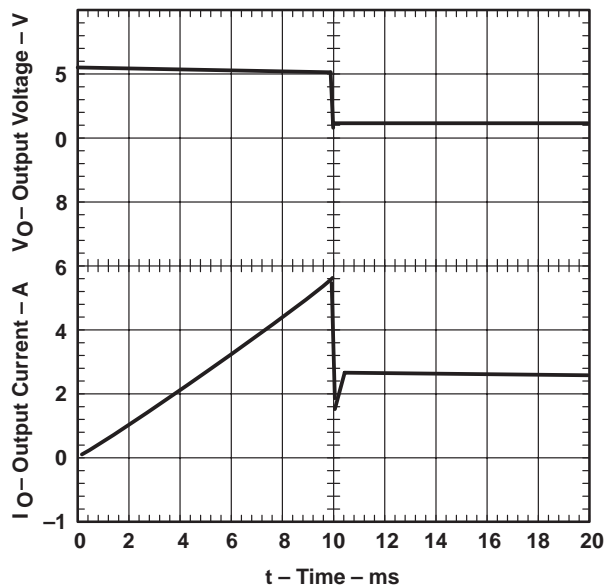


Figure 12. TPS2013 – Threshold Current,
 $V_{I(IN)} = 5.5\text{ V}$

PARAMETER MEASUREMENT INFORMATION

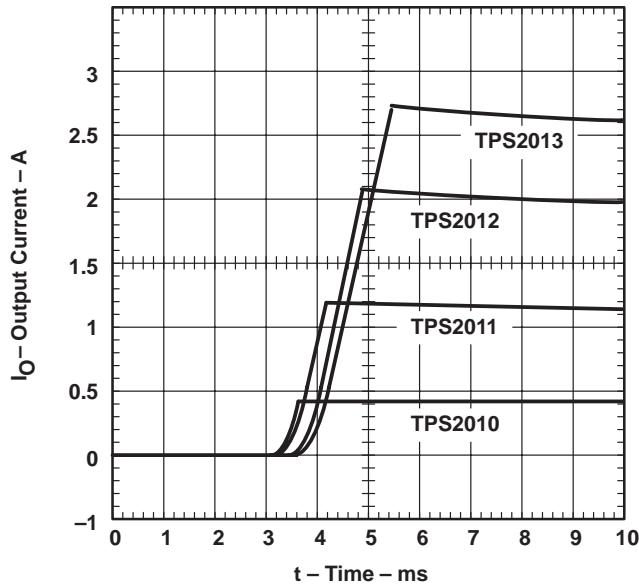


Figure 13. Turned-On (Enabled) Into Short Circuit, $V_{I(IN)} = 5.5 V$

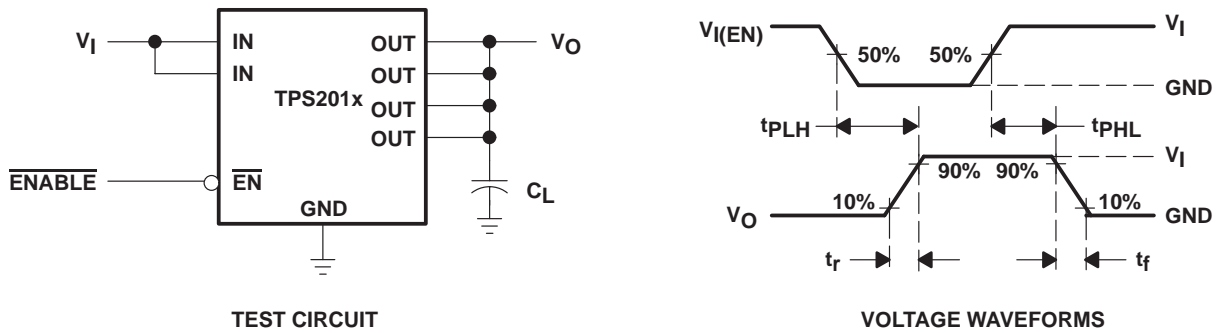


Figure 14. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

TURN-ON DELAY TIME
vs
INPUT VOLTAGE

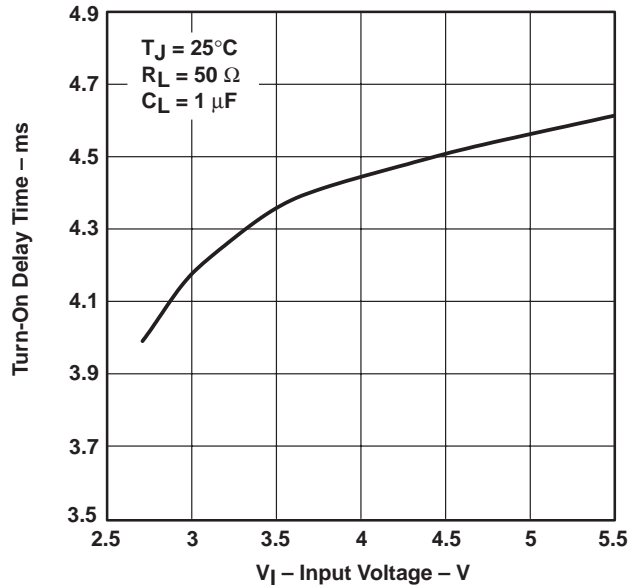


Figure 15

TURN-OFF DELAY TIME
vs
INPUT VOLTAGE

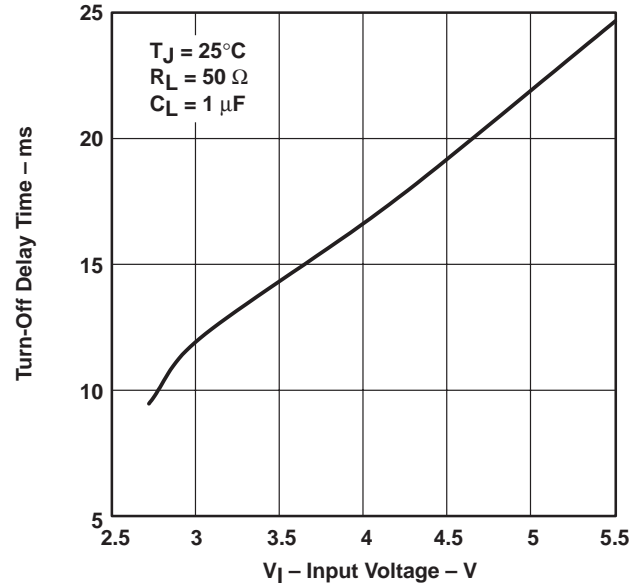


Figure 16

RISE TIME
vs
OUTPUT CURRENT

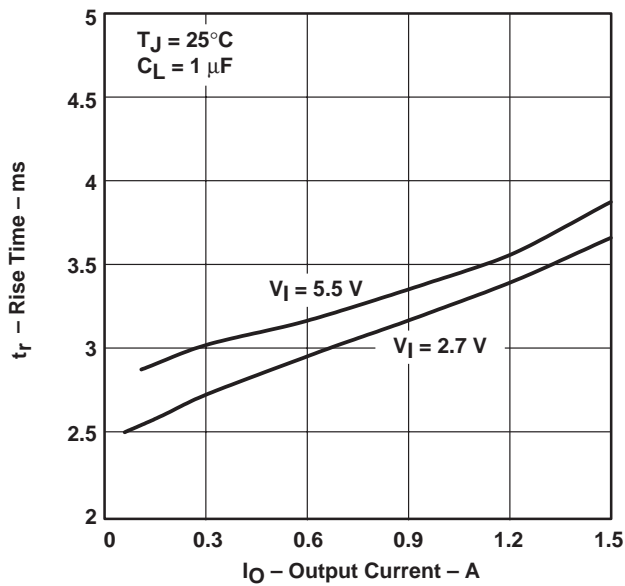


Figure 17

FALL TIME
vs
OUTPUT CURRENT

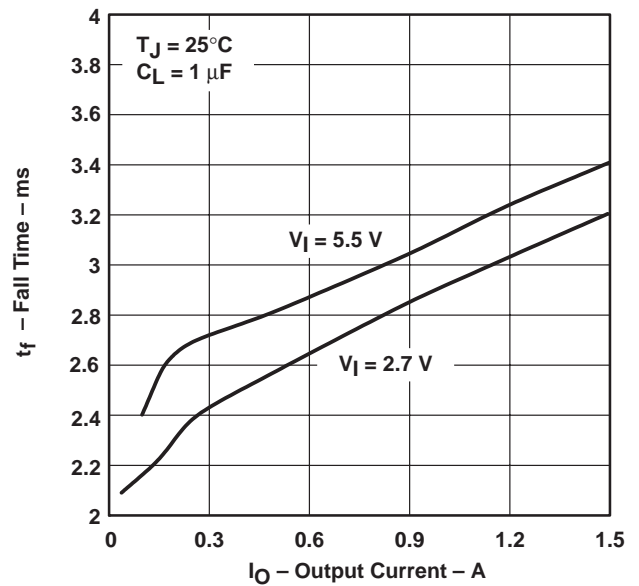


Figure 18

TYPICAL CHARACTERISTICS

SUPPLY CURRENT (OUTPUT ENABLED)
vs
JUNCTION TEMPERATURE

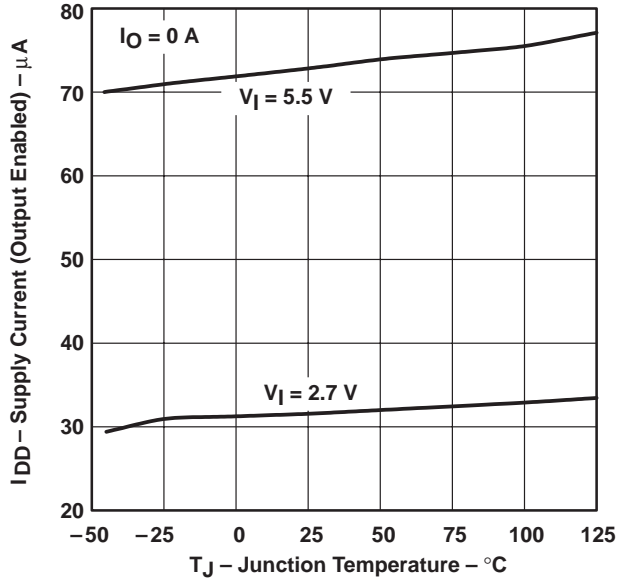


Figure 19

SUPPLY CURRENT (OUTPUT DISABLED)
vs
JUNCTION TEMPERATURE

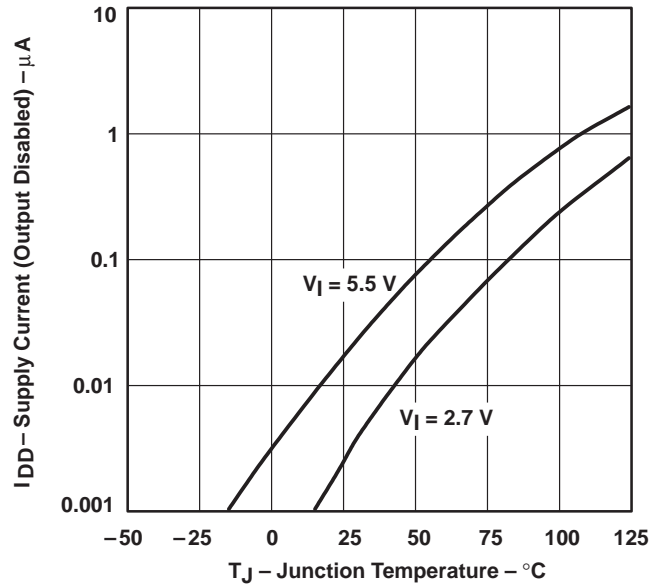


Figure 20

SUPPLY CURRENT (OUTPUT ENABLED)
vs
INPUT VOLTAGE

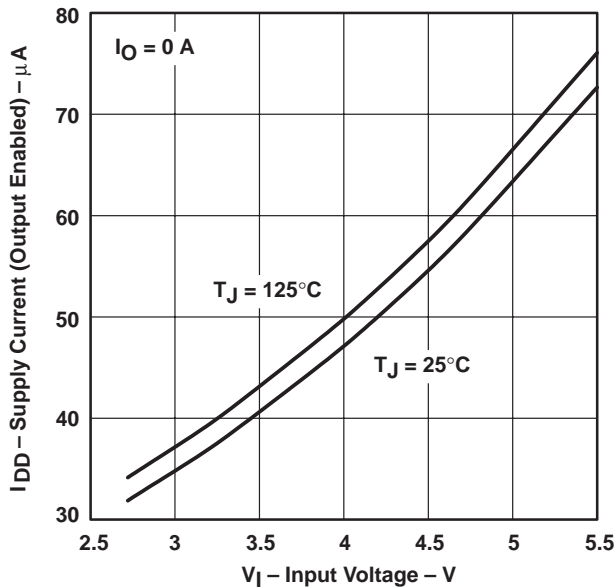


Figure 21

SUPPLY CURRENT (OUTPUT DISABLED)
vs
INPUT VOLTAGE

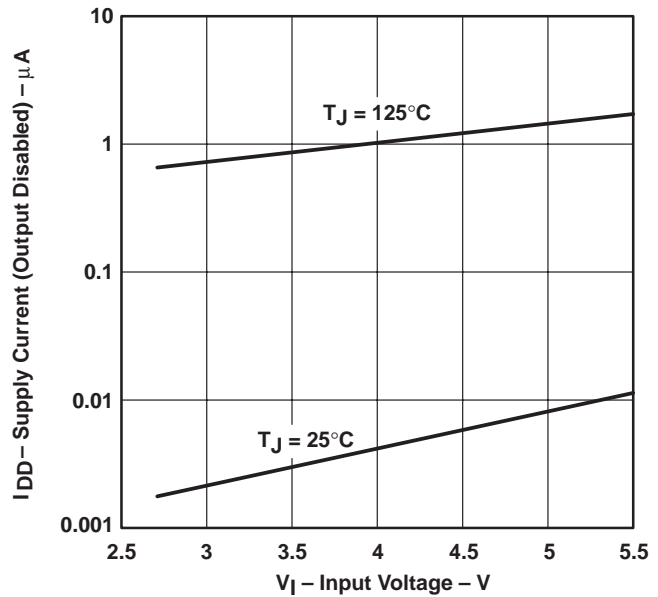


Figure 22

TYPICAL CHARACTERISTICS

ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

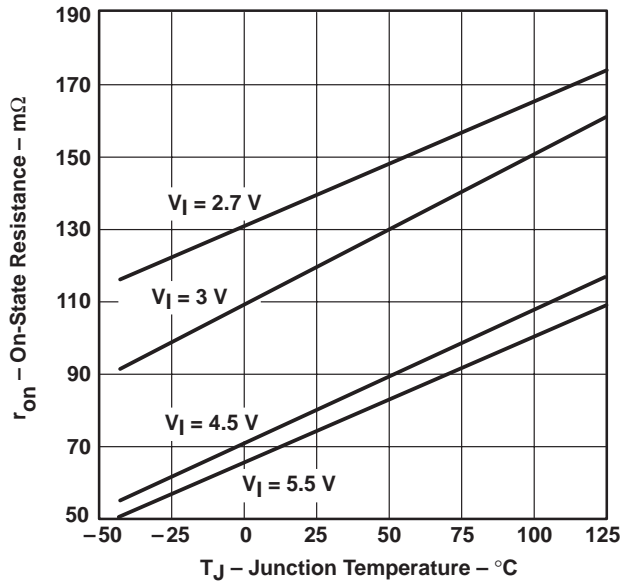


Figure 23

ON-STATE RESISTANCE
vs
INPUT VOLTAGE

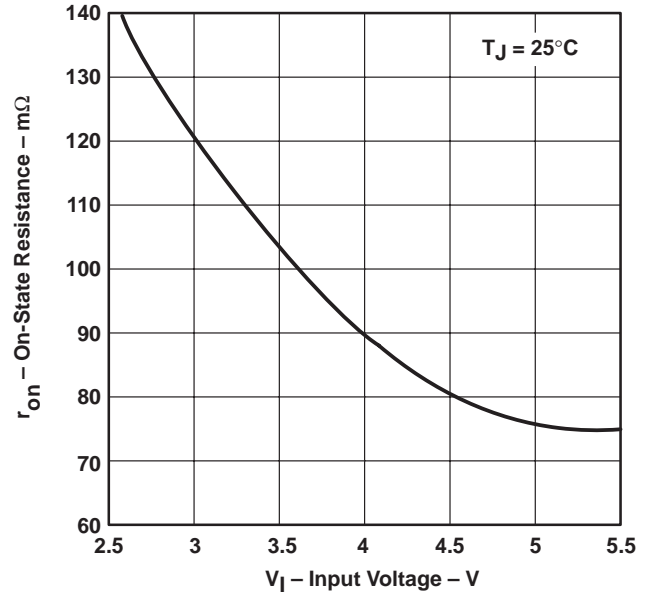


Figure 24

INPUT VOLTAGE TO OUTPUT VOLTAGE
vs
INPUT VOLTAGE

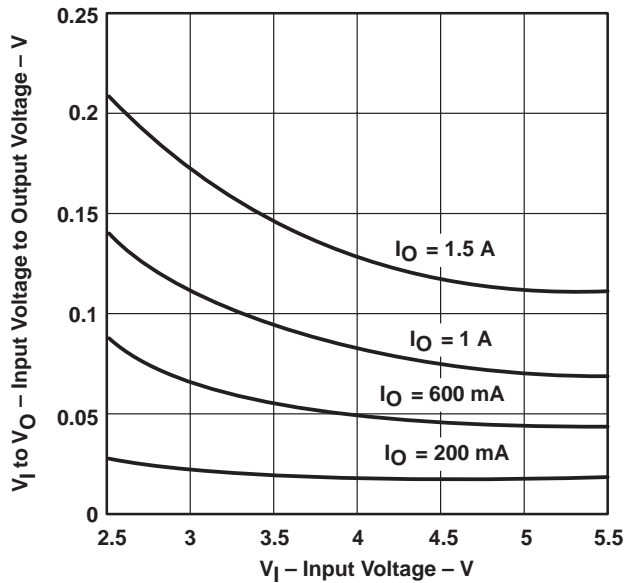


Figure 25

SHORT-CIRCUIT CURRENT
vs
INPUT VOLTAGE

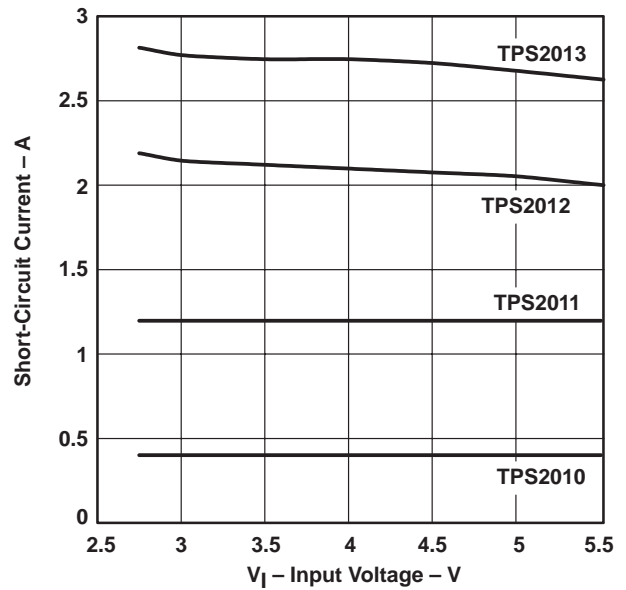


Figure 26

TYPICAL CHARACTERISTICS

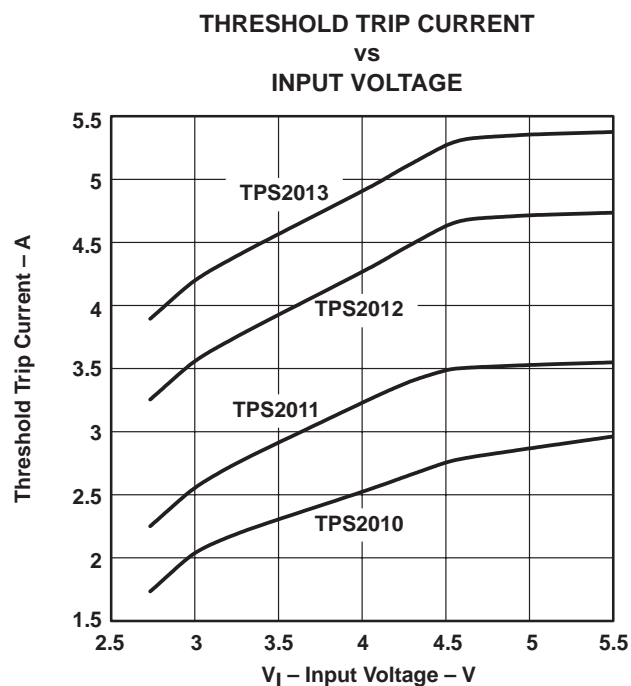


Figure 27

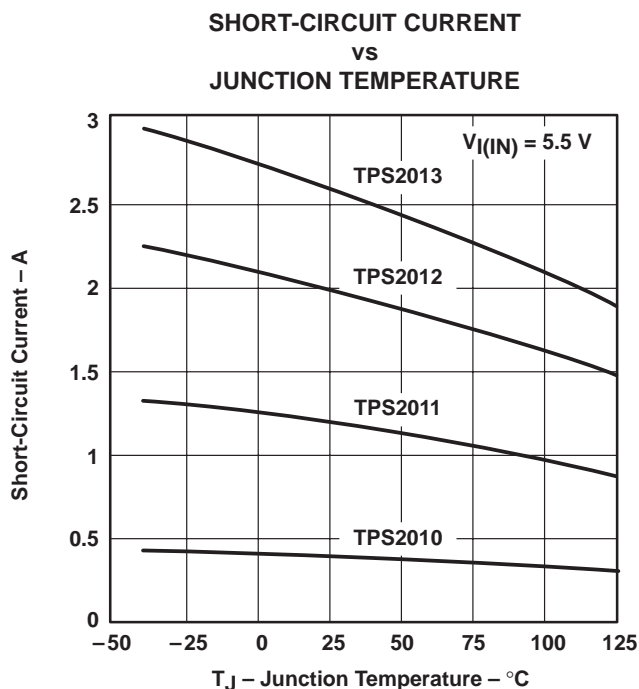


Figure 28

APPLICATION INFORMATION

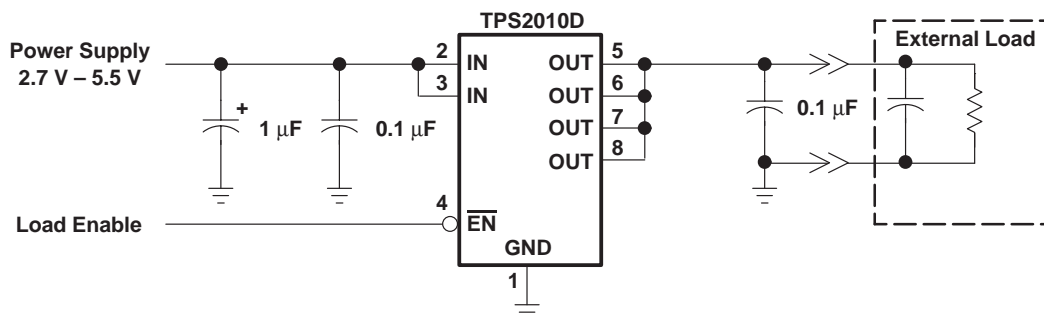


Figure 29. Typical Application

power supply considerations

The TPS201x family has multiple inputs and outputs, which must be connected in parallel to minimize voltage drop and prevent unnecessary power dissipation.

A 0.047-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. A high-value electrolytic capacitor is also desirable when the output load is heavy or has large paralleled capacitors. Bypassing the output with a 0.1-µF ceramic capacitor improves the immunity of the device to electrostatic discharge (ESD).

APPLICATION INFORMATION

overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike sense resistors and polyfuses, sense FETs do not increase series resistance to the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Shutdown only occurs if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 30). The TPS201x senses the short and immediately switches into a constant-current output.

Under the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents flow for a short time before the current-limit circuit can react (see Figures 5, 6, 7, and 8). After the current-limit circuit has tripped, the device limits normally.

Under the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached (see Figures 9, 10, 11, and 12). The TPS201x family is capable of delivering currents up to the current-limit threshold without damage. Once the threshold has been reached, the device switches into its constant-current mode.

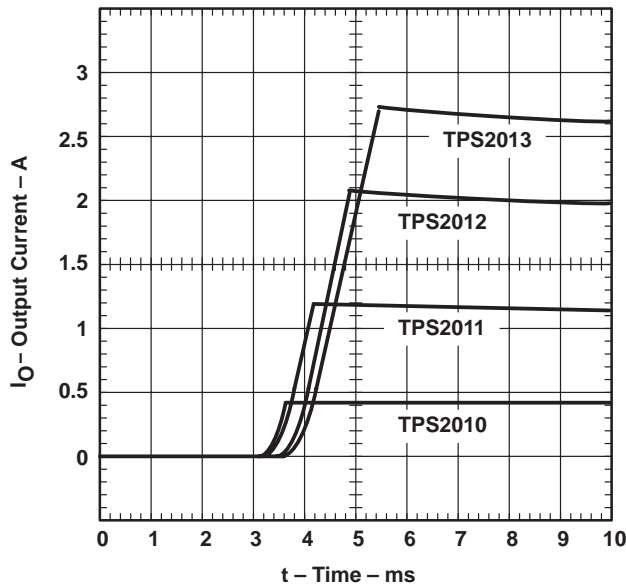


Figure 30. Turned-On (Enabled) Into Short Circuit, $V_{I(IN)} = 5.5\text{ V}$

APPLICATION INFORMATION

power dissipation and junction temperature

The low on resistance of the N-channel MOSFET allows small surface-mount packages, such as SOIC or TSSOP to pass large currents. The thermal resistances of these packages are high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find r_{on} at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read r_{on} from Figure 23. Next calculate the power dissipation using:

$$P_D = r_{on} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient temperature

$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, TSSOP = 179°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

thermal protection

Thermal protection is provided to prevent damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS201x into its constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to dangerously high levels. The protection circuit senses the junction temperature of the switch and shuts it off. The switch remains off until the junction has dropped approximately 20°C. The switch continues to cycle in this manner until the load fault or input power is removed.

ESD protection

All TPS201x terminals incorporate ESD-protection circuitry designed to withstand a 6-kV human-body-model discharge as defined in MIL-STD-883C. Additionally, the output is protected from discharges up to 12 kV.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2010D	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2010	
TPS2010DG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2010	
TPS2010DR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2010	
TPS2010DRG4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2010	
TPS2011D	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2011	
TPS2011DG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2011	
TPS2011DR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2011	
TPS2011DRG4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2011	
TPS2012D	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2012	
TPS2012DG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2012	
TPS2012DR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2012	
TPS2012DRG4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2012	
TPS2013D	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2013	
TPS2013DG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2013	
TPS2013DR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2013	
TPS2013DRG4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2013	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2010DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2011DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2012DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2013DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2010DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2011DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2012DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2013DR	SOIC	D	8	2500	340.5	338.1	20.6

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.