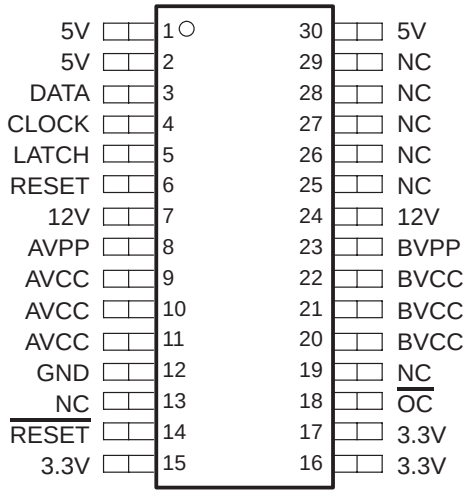
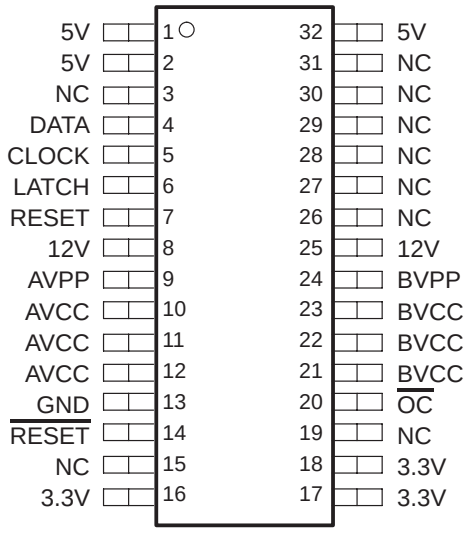
- **Fully Integrated V_{CC} and V_{pp} Switching for Dual-Slot PC Card™ Interface**
- **P²C™ 3-Lead Serial Interface Compatible With CardBus™ Controllers**
- **3.3 V Low-Voltage Mode**
- **Meets PC Card Standards**
- **RESET for System Initialization of PC Cards**
- **12-V Supply Can Be Disabled Except During 12-V Flash Programming**
- **Short Circuit and Thermal Protection**
- **30-Pin SSOP (DB) and 32-Pin TSSOP (DAP)**
- **Compatible With 3.3-V, 5-V and 12-V PC Cards**
- **Low $r_{DS(on)}$ (140-mΩ 5-V V_{CC} Switch; 110-mΩ 3.3-V V_{CC} Switch)**
- **Break-Before-Make Switching**

DB OR DF PACKAGE
(TOP VIEW)



DAP PACKAGE
(TOP VIEW)



NC − No internal connection

description

The TPS2206 PC Card power-interface switch provides an integrated power-management solution for two PC Cards. All of the discrete power MOSFETs, a logic section, current limiting, and thermal protection for PC Card control are combined on a single integrated circuit (IC), using the Texas Instruments LinBiCMOS™ process. The circuit allows the distribution of 3.3-V, 5-V, and/or 12-V card power by means of the P²C (PCMCIA Peripheral-Control) Texas Instruments nonproprietary serial interface. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability.

The TPS2206 is backward compatible with the TPS2202 and TPS2202A, except that there is no V_{DD} connection. Bias current is derived from either the 3.3-V input pin or the 5-V input pin. The TPS2206 also eliminates the APWR_GOOD and BPWR_GOOD pins of the TPS2202 and TPS2202A.

The TPS2206 features a 3.3-V low-voltage mode that allows for 3.3-V switching without the need for 5 V. This facilitates low-power system designs such as sleep mode and pager mode where only 3.3 V is available.

description (continued)

The TPS2206 incorporates a reset function, selectable by one of two inputs, to help alleviate system errors. The reset function enables PC Card initialization concurrent with host platform initialization, allowing a system reset. Reset is accomplished by grounding the V_{CC} and V_{pp} (flash-memory programming voltage) outputs, which discharges residual card voltage.

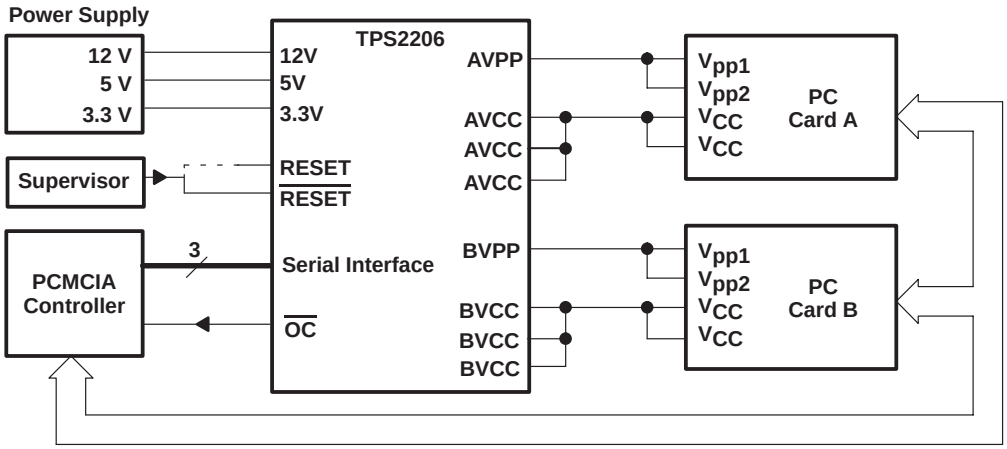
End equipment for the TPS2206 includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras and bar-code scanners.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			CHIP FORM (Y)
	PLASTIC SMALL OUTLINE (DB)	PLASTIC SMALL OUTLINE (DF)	TSSOP (DAP)	
−40°C to 85°C	TPS2206IDB	TPS2206IDFR	TPS2206IDAPR	TPS2206Y

The DB package is available taped and reeled (add an R suffix to the device type, e.g., TPS2206IDBR). The DF and DAP packages are only available taped and reeled, indicated by the R suffix.

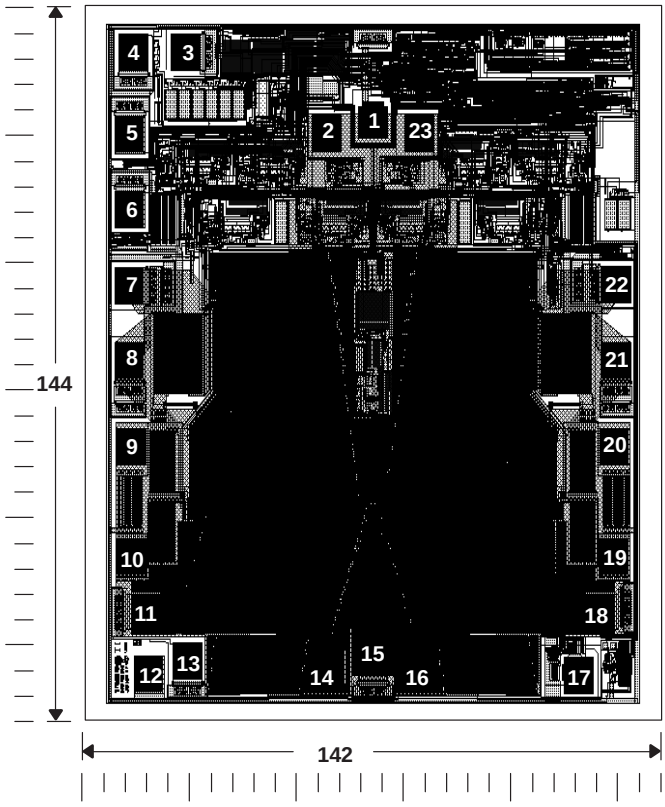
typical PC card power-distribution application

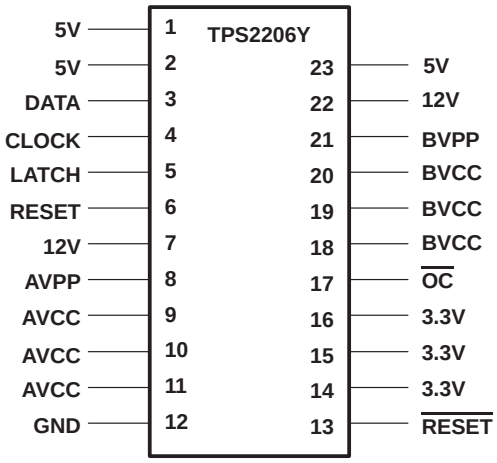


TPS2206Y chip information

This chip, when properly assembled, displays characteristics similar to those of the TPS2206. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	DB, DF	DAP		
3.3V	15, 16, 17	16, 17, 18	I	3.3-V V_{CC} input for card power
5V	1, 2, 30	1, 2, 32	I	5-V V_{CC} input for card power and/or chip power
12V	7, 24	8, 25	I	12-V V_{pp} input for card power
AVCC	9, 10, 11	10, 11, 12	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance to card
AVPP	8	9	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance to card
BVCC	20, 21, 22	21, 22, 23	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance
BVPP	23	24	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance
CLOCK	4	5	I	Logic-level clock for serial data word
DATA	3	4	I	Logic-level serial data word
GND	12	13		Ground
LATCH	5	6	I	Logic-level latch for serial data word
NC	13, 19, 25, 26, 27, 28, 29	3, 19, 26, 27, 28, 29, 30, 31		No internal connection
$\overline{OC}$	18	20	O	Logic-level overcurrent. $\overline{OC}$ reports output that goes low when an overcurrent condition exists
RESET	6	7	I	Logic-level RESET input active high. Do not connect if terminal 14 is used.
$\overline{RESET}$	14	14	I	Logic-level $\overline{RESET}$ input active low. Do not connect if terminal 6 is used.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range for card power: $V_{I(5V)}$ . . . . . −0.3 V to 7 V
$V_{I(3.3V)}$ . . . . . −0.3 V to 7 V
$V_{I(12V)}$ . . . . . −0.3 V to 14 V
Logic input voltage . . . . . −0.3 V to 7 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Output current (each card): $I_{O(xVCC)}$ . . . . . internally limited
$I_{O(xVPP)}$ . . . . . internally limited
Operating virtual junction temperature range, T_J . . . . . −40°C to 150°C
Operating free-air temperature range, T_A . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE		$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB		1024 mW	8.2 mW/°C	655 mW	532 mW
DF		1158 mW	9.26 mW/°C	741 mW	602 mW
DAP	No backplane	1625 mW	13 mW/°C	1040 mW	845 mW
	Backplane§	6044 mW	48.36 mW/°C	3869 mW	3143 mW

‡ These devices are mounted on an FR4 board with no special thermal considerations.
§ 2-oz backplane with 2-oz traces; 5.2-mm × 11-mm thermal pad with 6-mil solder; 0.18-mm diameter vias in a 3×6 array.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage range, V_I	$V_{I(5V)}$	0	5.25	V
	$V_{I(3.3V)}$	0	5.25	V
	$V_{I(12V)}$	0	13.5	V
Output current	$I_{O(xVCC)}$ at 25°C		1	A
	$I_{O(xVPP)}$ at 25°C		150	mA
Clock frequency		0	2.5	MHz
Operating virtual junction temperature, T_J		−40	125	°C

electrical characteristics, T_A = 25°C, $V_{I(5V)}$ = 5 V (unless otherwise noted)

dc characteristics

PARAMETER			TEST CONDITIONS	TPS2206 MIN	TPS2206 TYP	TPS2206 MAX	UNIT
	Switch resistances†	5 V to xVCC			103	140	mΩ
		3.3 V to xVCC	$V_{I(5V)}$ = 5 V, $V_{I(3.3\ V)}$ = 3.3 V		69	110	
		3.3 V to xVCC	$V_{I(5V)}$ = 0, $V_{I(3.3V)}$ = 3.3 V		96	180	
		5 V to xVPP				6	Ω
		3.3 V to xVPP				6	
		12 V to xVPP				1	
$V_{O(xVPP)}$	Clamp low voltage		I_{pp} at 10 mA			0.8	V
$V_{O(xVCC)}$	Clamp low voltage		I_{CC} at 10 mA			0.8	V
I_{lkg}	Leakage current	I_{pp} high-impedance state	T_A = 25°C		1	10	µA
			T_A = 85°C			50	
		I_{CC} high-impedance state	T_A = 25°C		1	10	
			T_A = 85°C			50	
I_I	Input current	$V_{I(5V)}$ = 5 V	$V_{O(AVCC)}$ = $V_{O(BVCC)}$ = 5 V, $V_{O(AVPP)}$ = $V_{O(BVPP)}$ = 12 V		117	150	µA
		$V_{I(5V)}$ = 0, $V_{I(3.3V)}$ = 3.3 V	$V_{O(AVCC)}$ = $V_{O(BVCC)}$ = 3.3 V, $V_{O(AVPP)}$ = $V_{O(BVPP)}$ = 0		131	150	
		Shutdown mode	$V_{O(BVCC)}$ = $V_{O(AVCC)}$ = $V_{O(AVPP)}$ = $V_{O(BVPP)}$ = Hi-Z			1	µA
I_{OS}	Short-circuit output-current limit	$I_{O(xVCC)}$	T_J = 85°C, Output powered up into a short to GND	1		2.2	A
		$I_{O(xVPP)}$		120		400	mA

† Pulse-testing techniques are used to maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

logic section

PARAMETER	TEST CONDITIONS	TPS2206 MIN	TPS2206 MAX	UNIT
Logic input current			1	µA
Logic input high level		2		V
Logic input low level			0.8	V
Logic output high level	$V_{I(5V)}$= 5 V, I_O = 1mA	$V_{I(5V)}$−0.4		V
	$V_{I(5V)}$= 0, $V_{I(3.3V)}$ = 3.3 V, I_O = 1mA,	$V_{I(3.3V)}$−0.4		
Logic output low level	I_O = 1mA		0.4	V

switching characteristics†‡

PARAMETER		TEST CONDITIONS		TPS2206 MIN	TPS2206 TYP	TPS2206 MAX	UNIT
t_r	Output rise time	$V_{O(xVCC)}$			1.2		ms
		$V_{O(xVPP)}$			5		
t_f	Output fall time	$V_{O(xVCC)}$			10		
		$V_{O(xVPP)}$			14		
t_{pd}	Propagation delay (see Figure 1)	LATCH↑ to $V_{O(xVPP)}$	t_{on}		4.4		ms
			t_{off}		18		ms
		LATCH↑ to $V_{O(xVCC)}$ (3.3 V), $V_{I(5V)}$ = 5 V	t_{on}		6.5		ms
			t_{off}		20		ms
		LATCH↑ to $V_{O(xVCC)}$ (5 V)	t_{on}		5.7		ms
			t_{off}		25		ms
		LATCH↑ to $V_{O(xVCC)}$ (3.3 V), $V_{I(5V)}$ = 0	t_{on}		6.6		ms
			t_{off}		21		ms

† Refer to Parameter Measurement Information
‡ Switching Characteristics are with C_L = 150 µF.

electrical characteristics, T_A = 25°C, $V_{I(5V)}$ = 5 V (unless otherwise noted)

dc characteristics

PARAMETER			TEST CONDITIONS	TPS2206Y MIN	TPS2206Y TYP	TPS2206Y MAX	UNIT
	Switch resistances§	5 V to xVCC			103		mΩ
		3.3 V to xVCC	$V_{I(5V)}$ = 5 V, $V_{I(3.3\ V)}$ = 3.3 V		69		
		3.3 V to xVCC	$V_{I(5V)}$ = 0, $V_{I(3.3V)}$ = 3.3 V		96		
		5 V to xVPP			4.74		Ω
		3.3 V to xVPP			4.74		
		12 V to xVPP			0.724		
$V_{O(xVPP)}$	Clamp low voltage		I_{pp} at 10 mA		0.275		V
$V_{O(xVCC)}$	Clamp low voltage		I_{CC} at 10 mA		0.275		V
I_{lkg}	Leakage current	I_{pp} High-impedance state	T_A = 25°C		1		µA
		I_{CC} High-impedance state	T_A = 25°C		1		
I_I	Input current	$V_{I(5V)}$ = 5 V	$V_{O(AVCC)}$ = $V_{O(BVCC)}$ = 5 V, $V_{O(AVPP)}$ = $V_{O(BVPP)}$ = 12 V		117		µA
		$V_{I(5V)}$ = 0, $V_{I(3.3V)}$ = 3.3 V	$V_{O(AVCC)}$ = $V_{O(BVCC)}$ = 3.3 V, $V_{O(AVPP)}$ = $V_{O(BVPP)}$ = 0		131		

§ Pulse-testing techniques are used to maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

switching characteristics†‡

PARAMETER		TEST CONDITIONS		TPS2206Y MIN	TPS2206Y TYP	TPS2206Y MAX	UNIT
t_r	Output rise time	$V_{O(xVCC)}$			1.2		ms
		$V_{O(xVPP)}$			5		
t_f	Output fall time	$V_{O(xVCC)}$			10		
		$V_{O(xVPP)}$			14		
t_{pd}	Propagation delay (see Figure 1)	LATCH↑ to $V_{O(xVPP)}$	t_{on}		4.4		ms
			t_{off}		18		ms
		LATCH↑ to $V_{O(xVCC)}$ (3.3 V), $V_{I(5V)}$ = 5 V	t_{on}		6.5		ms
			t_{off}		20		ms
		LATCH↑ to $V_{O(xVCC)}$ (5 V)	t_{on}		5.7		ms
			t_{off}		25		ms
		LATCH↑ to $V_{O(xVCC)}$ (3.3 V), $V_{I(5V)}$ = 0	t_{on}		6.6		ms
			t_{off}		21		ms

† Refer to Parameter Measurement Information
‡ Switching Characteristics are with C_L = 150 μF.

PARAMETER MEASUREMENT INFORMATION

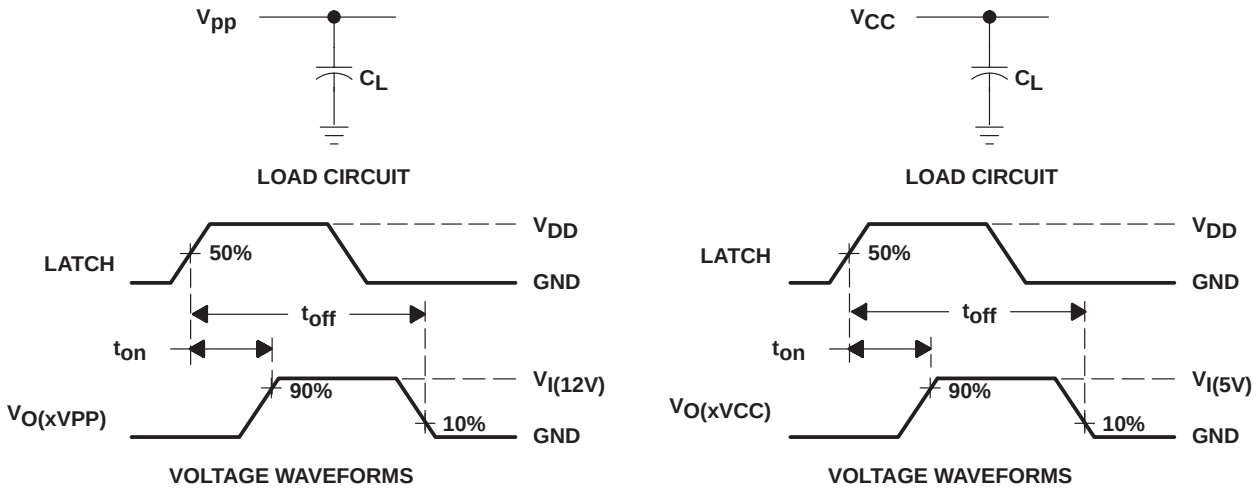
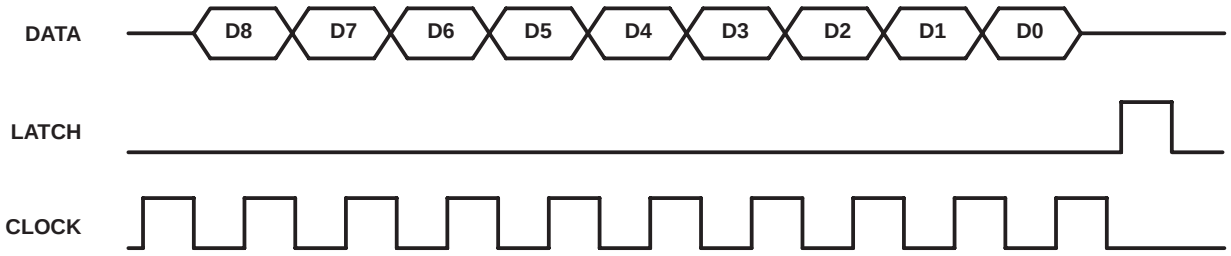


Figure 1. Test Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

Table of Timing Diagrams

	FIGURE
Serial-Interface Timing	2
xVCC Propagation Delay and Rise Time With 1-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 5 V	3
xVCC Propagation Delay and Fall Time With 1-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 5 V	4
xVCC Propagation Delay and Rise Time With 150-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 5 V	5
xVCC Propagation Delay and Fall Time With 150-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 5 V	6
xVCC Propagation Delay and Rise Time With 1-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 0	7
xVCC Propagation Delay and Fall Time With 1-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 0	8
xVCC Propagation Delay and Rise Time With 150-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 0	9
xVCC Propagation Delay and Fall Time With 150-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 0	10
xVCC Propagation Delay and Rise Time With 1-µF Load, 5-V Switch	11
xVCC Propagation Delay and Fall Time With 1-µF Load, 5-V Switch	12
xVCC Propagation Delay and Rise Time With 150-µF Load, 5-V Switch	13
xVCC Propagation Delay and Fall Time With 150-µF Load, 5-V Switch	14
xVPP Propagation Delay and Rise Time With 1-µF Load, 12-V Switch	15
xVPP Propagation Delay and Fall Time With 1-µF Load, 12-V Switch	16
xVPP Propagation Delay and Rise Time With 150-µF Load, 12-V Switch	17
xVPP Propagation Delay and Fall Time With 150-µF Load, 12-V Switch	18



NOTE A: Data is clocked in on the positive leading edge of the clock. The latch should occur before the next positive leading edge of the clock. For definition of D0 to D8, see the control logic table.

Figure 2. Serial-Interface Timing

PARAMETER MEASUREMENT INFORMATION

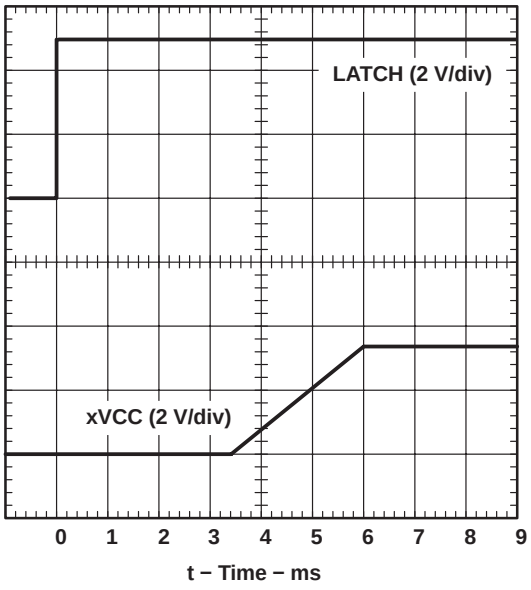


Figure 3. xVCC Propagation Delay and Rise Time With 1-μF Load, 3.3-V Switch, ($V_{I(5V)}$ = 5 V)

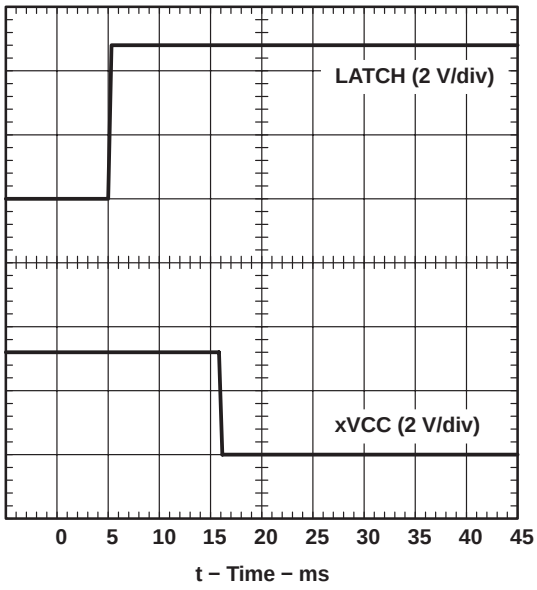


Figure 4. xVCC Propagation Delay and Fall Time With 1-μF Load, 3.3-V Switch, ($V_{I(5V)}$ = 5 V)

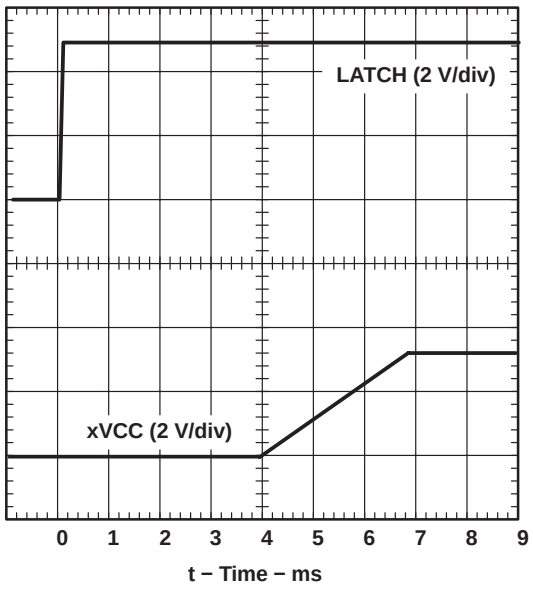


Figure 5. xVCC Propagation Delay and Rise Time With 150-μF Load, 3.3-V Switch, $V_{I(5V)}$ = 5 V

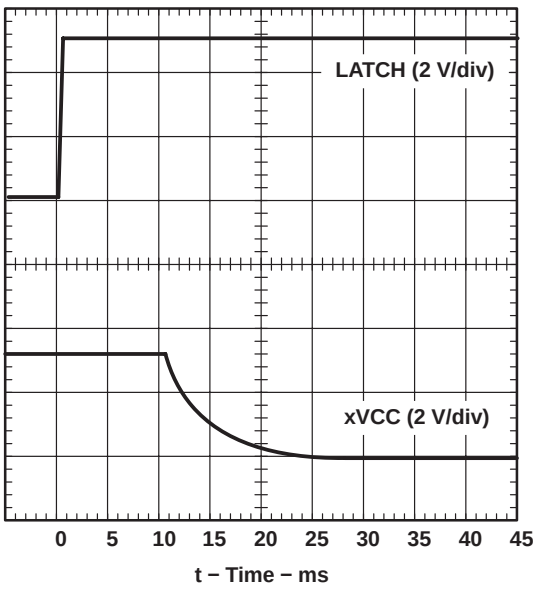


Figure 6. xVCC Propagation Delay and Fall Time With 150-μF Load, 3.3-V Switch, $V_{I(5V)}$ = 5 V

PARAMETER MEASUREMENT INFORMATION

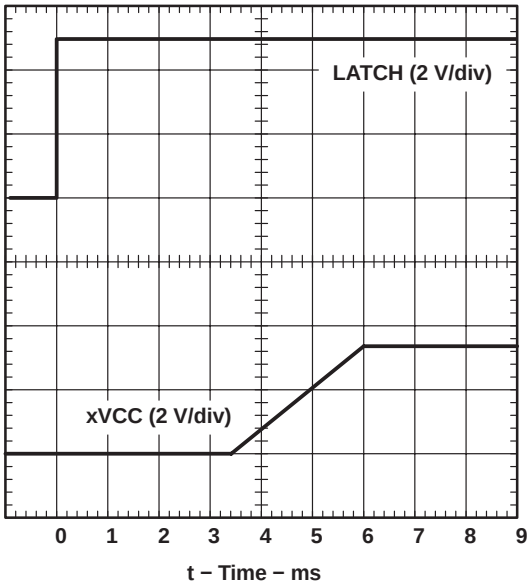


Figure 7. xVCC Propagation Delay and Rise Time With 1-μF Load, 3.3-V Switch, $V_{I(5V)}$ = 0

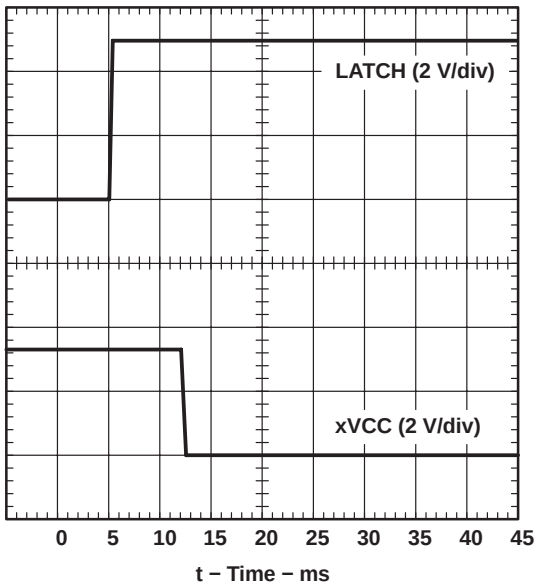


Figure 8. xVCC Propagation Delay and Fall Time With 1-μF Load, 3.3-V Switch, $V_{I(5V)}$ = 0

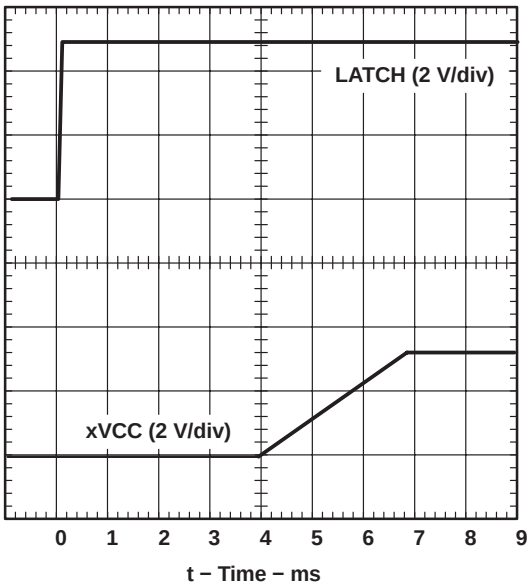


Figure 9. xVCC Propagation Delay and Rise Time With 150-μF Load, 3.3-V Switch, $V_{I(5V)}$ = 0

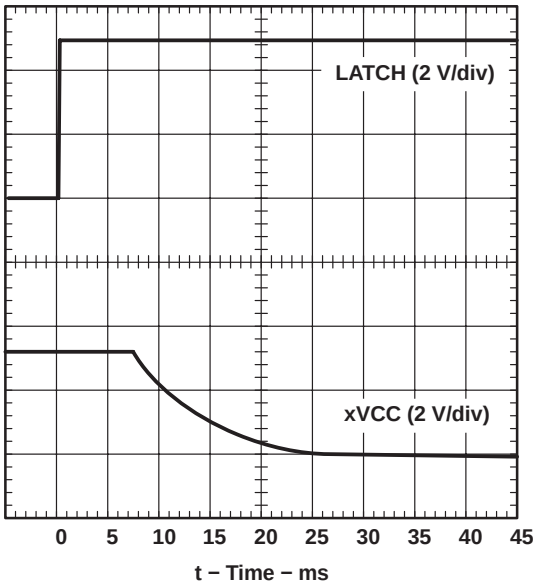


Figure 10. xVCC Propagation Delay and Fall Time With 150-μF Load, 3.3-V Switch, $V_{I(5V)}$ = 0

PARAMETER MEASUREMENT INFORMATION

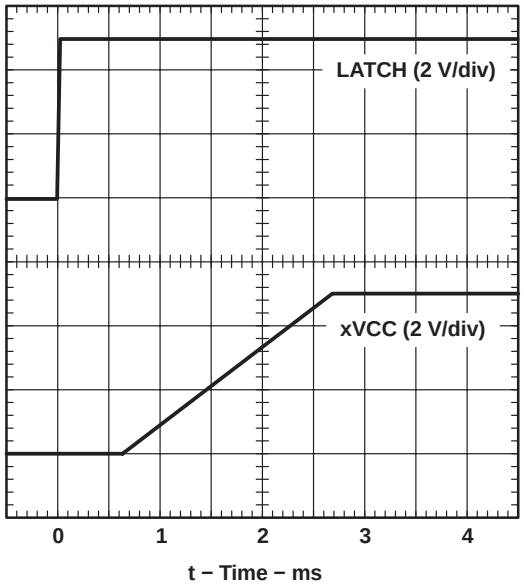


Figure 11. xVCC Propagation Delay and Rise Time With 1-μF Load, 5-V Switch

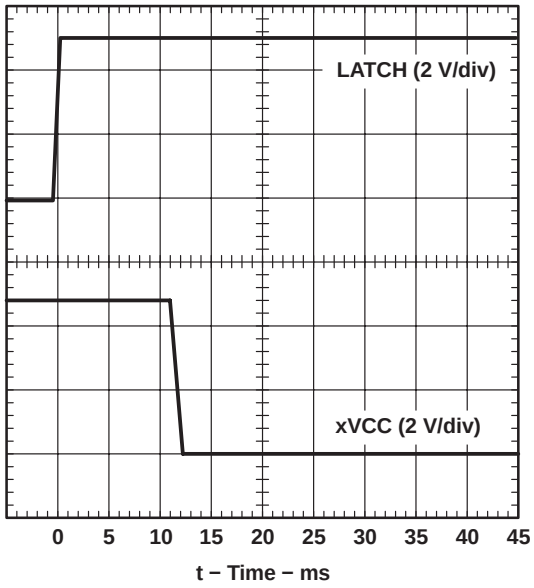


Figure 12. xVCC Propagation Delay and Fall Time With 1-μF Load, 5-V Switch

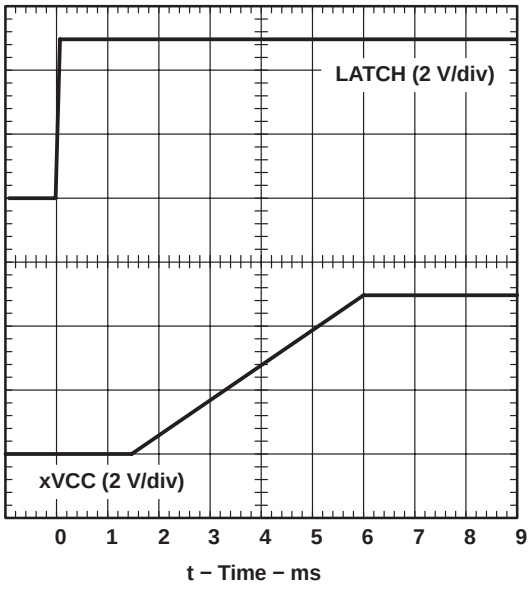


Figure 13. xVCC Propagation Delay and Rise Time With 150-μF Load, 5-V Switch

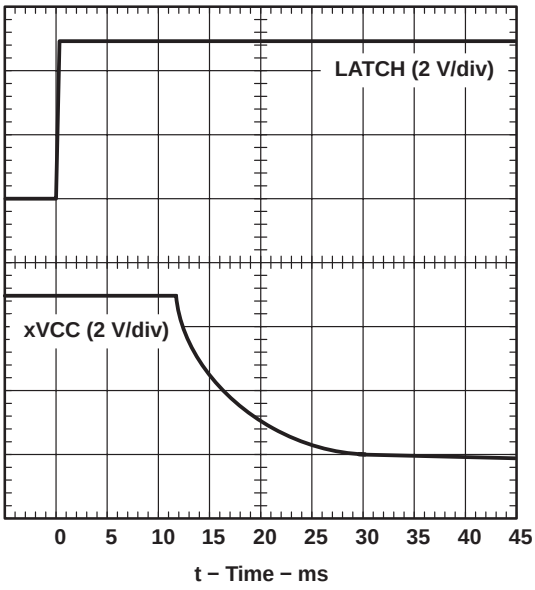


Figure 14. xVCC Propagation Delay and Fall Time With 150-μF Load, 5-V Switch

PARAMETER MEASUREMENT INFORMATION

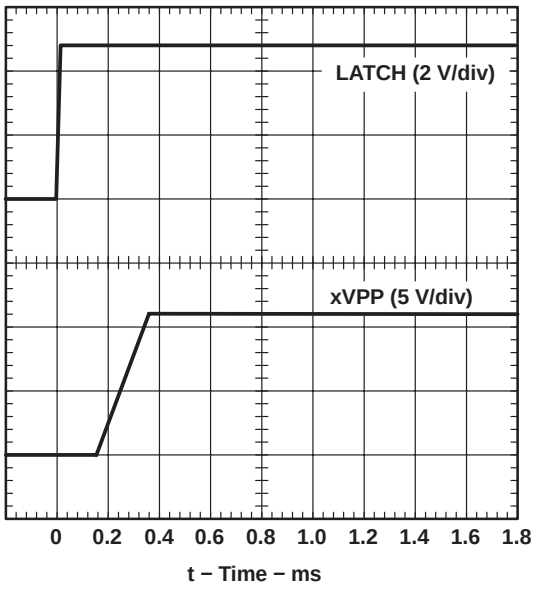


Figure 15. xVPP Propagation Delay and Rise Time With 1-μF Load, 12-V Switch

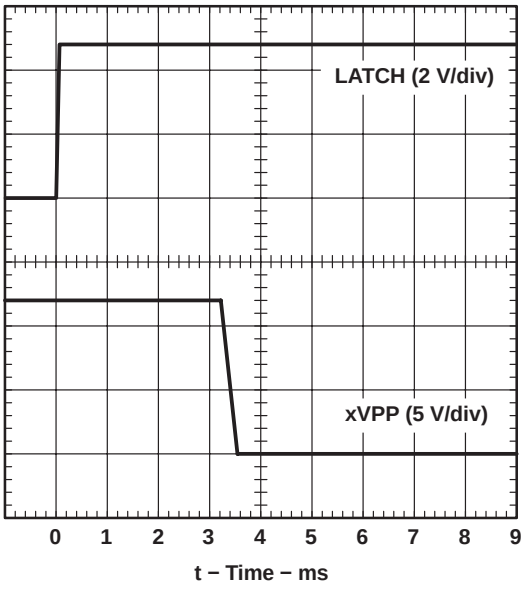


Figure 16. xVPP Propagation Delay and Fall Time With 1-μF Load, 12-V Switch

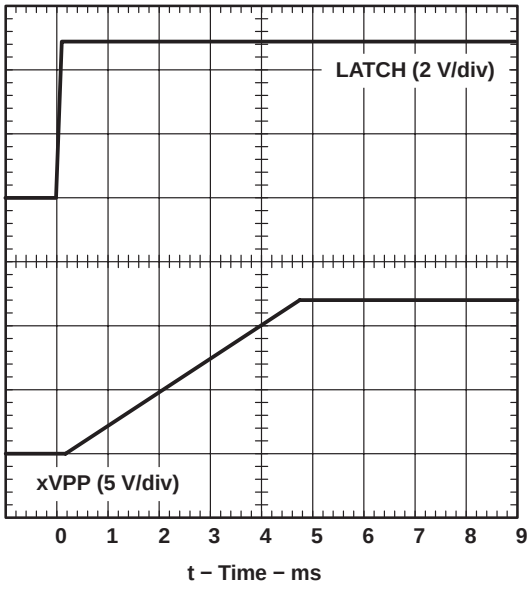


Figure 17. xVPP Propagation Delay and Rise Time With 150-μF Load, 12-V Switch

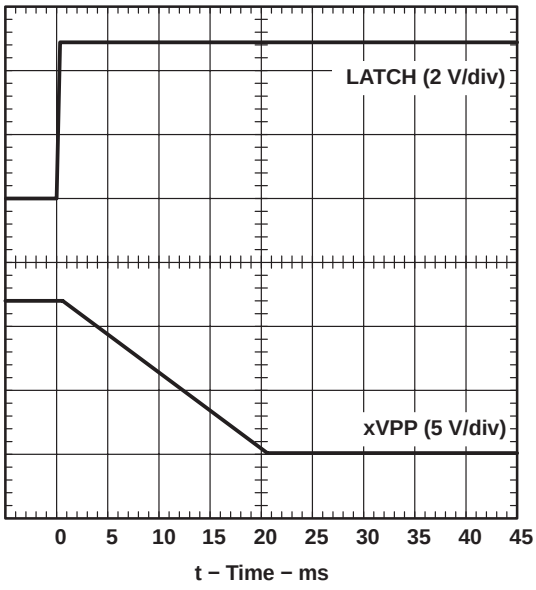


Figure 18. xVPP Propagation Delay and Fall Time With 150-μF Load, 12-V Switch

TYPICAL CHARACTERISTICS

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$V_{O(xVCC)}$	Output voltage, 3.3-V switch, $V_{I(5V)}$ = 5 V	vs Output current	26
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$I_{OS(xVCC)}$	Short-circuit current, 3.3-V switch	vs Junction temperature	30
$I_{OS(xVPP)}$	Short-circuit current, 12-V switch	vs Junction temperature	31

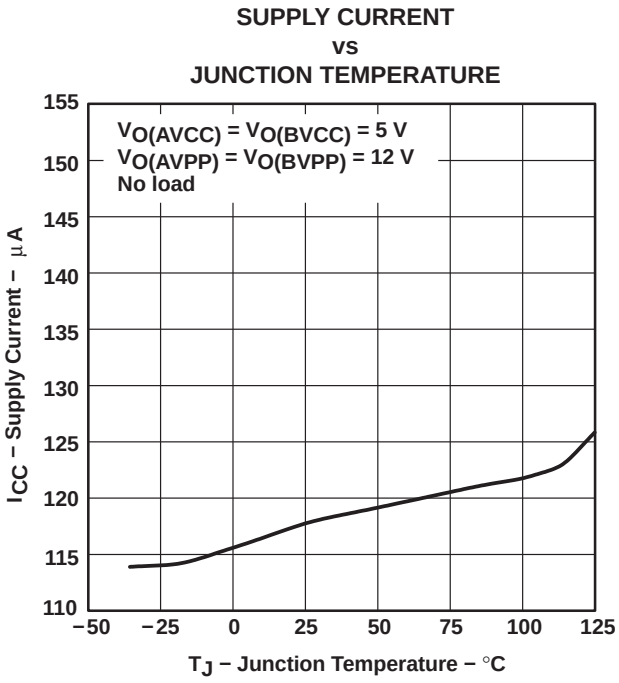


Figure 19

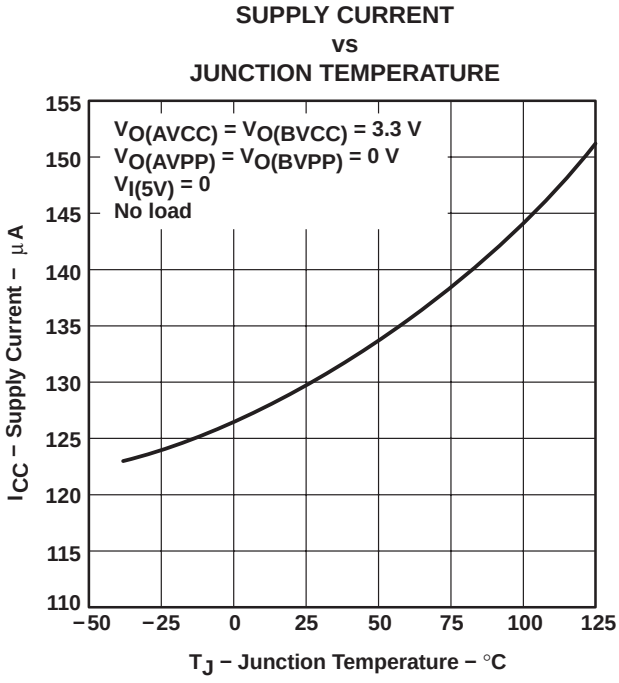


Figure 20

TYPICAL CHARACTERISTICS

3.3-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

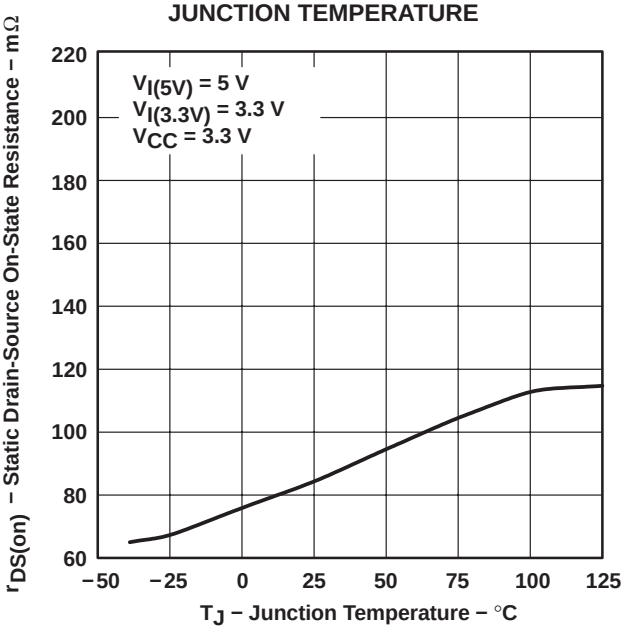


Figure 21

3.3-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

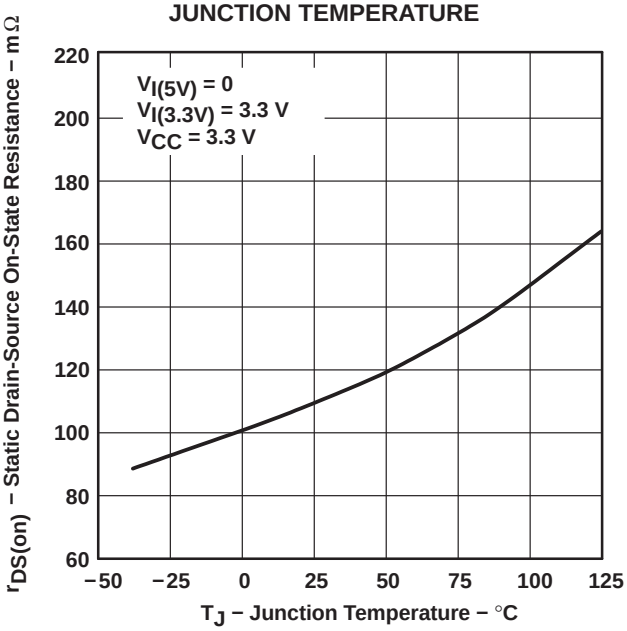


Figure 22

5-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

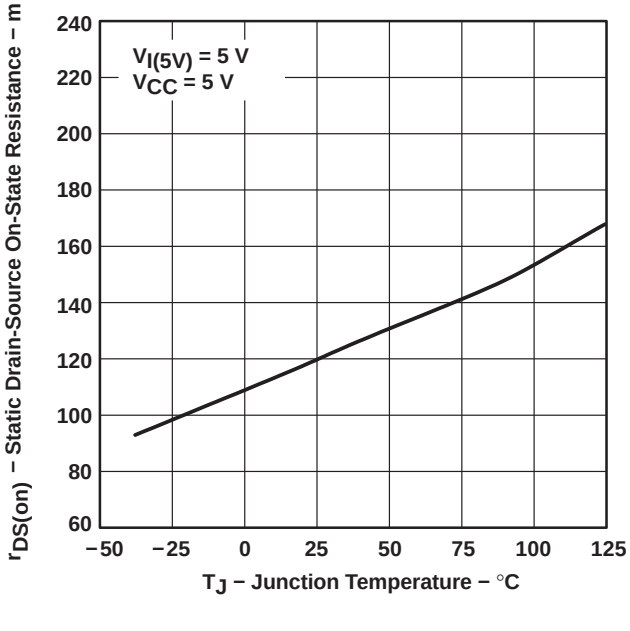


Figure 23

12-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

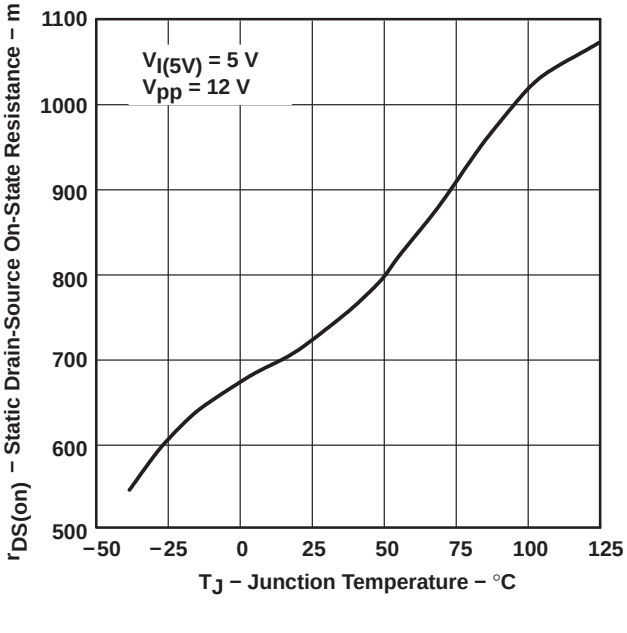


Figure 24

TYPICAL CHARACTERISTICS

5-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

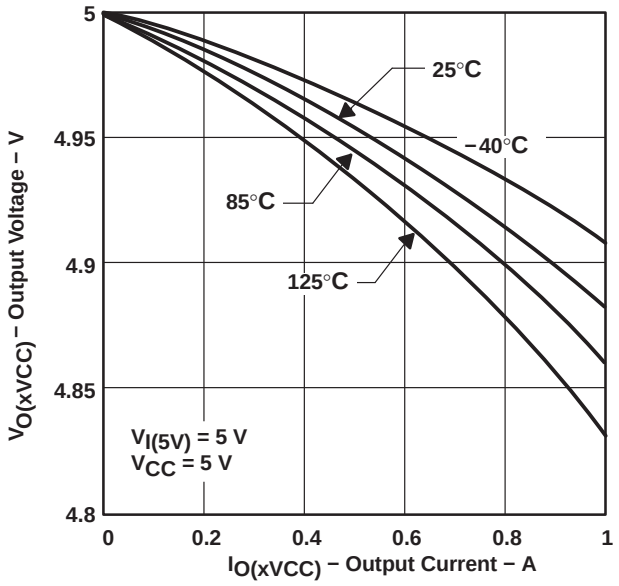


Figure 25

3.3-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

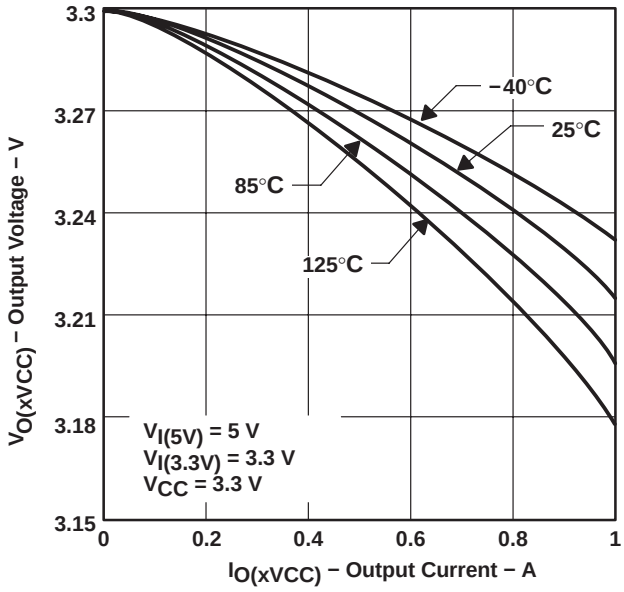


Figure 26

3.3-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

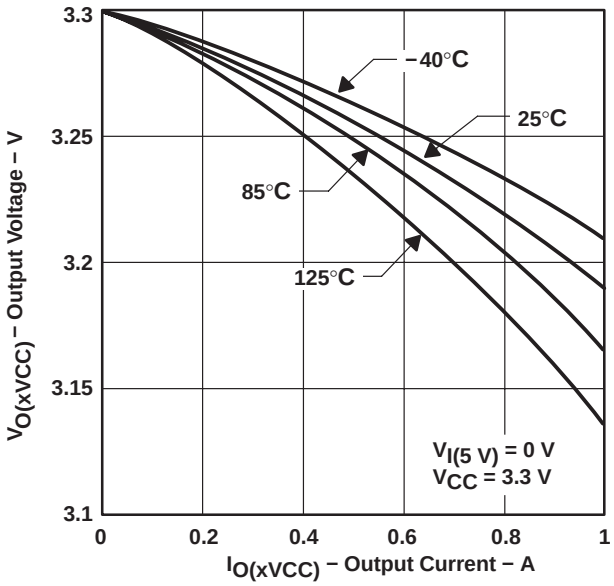


Figure 27

12-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

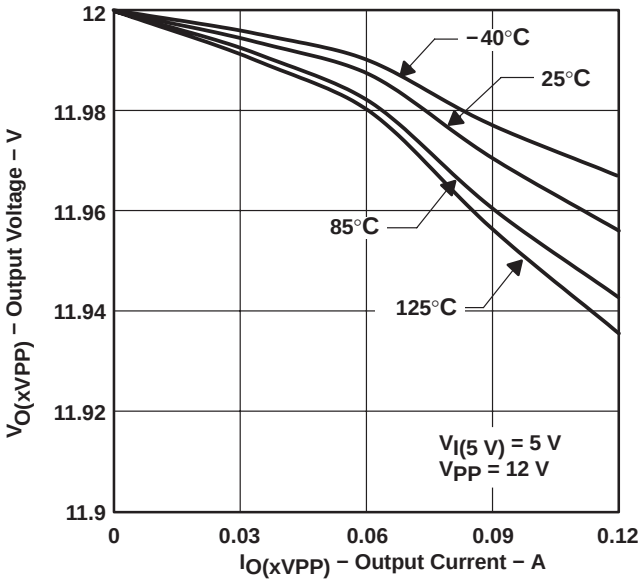


Figure 28

TYPICAL CHARACTERISTICS

5-V SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

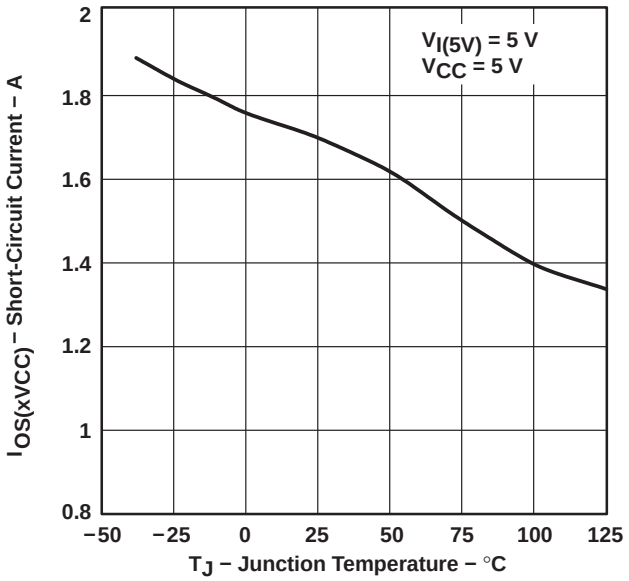


Figure 29

3.3-V SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

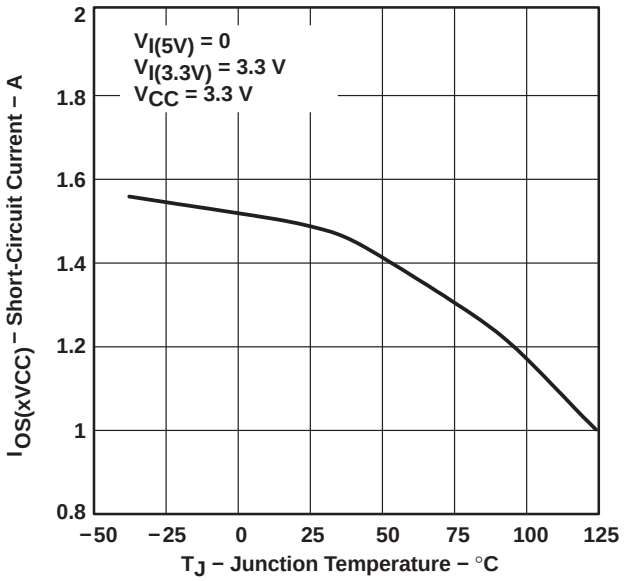


Figure 30

12-V SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

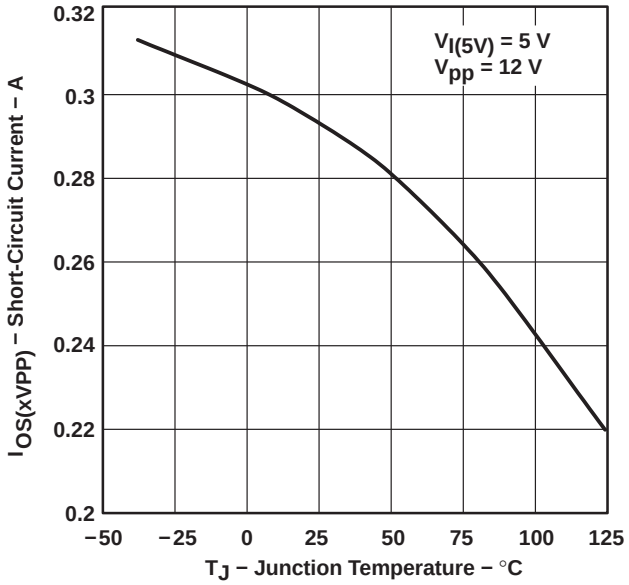


Figure 31

APPLICATION INFORMATION

overview

PC Cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited on-board memory. The idea of add-in cards quickly took hold; modems, wireless LANs, Global Positioning Satellite System (GPS), multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA was established, comprised of members from leading computer, software, PC Card, and semiconductor manufacturers. One key goal was to realize the *plug-and-play* concept. Cards and hosts from different vendors should be compatible—able to communicate with one another transparently.

PC Card power specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the 68 terminals of the PC Card connector. This power interface consists of two V_{CC}, two V_{pp}, and four ground terminals. Multiple V_{CC} and ground terminals minimize connector-terminal and line resistance. The two V_{pp} terminals were originally specified as separate signals but are commonly tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} terminals; flash-memory programming and erase voltage is supplied through the V_{pp} terminals.

designing for voltage regulation

The current PCMCIA specification for output-voltage regulation ($V_{O(reg)}$) of the 5-V output is 5% (250 mV). In a typical PC power-system design, the power supply has an output-voltage regulation ($V_{PS(reg)}$) of 2% (100 mV). Also, a voltage drop from the power supply to the PC Card will result from resistive losses (V_{PCB}) in the PCB traces and the PCMCIA connector. A typical design would limit the total of these resistive losses to less than 1% (50 mV) of the output voltage. Therefore, the allowable voltage drop (V_{DS}) for the TPS2206 would be the PCMCIA voltage regulation less the power supply regulation and less the PCB and connector resistive drops:

$$V_{DS} = V_{O(reg)} - V_{PS(reg)} - V_{PCB} \quad (1)$$

Typically, this would leave 100 mV for the allowable voltage drop across the TPS2206. The voltage drop is the output current multiplied by the switch resistance of the TPS2206. Therefore, the maximum output current that can be delivered to the PC Card in regulation is the allowable voltage drop across the TPS2206 divided by the output switch resistance.

$$I_O max = \frac{V_{DS}}{r_{DS(on)}} \quad (2)$$

The xVCC outputs have been designed to deliver 700 mA at 5 V within regulation over the operating temperature range. Current proposals for the PCMCIA specifications are to limit the power dissipated in the PCMCIA slot to 3 W. With an input voltage of 5 V, 700 mA continuous is the maximum current that can be delivered to the PC Card. The TPS2206 is capable of delivering up to 1 A continuously, but during worst-case conditions the output may not be within regulation. This is generally acceptable because the majority of PC Cards require less than 700 mA continuous. Some cards require higher peak currents (disk drives during initial platter spin-up), but it is generally acceptable for small voltage sags to occur during these peak currents.

The xVCC outputs have been designed to deliver 1 A continuously at 3.3 V within regulation over the operating temperature range. The PCMCIA specification for output voltage regulation of the 3.3-V output is 300 mV. Using the voltage drop percentages (2%) for power supply regulation and PCB resistive loss (1%), the allowable voltage drop for the 3.3 V switch is 200 mV.

The xVPP outputs have been designed to deliver 150 mA continuously at 12 V.

APPLICATION INFORMATION

overcurrent and overtemperature protection

PC Cards are inherently subject to damage that can result from mishandling. Host systems require protection against short-circuited cards that could lead to power supply or PCB-trace damage. Even systems robust enough to withstand a short circuit would still undergo rapid battery discharge into the damaged PC Card, resulting in the rather sudden and unacceptable loss of system power. Most hosts include fuses for protection. However, the reliability of fused systems is poor, as blown fuses require troubleshooting and repair, usually by the manufacturer.

The TPS2206 takes a two-pronged approach to overcurrent protection. First, instead of fuses, sense FETs monitor each of the power outputs. Excessive current generates an error signal that linearly limits the output current, preventing host damage or failure. Sense FETs, unlike sense resistors or polyfuses, have an added advantage in that they do not add to the series resistance of the switch and thus produce no additional voltage losses. Second, when an overcurrent condition is detected, the TPS2206 asserts a signal at $\overline{OC}$ that can be monitored by the microprocessor to initiate diagnostics and/or send the user a warning message. In the event that an overcurrent condition persists, causing the IC to exceed its maximum junction temperature, thermal-protection circuitry activates, shutting down all power outputs until the device cools to within a safe operating region.

12-V supply not required

Most PC Card switches use the externally supplied 12-V V_{pp} power for switch-gate drive and other chip functions, which requires that power be present at all times. The TPS2206 offers considerable power savings by using an internal charge pump to generate the required higher voltages from the 5-V or 3.3-V input; therefore, the external 12-V supply can be disabled except when needed for flash-memory functions, thereby extending battery lifetime. Do not ground the 12-V input if the 12-V input is not used. Additional power savings are realized by the TPS2206 during a software shutdown in which quiescent current drops to a maximum of 1 μA.

backward compatibility and 3.3-V low-voltage mode

The TPS2206 is backward compatible with the TPS2202 AND TPS2202A products, with the following considerations. Pin 25 (V_{DD} on TPS2202/TPS2202A) is a no connect because bias current is derived from either the 3.3-V input pin or the 5-V input pin. Also, the TPS2206 does not have the APWR_GOOD or BPWR_GOOD VPP reporting outputs. These are left as no connects.

The TPS2206 operates in 3.3-V low-voltage mode when 3.3 volts is the only available input voltage ($V_{I(5V)}$=0). This allows host and PC Cards to be operated in low-power 3.3-V-only modes such as sleep modes or pager modes. Note that in this operation mode, the TPS2206 derives its bias current from the 3.3-V input pin and only 3.3 V can be delivered to the PC Card. The 3.3-V switch resistance increases, but the added switch resistance should not be critical, because only a small amount of current is delivered in this mode. If 6% (198 mV) is allowed for the 3.3-V switch voltage drop, a 500-mΩ switch could deliver over 350 mA to the PC Card.

voltage transitioning requirement

PC Cards, like portables, are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2206 is designed to meet all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the capacitors on 3.3-V-compatible cards be discharged to below 0.8 V before applying 3.3-V power. This ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge and functions as a power reset. The TPS2206 offers a selectable V_{CC} and V_{pp} ground state, in accordance with PCMCIA 3.3-V/5-V switching specifications, to fully discharge the card capacitors while switching between V_{CC} voltages.

APPLICATION INFORMATION

output ground switches

Several PCMCIA power-distribution switches on the market do not have an active-grounding FET switch. These devices do not meet the PC Card specification requiring a discharge of V_{CC} within 100 ms. PC Card resistance can not be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes. A method commonly shown to alleviate this problem is to add to the switch output an external 100-kΩ resistor in parallel with the PC Card. Considering that this is the only discharge path to ground, a timing analysis shows that the RC time constant delays the required discharge time to more than 2 seconds. The only way to ensure timing compatibility with PC Card standards is to use a power-distribution switch that has an internal ground switch, like that of the TPS22xx family, or add an external ground FET to each of the output lines with the control logic necessary to select it.

In summary, the TPS2206 is a complete single-chip dual-slot PC Card power interface. It meets all currently defined PCMCIA specifications for power delivery in 5-V, 3.3-V, and mixed systems, and offers a serial control interface. The TPS2206 offers functionality, power savings, overcurrent and thermal protection, and fault reporting in one 30-pin SSOP surface-mount package for maximum value added to new portable designs.

power-supply considerations

The TPS2206 has multiple pins for each of its 3.3-V, 5-V, and 12-V power inputs and for the switched V_{CC} outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is significantly higher than that specified, resulting in increased voltage drops and lost power. Both 12-V inputs must be connected for proper V_{pp} switching; it is recommended that all input and output power pins be paralleled for optimum operation.

Although the TPS2206 is fairly immune to power input fluctuations and noise, it is generally considered good design practice to bypass power supplies typically with a 1-µF electrolytic or tantalum capacitor paralleled by a 0.047-µF to 0.1-µF ceramic capacitor. It is strongly recommended that the switched V_{CC} and V_{pp} outputs be bypassed with a 0.1-µF or larger capacitor; doing so improves the immunity of the TPS2206 to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the TPS2206 and the load. High switching currents can produce large negative-voltage transients, which forward biases substrate diodes, resulting in unpredictable performance. Similary, no pin should be taken below −0.3 V.

RESET or $\overline{\text{RESET}}$ inputs

To ensure that cards are in a known state after power brownouts or system initialization, the PC Cards should be reset at the same time as the host by applying a low impedance to the V_{CC} and V_{pp} terminals. A low-impedance output state allows discharging of residual voltage remaining on PC Card filter capacitance, permitting the system (host and PC Cards) to be powered up concurrently. The RESET or $\overline{\text{RESET}}$ input closes internal switches S1, S4, S7, and S10 with all other switches left open (see TPS2206 control-logic table). The TPS2206 remains in the low-impedance output state until the signal is deasserted and further data is clocked in and latched. RESET or $\overline{\text{RESET}}$ is provided for direct compatibility with systems that use either an active-low or active-high reset voltage supervisor. The unused pin is internally pulled up or down and should be left unconnected.

APPLICATION INFORMATION

overcurrent and thermal protection

The TPS2206 uses sense FETs to check for overcurrent conditions in each of the V_{CC} and V_{pp} outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore, voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. When an overcurrent condition is detected, only the power output affected is limited; all other power outputs continue to function normally. The $\overline{OC}$ indicator, normally a logic high, is a logic low when any overcurrent condition is detected, providing for initiation of system diagnostics and/or sending a warning message to the user.

During power up, the TPS2206 controls the rise time of the V_{CC} and V_{pp} outputs and limits the current into a faulty card or connector. If a short circuit is applied after power is established (e.g., hot insertion of a bad card), current is initially limited only by the impedance between the short and the power supply. In extreme cases, as much as 10 A to 15 A may flow into the short before the current limiting of the TPS2206 engages. If the V_{CC} or V_{pp} outputs are driven below ground, the TPS2206 may latch nondestructively in an off state. Cycling power will reestablish normal operation.

Overcurrent limiting for the V_{CC} outputs is designed to activate, if powered up, into a short in the range of 1 A to 2.2 A, typically at about 1.6 A. The V_{pp} outputs limit from 120 mA to 400 mA, typically around 280 mA. The protection circuitry acts by linearly limiting the current passing through the switch rather than initiating a full shutdown of the supply. Shutdown occurs only during thermal limiting.

Thermal limiting prevents destruction of the IC from overheating if the package power-dissipation ratings are exceeded. Thermal limiting disables all power outputs (both A and B slots) until the device has cooled.

calculating junction temperature

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, T_J, of the die. The junction temperature is dependent on both $r_{DS(on)}$ and the current through the switch. To calculate T_J, first find $r_{DS(on)}$ from Figures 21, 22, 23, and 24 using an initial temperature estimate about 50°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \times I^2 \quad (3)$$

Next, sum the power dissipation and calculate the junction temperature:

$$T_J = \left(\Sigma P_D \times R_{\theta JA}\right) + T_A,\ R_{\theta JA} = 108\ ^\circ C/W \quad (4)$$

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

logic input and outputs

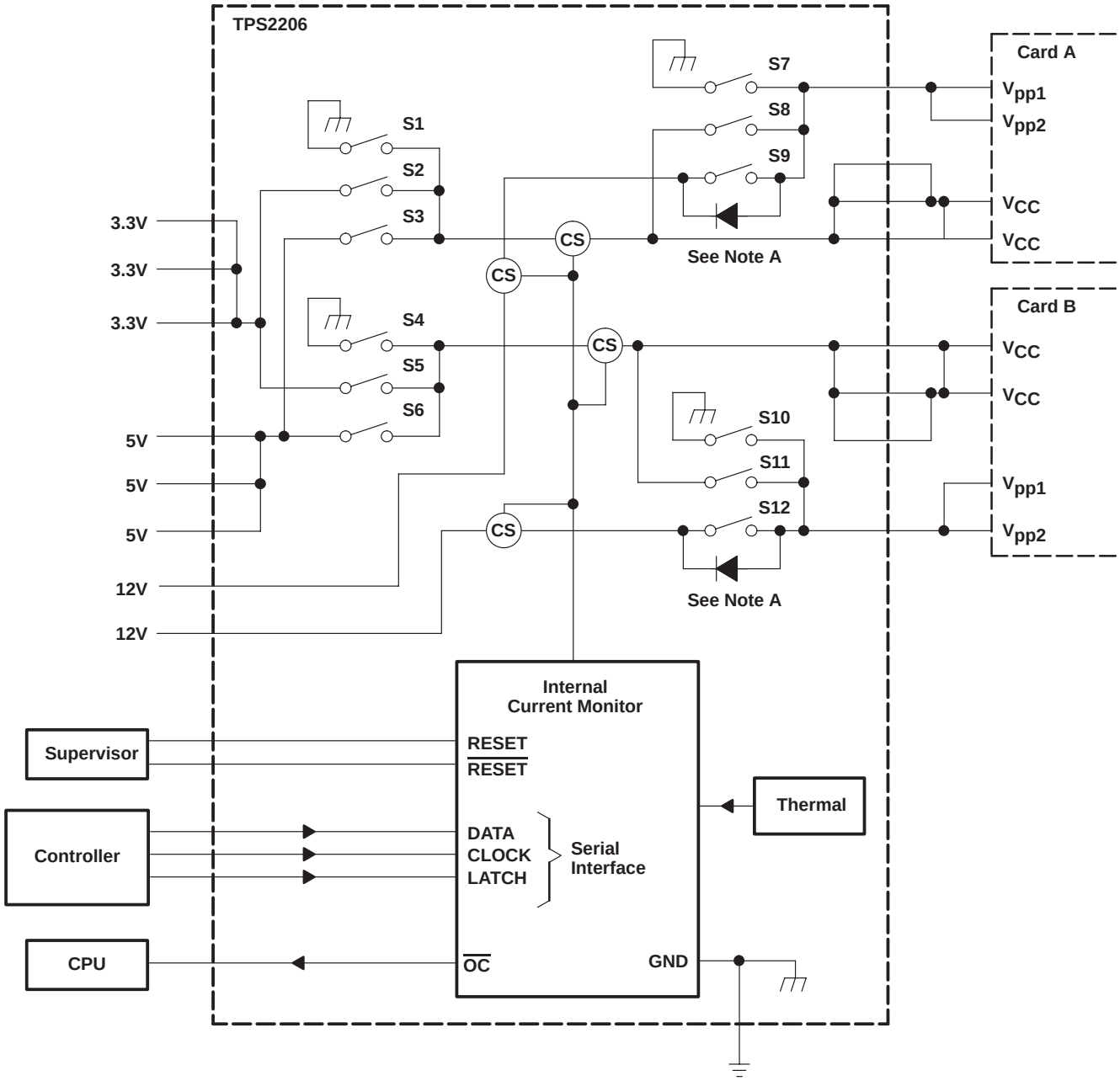
The serial interface consists of DATA, CLOCK, and LATCH leads. The data is clocked in on the positive leading edge of the clock (see Figure 2). The 9-bit (D0 through D8) serial data word is loaded during the positive edge of the latch signal. The latch signal should occur before the next positive leading edge of the clock.

The shutdown bit of the data word places all V_{CC} and V_{pp} outputs in a high-impedance state and reduces chip quiescent current to 1 μA to conserve battery power.

The TPS2206 serial interface is designed to be compatible with serial-interface PCMCIA controllers and current PCMCIA and Japan Electronic Industry Development Association (JEIDA) standards.

An overcurrent output ($\overline{OC}$) is provided to indicate an overcurrent condition in any of the V_{CC} or V_{pp} outputs as previously discussed.

APPLICATION INFORMATION



NOTE A: MOSFET switches S9 and S12 have a back-gate diode from the source to the drain. Unused switch inputs should never be grounded.

Figure 32. Internal Switching Matrix

APPLICATION INFORMATION

TPS2206 control logic

AVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{\text{SHDN}}$	D0 A_VPP_PGM	D1 A_VPP_VCC	S7	S8	S9	VAVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC†
1	1	0	OPEN	OPEN	CLOSED	VPP(12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

BVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{\text{SHDN}}$	D4 B_VPP_PGM	D5 B_VPP_VCC	S10	S11	S12	VBVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC‡
1	1	0	OPEN	OPEN	CLOSED	VPP(12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

AVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{\text{SHDN}}$	D3 $\overline{\text{A\_VCC3}}$	D2 $\overline{\text{A\_VCC5}}$	S1	S2	S3	VAVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3.3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

BVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{\text{SHDN}}$	D6 $\overline{\text{B\_VCC3}}$	D7 $\overline{\text{B\_VCC5}}$	S4	S5	S6	VBVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3.3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

† Output depends on AVCC
‡ Output depends on BVCC

ESD protection

All TPS2206 inputs and outputs incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The V_{CC} and V_{pp} outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1-µF capacitors protects the devices from discharges up to 10 kV.

APPLICATION INFORMATION

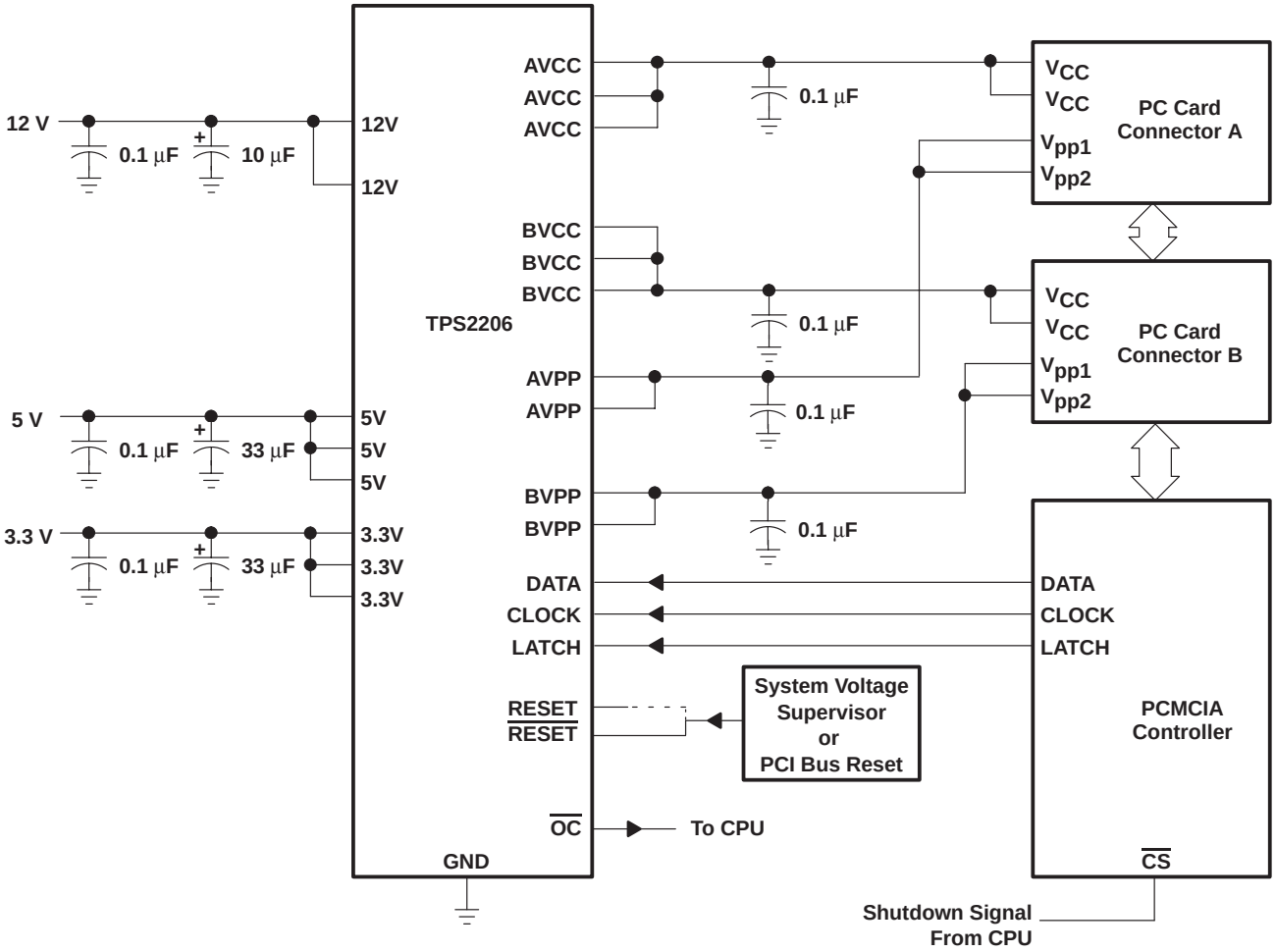


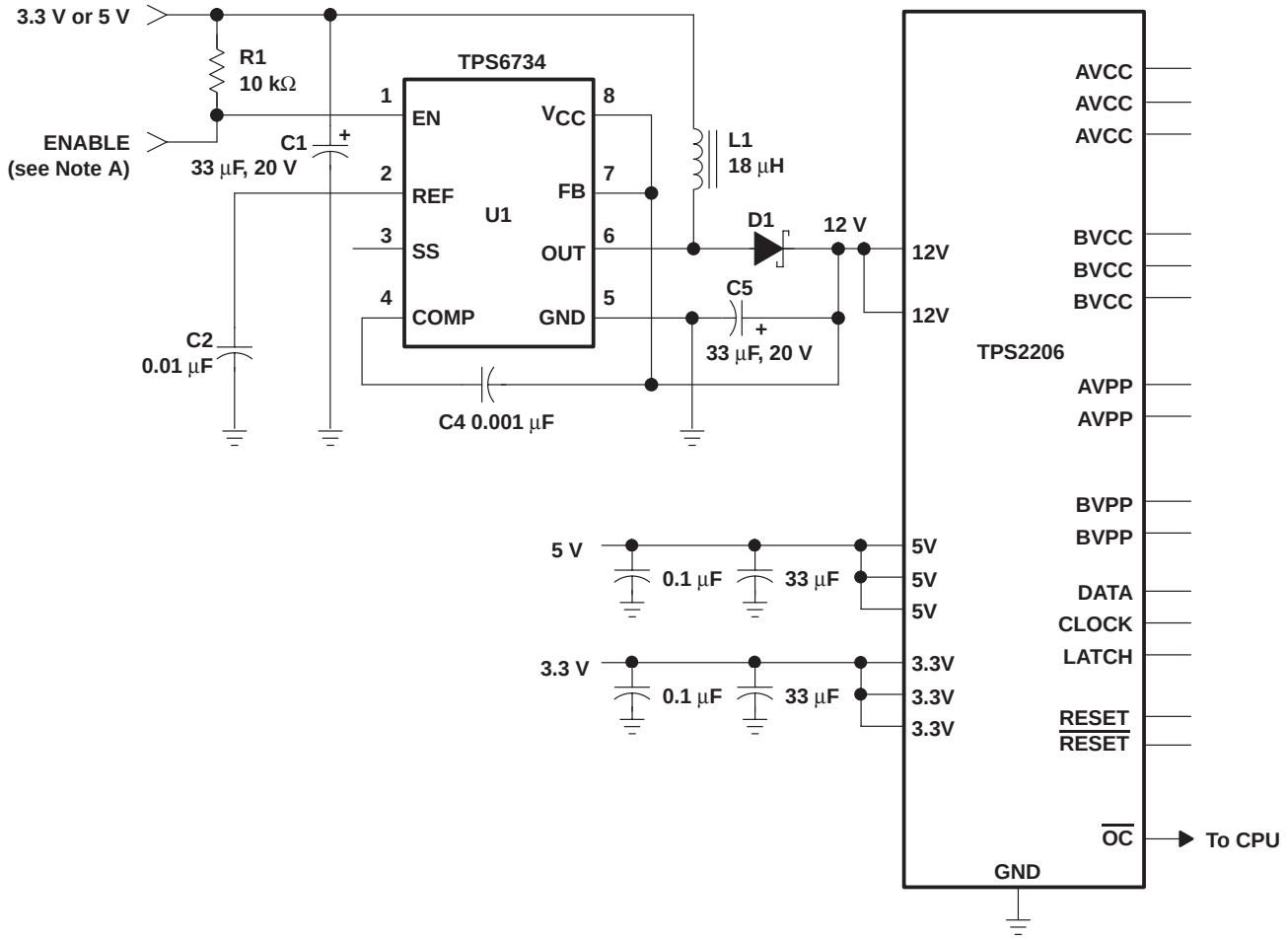
Figure 33. Detailed Interconnections and Capacitor Recommendations

APPLICATION INFORMATION

12-V flash memory supply

The TPS6734 is a fixed 12-V output boost converter capable of delivering 120 mA from inputs as low as 2.7 V. The device is pin-for-pin compatible with the MAX734 regulator and offers the following advantages: lower supply current, wider operating input-voltage range, and higher output currents. As shown in Figure 1, the only external components required are: an inductor, a Schottky rectifier, an output filter capacitor, an input filter capacitor, and a small capacitor for loop compensation. The entire converter occupies less than 0.7 in^2 of PCB space when implemented with surface-mount components. An enable input is provided to shut the converter down and reduce the supply current to 3 μA when 12 V is not needed.

The TPS6734 is a 170-kHz current-mode PWM (pulse-width modulation) controller with an n-channel MOSFET power switch. Gate drive for the switch is derived from the 12-V output after start-up to minimize the die area needed to realize the 0.7-Ω MOSFET and improve efficiency at input voltages below 5 V. Soft start is accomplished with the addition of one small capacitor. A 1.22-V reference (pin 2) is brought out for external use. For additional information, see the TPS6734 data sheet (SLVS127).



NOTE A: The enable terminal can be tied to a generall purpose I/O terminal on the PCMCIA controller or tied high.

Figure 34. TPS2206 with TPS6734 12-V, 120-mA Supply

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2206IDAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS2206I	Samples
TPS2206IDB	ACTIVE	SSOP	DB	30	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2206I	Samples
TPS2206IDBG4	ACTIVE	SSOP	DB	30	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2206I	Samples
TPS2206IDBR	ACTIVE	SSOP	DB	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2206I	Samples
TPS2206IDFR	LIFEBUY	SSOP	DF	30		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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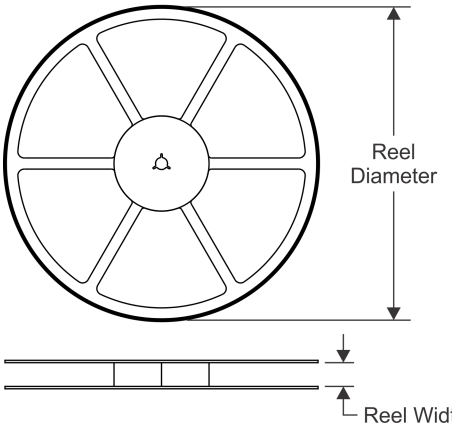
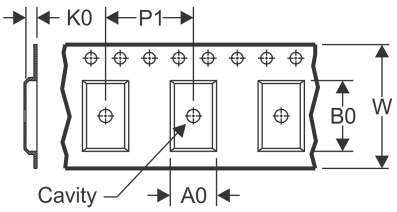
TAPE AND REEL INFORMATION

REEL DIMENSIONS

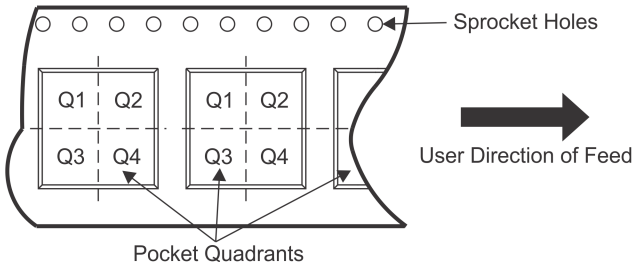


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

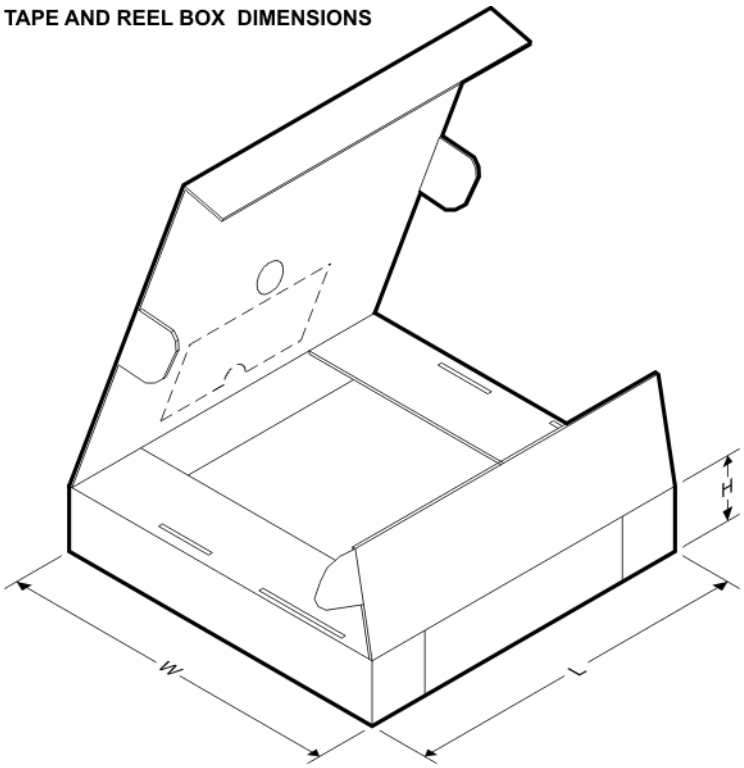
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2206IDAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1
TPS2206IDBR	SSOP	DB	30	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2206IDAPR	HTSSOP	DAP	32	2000	367.0	367.0	45.0
TPS2206IDBR	SSOP	DB	30	2000	367.0	367.0	38.0

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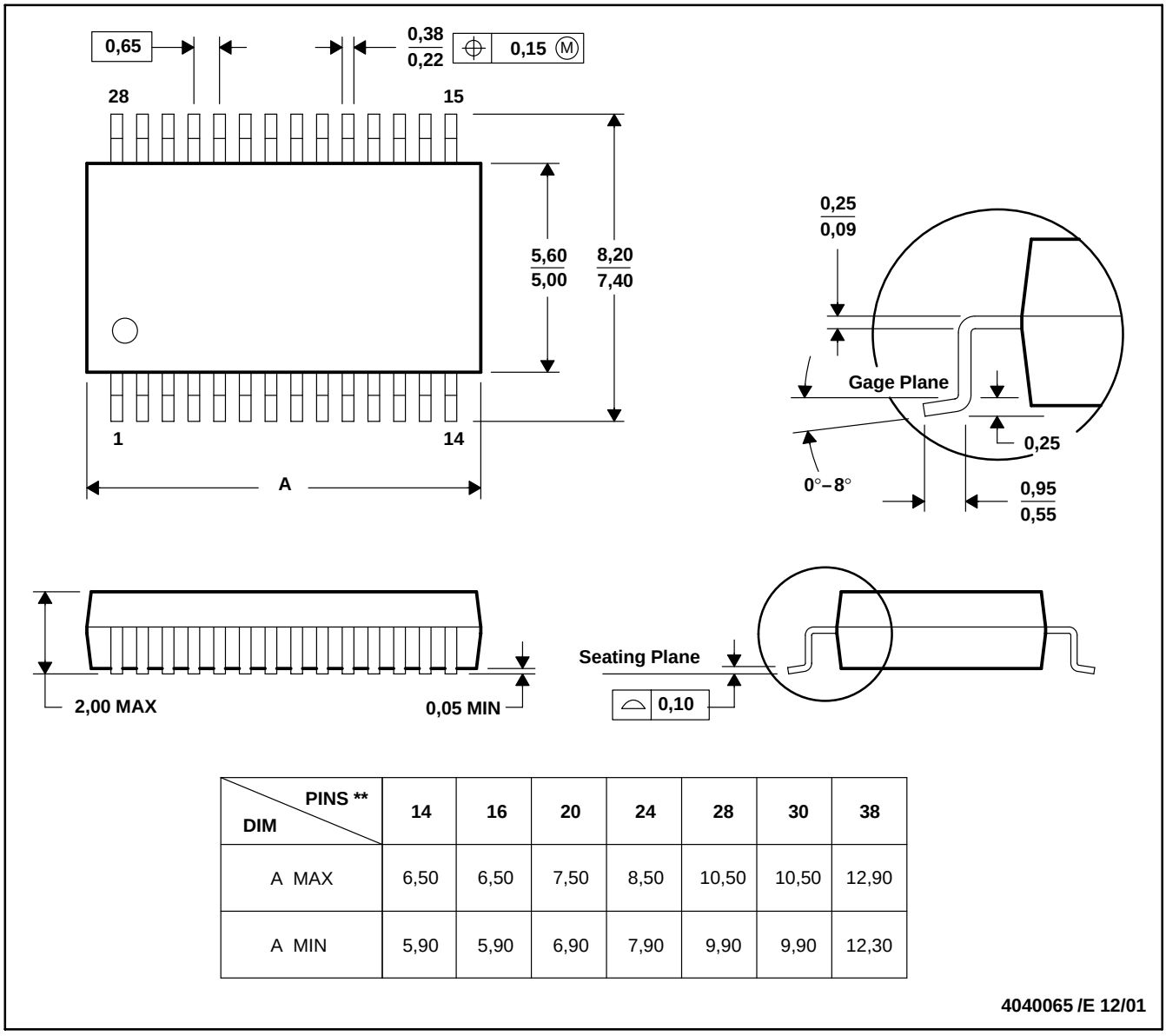
DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

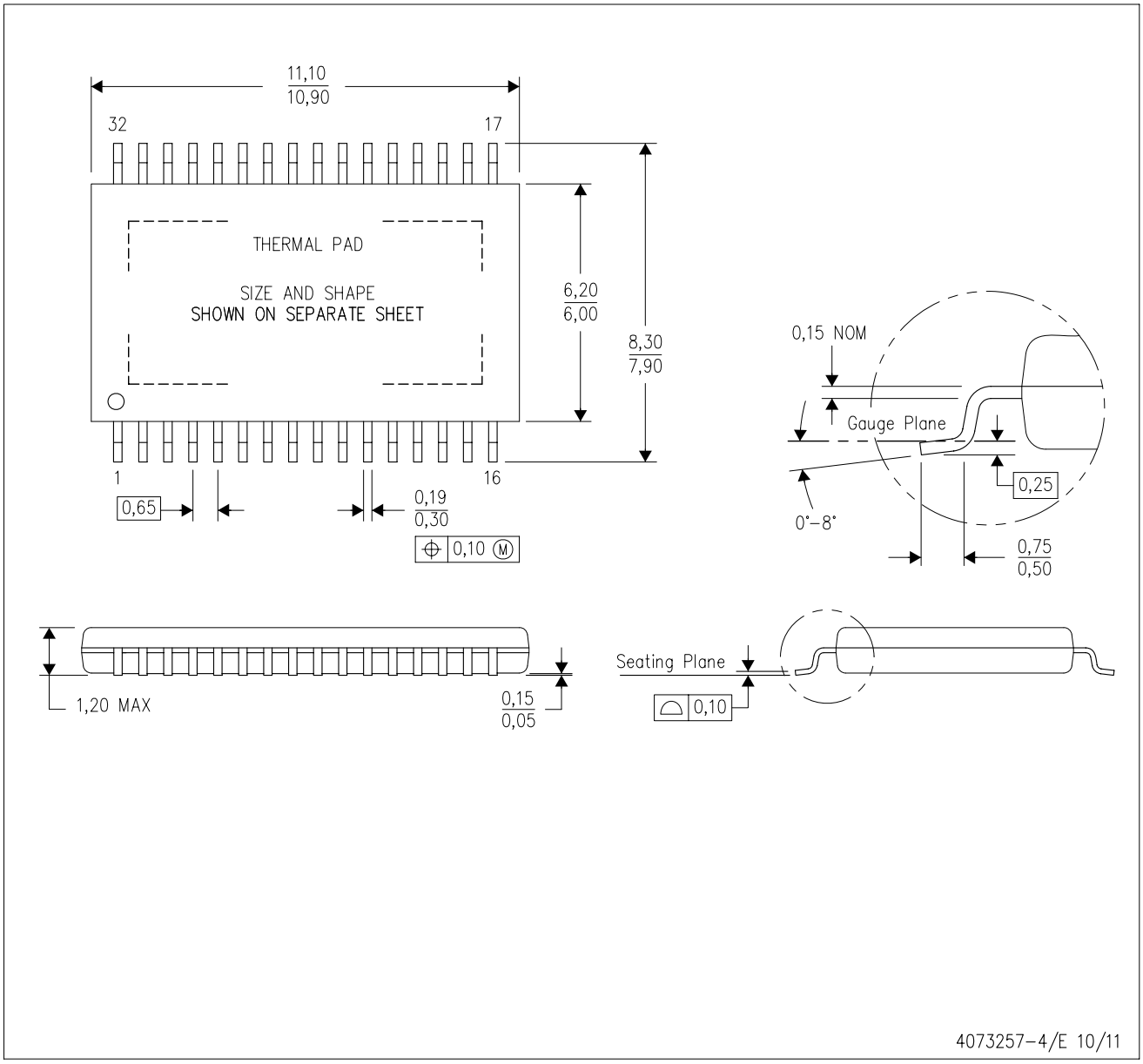


DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

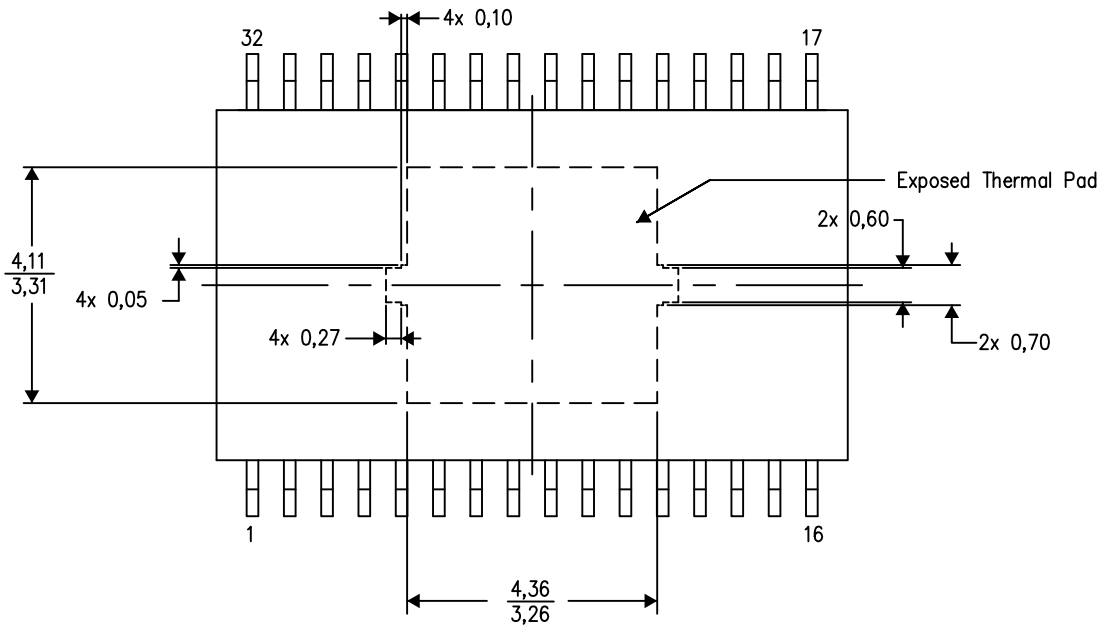
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

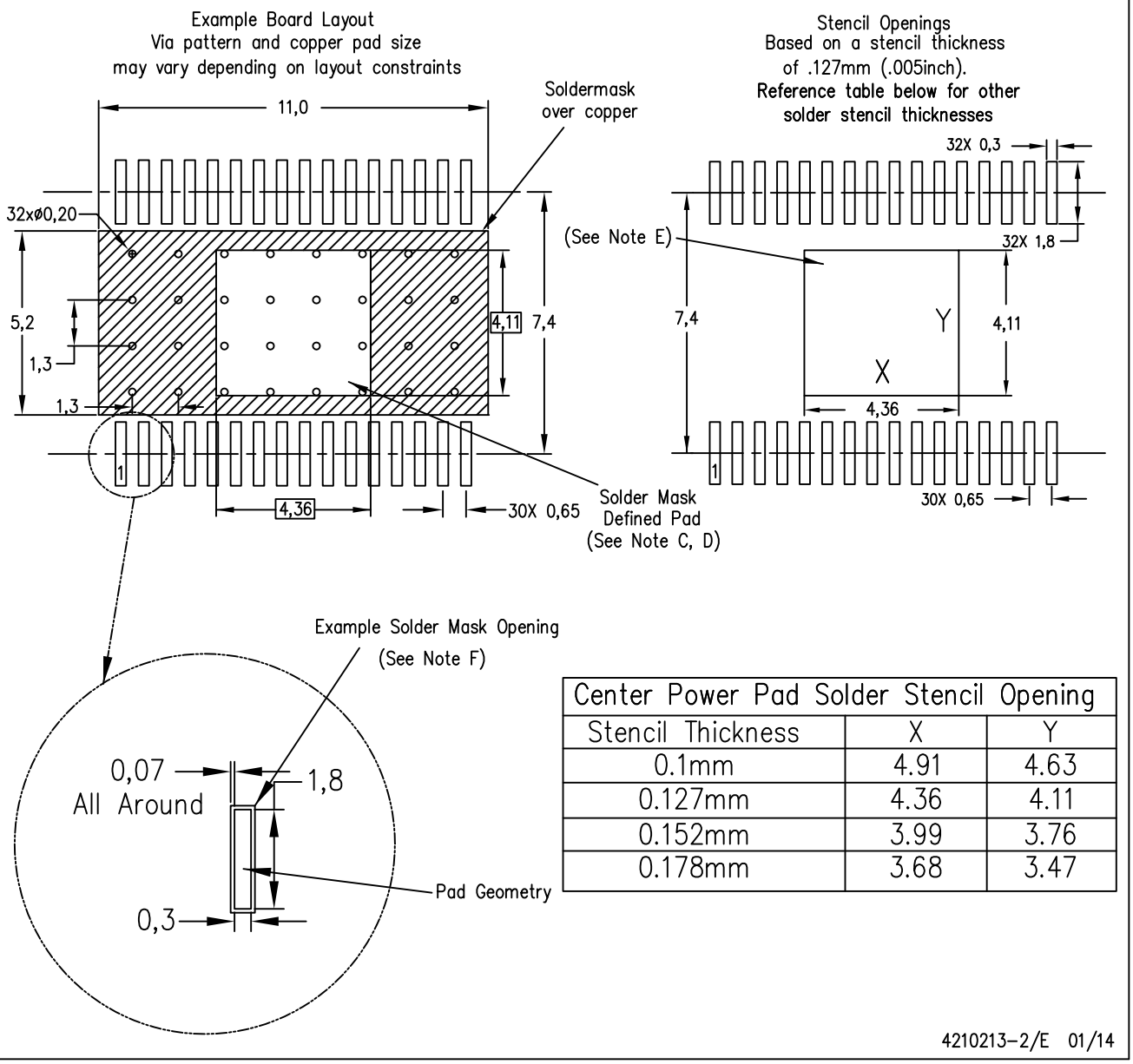
Exposed Thermal Pad Dimensions

4206319–3/M 09/13

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.91	4.63
0.127mm	4.36	4.11
0.152mm	3.99	3.76
0.178mm	3.68	3.47

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
F. Contact the board fabrication site for recommended soldermask tolerances.

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