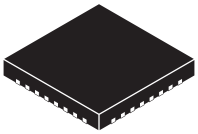


Fixed Frequency, 99% Duty Cycle Peak Current Mode Notebook System Power Controller

FEATURES

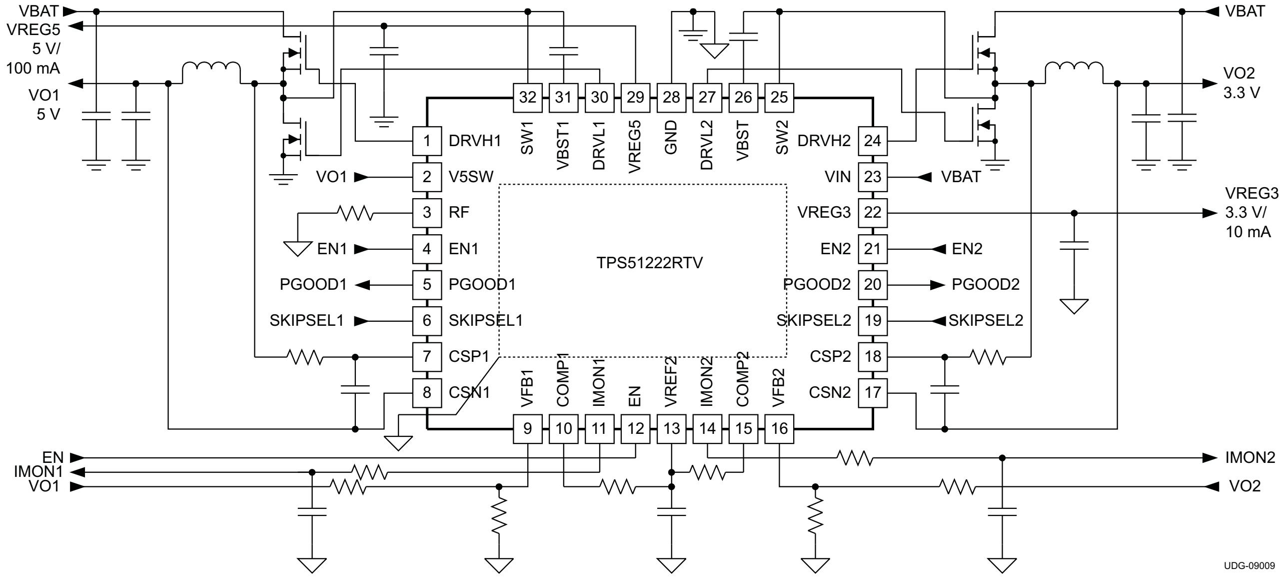
- **Input Voltage Range: 4.5 V to 32 V**
- **Output Voltage Range: 1 V to 12 V**
- **Selectable Light Load Operation (Continuous / Auto Skip / Out-Of-Audio™ Skip)**
- **Programmable Droop Compensation**
- **Voltage Servo Adjustable Soft Start**
- **200-kHz to 1-MHz Fixed-Frequency PWM**
- **Current Mode Architecture**
- **180° Phase Shift Between Channels**
- **Resistor or Inductor DCR Current Sensing**
- **Current Monitor Output for Each Channel**
- **Adaptive Zero Crossing Circuit**
- **Powergood Output for Each Channel**
- **OCL/OVP/UVP/UVLO Protections**
- **Thermal Shutdown (Non-Latch)**
- **Output Discharge Function**
- **Integrated Boot Strap MOSFET Switch**
- **QFN-32 (RTV) Package**

APPLICATIONS

- **Notebook Computer System and I/O Bus**
- **Point of Load in LCD TV, MFP**

DESCRIPTION

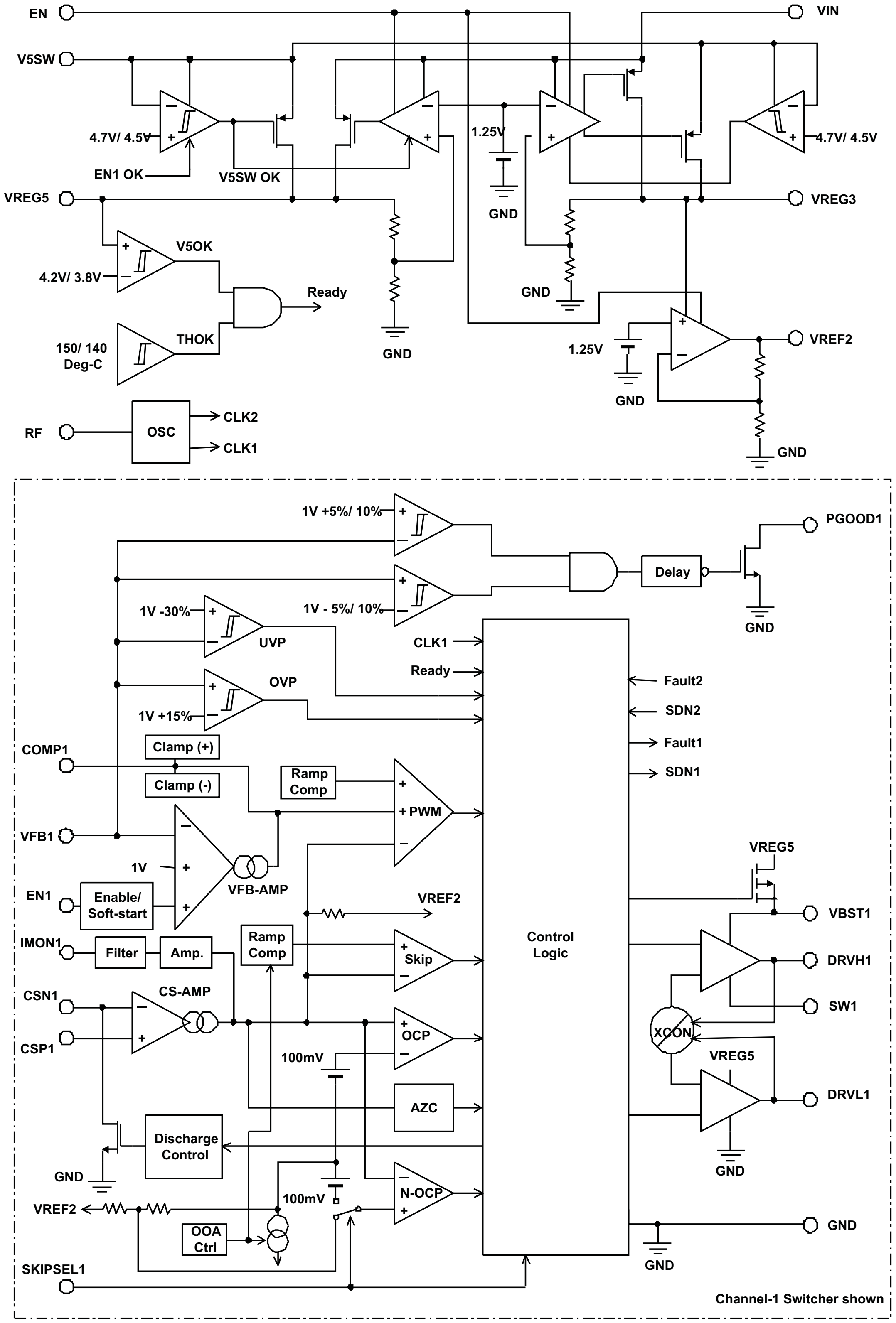
The TPS51222 is a dual synchronous buck regulator controller with two LDOs. It is optimized for 5-V/3.3-V system controller, enabling designers to cost effectively complete 2-cell to 4-cell notebook system power supply. The TPS51222 supports high efficiency, fast transient response, and 99% duty cycle operation. It supports supply input voltage ranging from 4.5 V to 32 V, and output voltages from 1 V to 12 V. Peak current mode supports stability operation with lower ESR capacitor and output accuracy. The high duty cycle (99%) operation and the wide input/output voltage range supports flexible design for small mobile PCs and a wide variety of other applications. The fixed frequency can be adjusted from 200 kHz to 1 MHz by a resistor, and each channel runs 180° out-of-phase. The TPS51222 can also synchronize to the external clock, and the interleaving ratio can be adjusted by its duty. The TPS51222 is available in the 32-pin 5 × 5 QFN package and is specified from –40°C to 85°C.



Out-Of-Audio, PowerPAD are trademarks of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		TPS51222	UNIT
Input voltage range (2)	VIN	–0.3 to 34	V
	VBST1, VBST2	–0.3 to 39	
	VBST1, VBST2(3)	–0.3 to 7	
	SW1, SW2	–5 to 34	
	CSN1, CSN2, CSP1, CSP2	–1 to 13.5	
	EN, EN1, EN2, SKIPSEL1, SKIPSEL2, VFB1, VFB2	–0.3 to 7	
	V5SW	–1 to 7	
	V5SW (to VREG5)(4)	–7 to 7	
Output voltage range(2)	DRVH1, DRVH2	–5 to 39	V
	DRVH1, DRVH2(3)	–0.3 to 7	V
	COMP1, COMP2, DRVL1, DRVL2, IMON1, IMON2, PGOOD1, PGOOD2, RF, VREF2, VREG5	–0.3 to 7	V
	VREG3	–0.3 to 3.6	V
T_J	Junction temperature	150	°C
T_{stg}	Storage temperature	–55 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the corresponding SW terminal.
(4) When EN is high and V5SW is grounded, or voltage is applied to V5SW when EN is low.

DISSIPATION RATINGS (2 oz. Trace and Copper Pad with Solder)

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
32-pin RTV	1.7 W	17 mW/°C	0.7 W

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply voltage	VIN	4.5		32	V
	V5SW	–0.8		6	
I/O voltage	VBST1, VBST2	–0.1		37	V
	DRVH1, DRVH2	–4.0		37	
	DRVH1, DRVH2 (wrt SW1, 2)	–0.1		6	
	SW1, SW2	–4.0		32	
	CSP1, CSP2, CSN1, CSN2	–0.8		13	
	COMP1, COMP2, DRVL1, DRVL2, EN, EN1, EN2, IMON1, IMON2, PGOOD1, PGOOD2, RF, SKIPSEL1, SKIPSEL2, VFB1, VFB2, VREF2, VREG5	–0.1		6	
	VREG3	–0.1		3.5	
T_A	Operating free-air temperature	–40		85	°C

ORDERING INFORMATION

T_A	PACKAGE(1)	ORDERABLE PART NUMBER	TRANSPORT MEDIA	QUANTITY	ECO PLAN
-40°C to 85°C	Plastic Quad Flat Pack (32-Pin QFN)	TPS51222RTVT	Tape and Reel	250	Green (RoHS and no Sb/Br)
		TPS51222RTVR	Tape and Reel	3000	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, EN = 3.3V, VIN = 12V, V5SW = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
$I_{(VINSDN)}$	VIN shutdown current	VIN shutdown current, T_A = 25°C, No Load, EN = 0V, V5SW = 0 V			7	15	µA
$I_{(VINSTBY)}$	VIN Standby Current	VIN standby current, T_A = 25°C, No Load, EN1 = EN2 = V5SW = 0 V			80	120	µA
$I_{(VBATSTBY)}$	Vbat Standby Current	Vbat standby current, T_A = 25°C, No Load SKIPSEL2 = 2V, EN2 = open, EN1 = V5SW = 0V(1)			500		µA
$I_{(V5SW)}$	V5SW Supply Current	V5SW current, T_A = 25°C, No Load, ENx = 5V, VFBx = 1.05 V			0.8		mA
VREF2 OUTPUT							
$V_{(VREF2)}$	VREF2 Output Voltage	$I_{(VREF2)}$ < ±10 µA, T_A = 25°C		1.98	2.00	2.02	V
		$I_{(VREF2)}$ < ±100 µA, 4.5V < VIN < 32 V		1.97	2.00	2.03	
VREG3 OUTPUT							
$V_{(VREG3)}$	VREG3 Output Voltage	V5SW = 0 V, $I_{(VREG3)}$ = 0 mA, T_A = 25°C		3.279	3.313	3.347	V
		V5SW = 0 V, 0 mA < $I_{(VREG3)}$ < 10 mA, 5.5 V < VIN < 32 V		3.135	3.300	3.400	
$I_{(VREG3)}$	VREG3 Output Current	VREG3 = 3 V		10	15	20	mA
VREG5 OUTPUT							
$V_{(VREG5)}$	VREG5 Output Voltage	V5SW = 0 V, $I_{(VREG5)}$ = 0 mA, T_A = 25°C		4.99	5.04	5.09	V
		V5SW = 0 V, 0 mA < $I_{(VREG5)}$ < 100 mA, 6 V < VIN < 32 V		4.90	5.03	5.15	
		V5SW = 0 V, 0 mA < $I_{(VREG5)}$ < 100 mA, 5.5 V < VIN < 32 V		4.50	5.03	5.15	V
$I_{(VREG5)}$	VREG5 Output Current	V5SW = 0 V, VREG5 = 4.5 V		100	150	200	mA
		V5SW = 5 V, VREG5 = 4.5 V		200	300	400	
$V_{(THV5SW)}$	Switchover Threshold	Turning on		4.55	4.7	4.8	V
		Hysteresis		0.15	0.20	0.25	
$t_{d(V5SW)}$	Switchover Delay	Turning on			7.7		ms
$R_{(V5SW)}$	5V SW Ron	$I_{(VREG5)}$ = 100 mA			0.5		Ω
OUTPUT							
$V_{(VFB)}$	VFB Regulation Voltage Tolerance	T_A = 25°C, No Load		0.9925	1.000	1.0075	V
		T_A = –40°C to 85°C , No Load		0.990	1.000	1.010	
$I_{(VFB)}$	VFB Input Current	VFBx = 1.05 V, COMPx = 1.8 V, T_A = 25°C		–50		50	nA
$R_{(Dischg)}$	CSNx Discharge Resistance	ENx = 0 V, CSNx = 0.5 V, T_A = 25°C			20	40	Ω
VOLTAGE TRANSCONDUCTANCE AMPLIFIER							
Gmv	Gain	T_A = 25°C			500		µS
V_{ID}	Differential Input Voltage Range			–30		30	mV
$I_{(COMPSINK)}$	COMP Maximum Sink Current	COMPx = 1.8 V	T_A = 0 to 85°C	27	33		µA
			T_A = –40 to 85°C	22	33		µA
$I_{(COMPSRC)}$	COMP Maximum Source Current	COMPx = 1.8 V			–33	–43	µA
V_{COMP}	COMP Clamp Voltage			2.18	2.22	2.26	V
V_{COMPN}	COMP Negative Clamp Voltage			1.73	1.77	1.81	V

(1) Specified by design. Detail external condition follows application circuit of Figure 52.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, EN = 3.3V, VIN = 12V, V5SW = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT AMPLIFIER							
G_C	Gain	CSNx = 5V, T_A = 25°C (2)			1.667		
V_{IC}	Common mode Input Voltage Range			0		13	V
V_{ID}	Differential Input Voltage Range	T_A = 25°C		–75		75	mV
POWERGOOD							
$V_{(THPG)}$	PG threshold	PG in from lower		92.5%	95%	97.5%	
		PG in from higher		102.5%	105%	107.5%	
		PG hysteresis			5%		
$I_{(PG)}$	PG sink Current	PGOOD = 0.5 V			5		mA
$t_{(PGDLY)}$	PGOOD Delay	Delay for PG in		0.8	1	1.2	ms
SOFTSTART							
$t_{(SSDYL)}$	Soft Start Delay	Delay for Soft Start, ENx = Hi to SS-ramp starts			200		µs
$t_{(SS)}$	Soft Start Time	Internal Soft Start			960		µs
FREQUENCY AND DUTY CONTROL							
$f_{(SW)}$	Switching Frequency	Rf = 330 kΩ		273	303	333	kHz
$V_{(THRF)}$	RF Threshold	Lo to Hi		0.7	1.3	2	V
		Hysteresis			0.2		V
$f_{(SYNC)}$	Sync Input Frequency Range (2)			200		1000	kHz
t_{ONmin}	Minimum On Time	$V_{(DRVH)}$ = 90% to 10%, No Load, CCM/ OOA (2)			120		ns
		$V_{(DRVH)}$ = 90% to 10%, No Load, Auto-skip			160	250	ns
t_{OFFmin}	Minimum Off Time	$V_{(DRVH)}$ = 10% to 90%, No Load			290	400	ns
t_D	Dead time	DRVH-off to DRVL-on		10	30	50	ns
		DRVL-off to DRVH-on		30	40	70	ns
$V_{(DTH)}$	DRVH-off threshold	DRVH to GND (2)			1		V
$V_{(DTL)}$	DRVL-off threshold	DRVL to GND (2)			1		V
CURRENT SENSE							
$V_{(OCL)}$	Current limit threshold	2 V< V_{CSNx} < 12.6 V	T_A = 0 to 85°C	56	60	65	mV
			T_A = –40 to 85°C	55	60	68	
		0.95 V < V_{CSNx} < 12.6 V	T_A = 0 to 85°C	55	60	67	
			T_A = –40 to 85°C	54	60	72	
V_{ZCAJ}	Auto-Zero cross adjustable offset range	0.95 V < V_{CSNx} < 12.6 V, Auto-skip	Positive		5		mV
			Negative		–5		
$V_{(ZC)}$	Zero cross detection comparator Offset	0.95 V < V_{CSNx} < 12.6 V, OOA		–4	0	4	mV
$V_{(OCLN-LV)}$	Negative current limit threshold	0.95 V < V_{CSNx} < 12.6 V	T_A = 0 to 85°C	–50	–60	–73	
			T_A = –40 to 85°C	–49	–60	–77	

(2) Specified by design.

ELECTRICAL CHARACTERISTICS (continued)

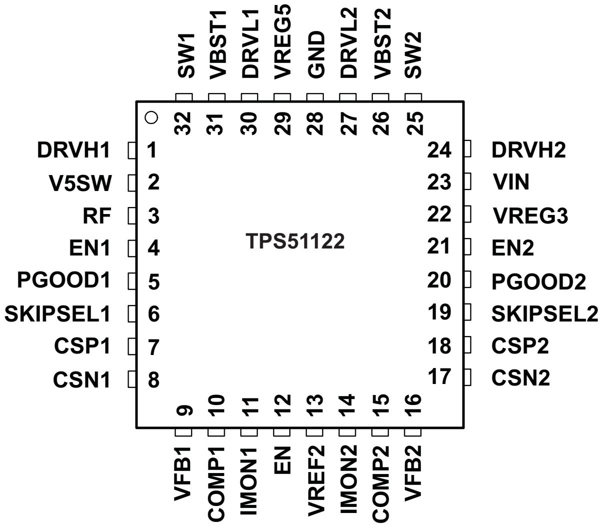
over operating free-air temperature range, EN = 3.3V, VIN = 12V, V5SW = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVERS						
$R_{(DRVH)}$	DRVH resistance	Source, $V_{(VBST-DRVH)}$ = 0.1 V		1.7	5	Ω
		Sink, $V_{(DRVH-SW)}$ = 0.1 V		1	3	
$R_{(DRVL)}$	DRVL resistance	Source, $V_{(VREG5-DRVL)}$ = 0.1 V		1.3	4	Ω
		Sink, $V_{(DRVL-GND)}$ = 0.1 V		0.7	2	
CURRENT MONITOR						
G_{IMON}	Current monitor gain			50		
V_{IMON}	Current monitor output	V_{CSPx}–V_{CSNx} = 60 mV, 0.95 V < V_{CSNx} < 12.6 V, T_A = 25°C	2.75	3.00	3.25	V
$V_{IMON-OFF}$	Current monitor output offset	V_{CSPx}–V_{CSNx} = 0 mV, 0.95 V < V_{CSNx} < 12.6 V, T_A = 25°C	–200		200	mV
UVP, OVP AND UVLO						
$V_{(OVP)}$	OVP Trip Threshold	OVP detect	110%	115%	120%	
$t_{(OVPDLY)}$	OVP Prop Delay			1.5		µs
$V_{(UVP)}$	UVP Trip Threshold	UVP detect	65%	70%	73%	
$t_{(UVPDLY)}$	UVP Delay		0.8	1	1.2	ms
$V_{(UVREF2)}$	VREF2 UVLO Threshold	Wake up	1.7	1.8	1.9	V
		Hysteresis	75	100	125	mV
$V_{(UVREG3)}$	VREG3 UVLO Threshold	Wake up	3	3.1	3.2	V
		Hysteresis	0.10	0.15	0.20	
$V_{(UVREG5)}$	VREG5 UVLO Threshold	Wake up	4.1	4.2	4.3	V
		Hysteresis	0.35	0.40	0.44	V
INTERFACE AND LOGIC THRESHOLD						
$V_{(EN)}$	EN Threshold	Wake up	0.8	1	1.2	V
		Hysteresis	0.1	0.2	0.3	
$V_{(EN12)}$	EN1/EN2 Threshold	Wake up	0.45	0.50	0.55	V
		Hysteresis	0.1	0.2	0.3	
$V_{(EN12SS)}$	EN1/EN2 SS Start Threshold	SS-ramp start threshold at external soft start		1		V
$V_{(EN12SSEND)}$	EN1/EN2 SS End Threshold	SS-End threshold at external soft start (3)		2		V
$I_{(EN12)}$	EN1/EN2 Source Current	VEN1/EN2 = 0V	1.6	2	2.4	µA
$V_{(SKIPSEL)}$	SKIPSEL1/SKIPSEL2 Setting Voltage	Continuous			1.5	V
		Auto Skip	1.9		2.1	
		OOA Skip (min 1/8 Fsw)	3.2		3.4	
		OOA Skip (min 1/16 Fsw)	3.8			
$I_{(SKIPSEL)}$	SKIPSEL Input Current	SKIPSELx = 0 V	–0.5		0.5	µA
		SKIPSELx = 5 V	–0.5		0.5	
BOOT STRAP SW						
$V_{(FBST)}$	Forward Voltage	$V_{VREG5-VBST}$, I_F = 10 mA, T_A = 25°C		0.10	0.20	V
$I_{(BSTLK)}$	VBST Leakage Current	V_{VBST} = 37 V, V_{SW} = 32 V		0.01	1.5	µA
THERMAL SHUTDOWN						
$T_{(SDN)}$	Thermal SDN Threshold	Shutdown temperature(3)		150		°C
		Hysteresis(3)		10		

(3) Specified by design.

DEVICE INFORMATION

PINOUT



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP1	10	I	Loop compensation pin for current mode (error amplifier output). Connect R (and C if required) from this pin to VREF2 for proper loop compensation with current mode operation.
COMP2	15		
CSN1	8	I	Current sense comparator inputs (–). See the current sensing scheme section. Used as power supply for the current sense circuit for 5 V or higher output voltage setting. Also, used for output discharge terminal.
CSN2	17		
CSP1	7	I/O	Current sense comparator inputs (+). An RC network with high quality X5R or X7R ceramic capacitor should be used to extract voltage drop across DCR. 0.1-µF is a good value to start the design. See the current sensing scheme section for more details.
CSP2	18		
DRVH1	1	O	High-side MOSFET gate driver outputs. Source 1.7 Ω, sink 1.0 Ω, SW-node referenced floating driver. Drive voltage corresponds to VBST to SW voltage.
DRVH2	24		
DRVL1	30	O	Low-side MOSFET gate driver outputs. Source 1.3 Ω, sink 0.7 Ω, and GND referenced driver.
DRVL2	27		
EN	12	I	VREF2 and VREG5 linear regulators enable pin. When turning on, apply greater than 1.2 V and less than 6 V. Connect to GND to disable.
EN1	4	I	Channel 1 and channel 2 SMPS Enable Pins. When turning on, apply greater than 0.55 V and less than 6 V. Connect to GND to disable. Adjustable soft-start capacitance to be attached here.
EN2	21		
GND	28	–	Ground
IMON1	11	O	Current monitor outputs for channel 1 and channel 2. Adding an RC filter is recommended.
IMON2	14		
PGOOD1	5	O	Powergood window comparator outputs for channel 1 and channel 2. The recommended applied voltage should be less than 6 V, and the recommended pull-up resistance value is from 100 kΩ to 1 MΩ.
PGOOD2	20		
RF	3	I/O	Frequency setting pin. Connect a frequency setting resistor to (signal) GND. Connect to an external clock for synchronization.

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SKIPSEL1	6	I	Skip mode selection pin. GND: Continuous conduction mode VREF2: Auto Skip VREG3: OOA Auto Skip, maximum 7 skips (suitable for f_{sw} < 400kHz) VREG5: OOA Auto Skip, maximum 15 skips (suitable for equal to or greater than 400kHz)
SKIPSEL2	19		
SW2	25	I/O	High-side MOSFET gate driver returns.
SW1	32		
V5SW	2	I	VREG5 switchover power supply input pin. When EN1 is high, PGOOD1 indicates GOOD and V5SW voltage is higher than 4.8 V, switch-over function is enabled. Note: When switch-over is enabled, VREG5 output voltage is approximately equal to the V5SW input voltage.
VBST1	31	I	Supply inputs for high-side N-channel FET driver (boot strap terminal). Connect a capacitor (0.1-µF or greater is recommended) from this pin to respective SW terminal. Additional SB diode from VREG5 to this pin is an optional.
VBST2	26		
VFB1	9	I	SMPS voltage feedback Inputs. Connect the feedback resistors divider, and should be referred to (signal) GND.
VFB2	16		
VIN	23	I	Supply input for 5-V and 3.3-V linear regulator. Typically connected to VBAT.
VREF2	13	O	2-V reference output. Bypass to (signal) GND with 0.22-µF of ceramic capacitance.
VREG3	22	O	Always alive 3.3 V, 10 mA low dropout linear regulator output. Bypass to (signal) GND with more than 1-µF ceramic capacitance. Runs from VIN supply or from VREG5 when it is switched over to V5SW input.
VREG5	29	O	5-V, 100-mA low dropout linear regulator output. Bypass to (power) GND using a 10-µF ceramic capacitor. Runs from VIN supply. Internally connected to VBST and DRVL. Shuts off with EN. Switches over to V5SW when 4.8 V or above is provided. Note: When switch-over (see above V5SW) is enabled, VREG5 output voltage is approximately equal to V5SW input voltage.

TYPICAL CHARACTERISTICS

INPUT VOLTAGE SHUTDOWN CURRENT vs INPUT VOLTAGE

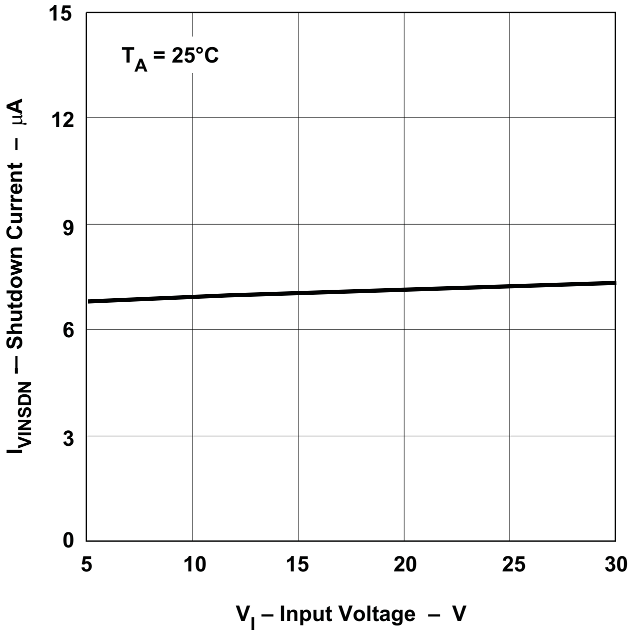


Figure 1.

INPUT VOLTAGE SHUTDOWN CURRENT vs JUNCTION TEMPERATURE

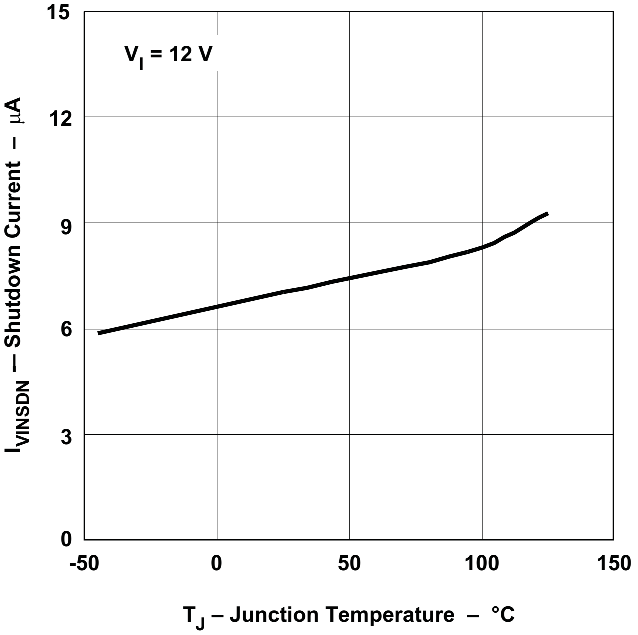


Figure 2.

INPUT VOLTAGE STANDBY CURRENT vs JUNCTION TEMPERATURE

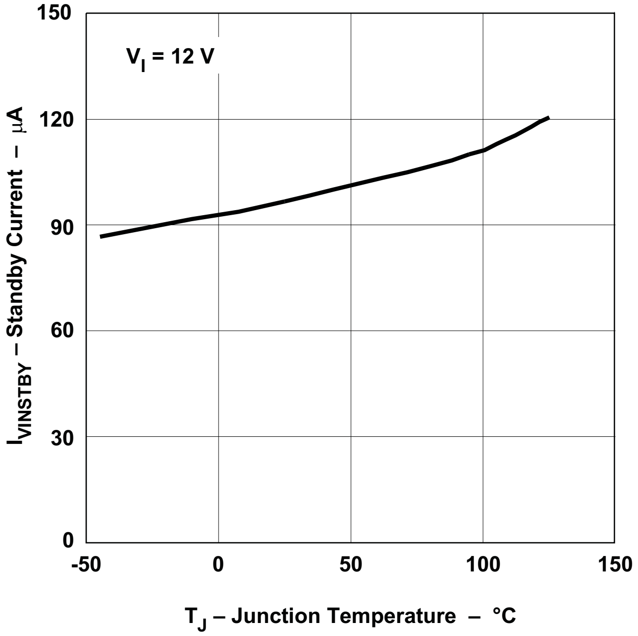


Figure 3.

INPUT VOLTAGE STANDBY CURRENT vs INPUT VOLTAGE

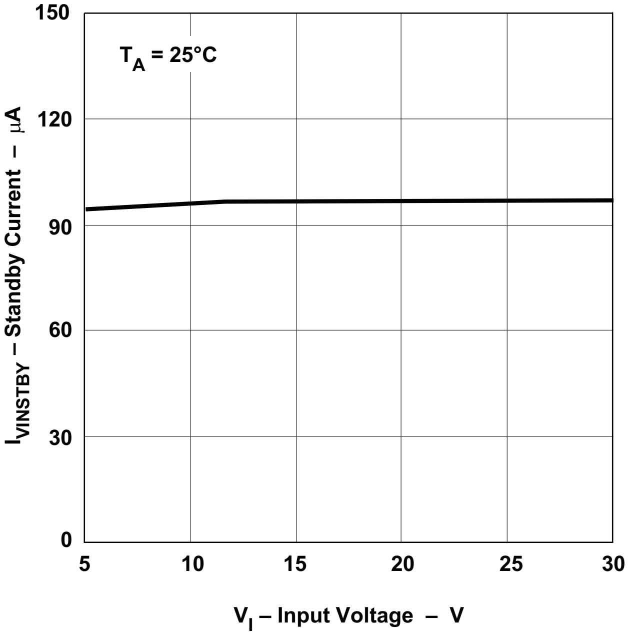


Figure 4.

TYPICAL CHARACTERISTICS (continued)

NO LOAD BATTERY CURRENT
vs
INPUT VOLTAGE

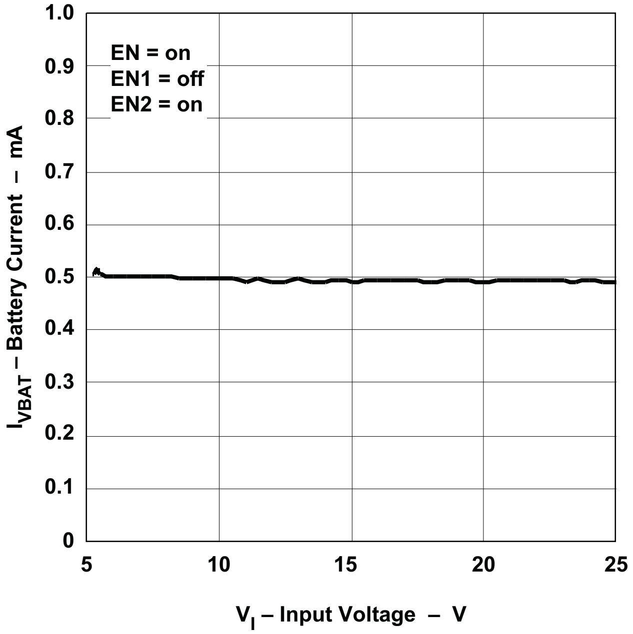


Figure 5.

NO LOAD BATTERY CURRENT
vs
INPUT VOLTAGE

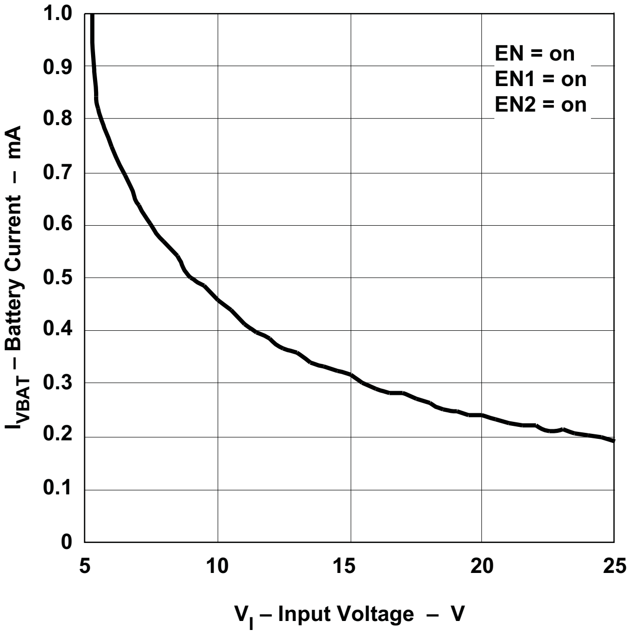


Figure 6.

BATTERY CURRENT
vs
INPUT VOLTAGE

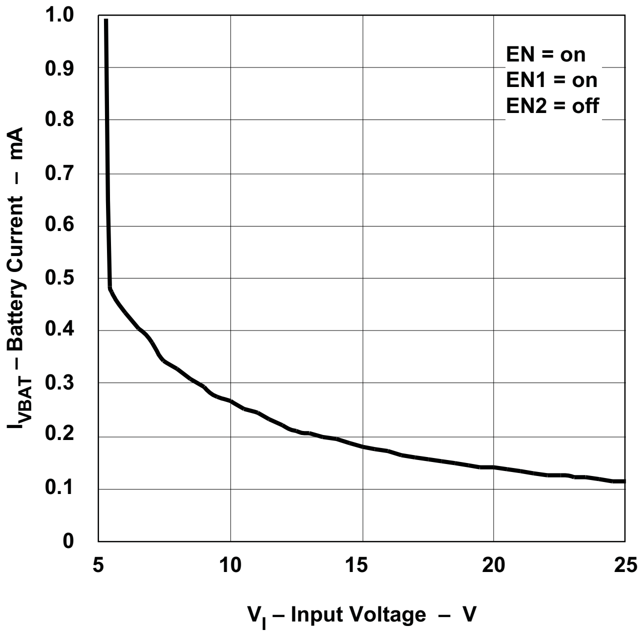


Figure 7.

VREF2 OUTPUT VOLTAGE
vs
OUTPUT CURRENT

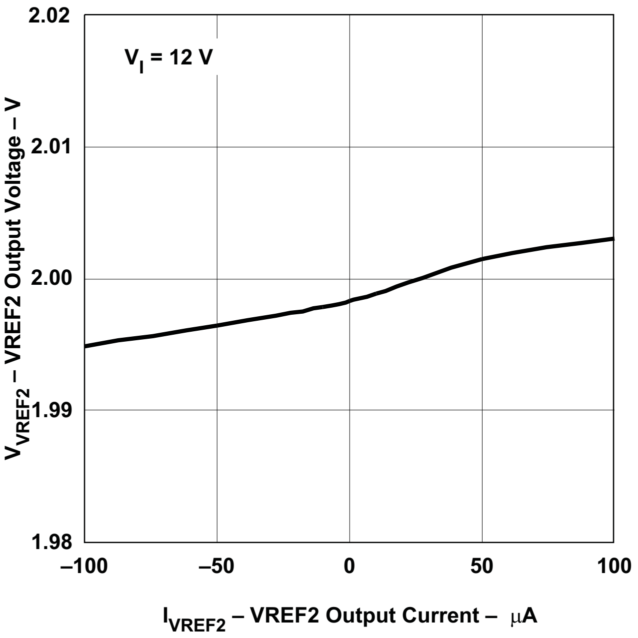


Figure 8.

TYPICAL CHARACTERISTICS (continued)

VREG3 OUTPUT VOLTAGE
vs
OUTPUT CURRENT

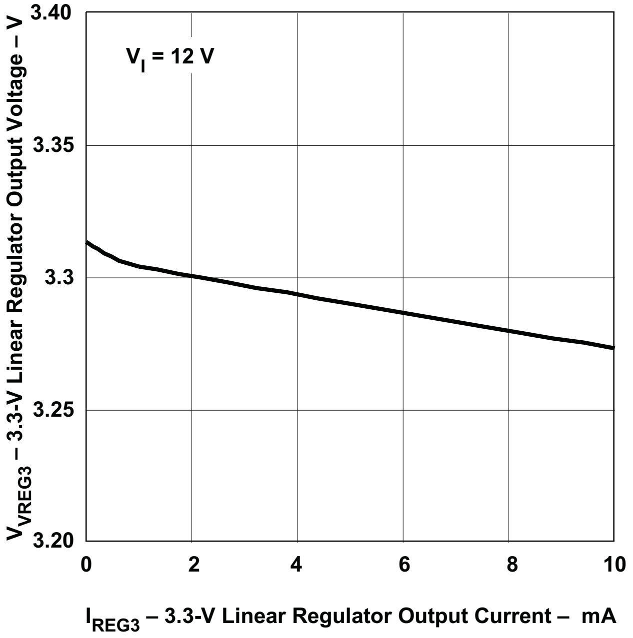


Figure 9.

VREG5 OUTPUT VOLTAGE
vs
OUTPUT CURRENT

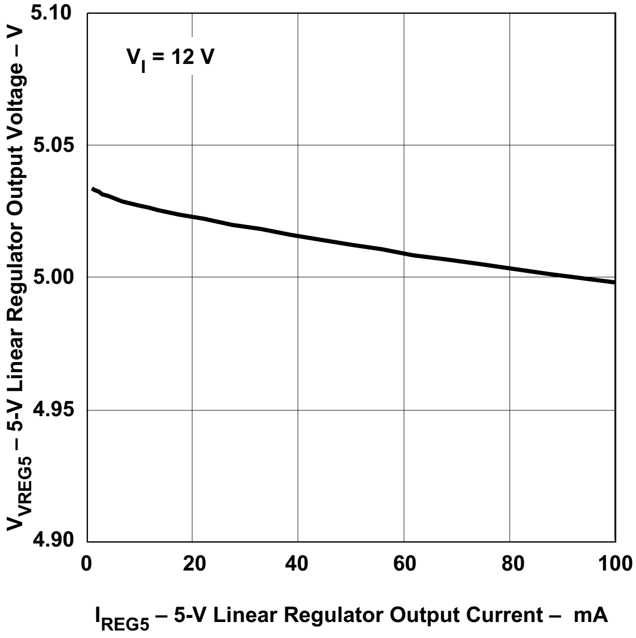


Figure 10.

SWITCHING FREQUENCY
vs
JUNCTION TEMPERATURE

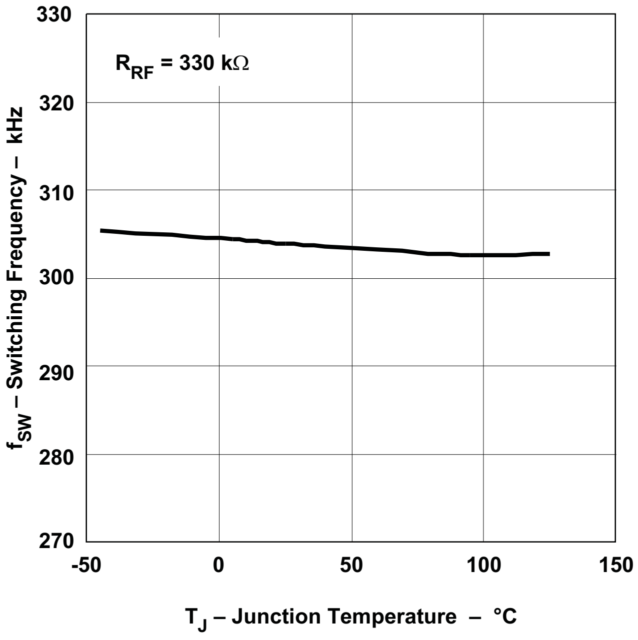


Figure 11.

FORWARD VOLTAGE OF BOOST SW
vs
JUNCTION TEMPERATURE

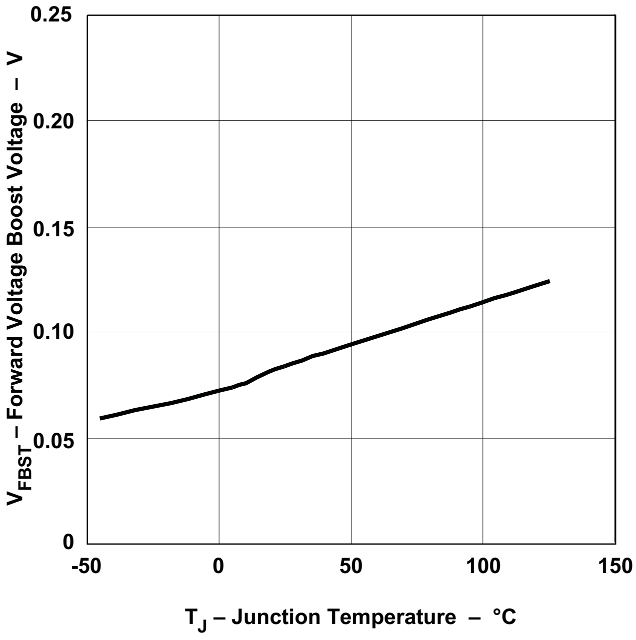


Figure 12.

TYPICAL CHARACTERISTICS (continued)

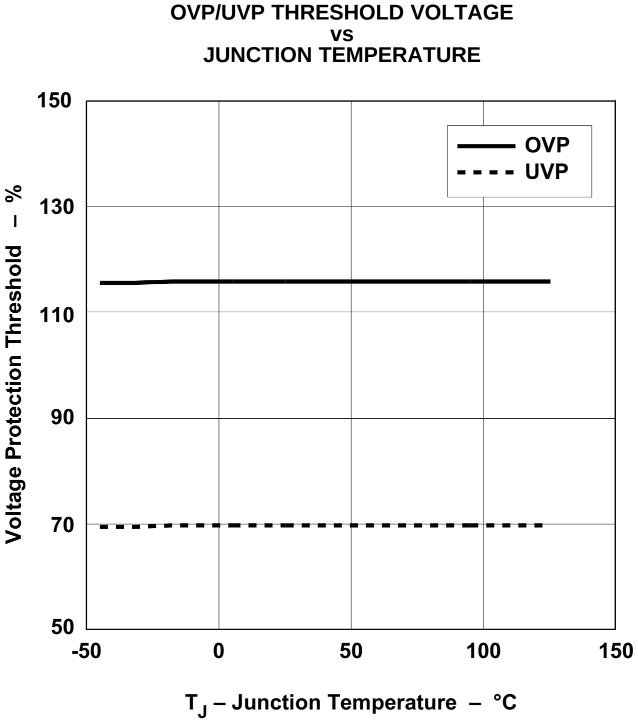


Figure 13.

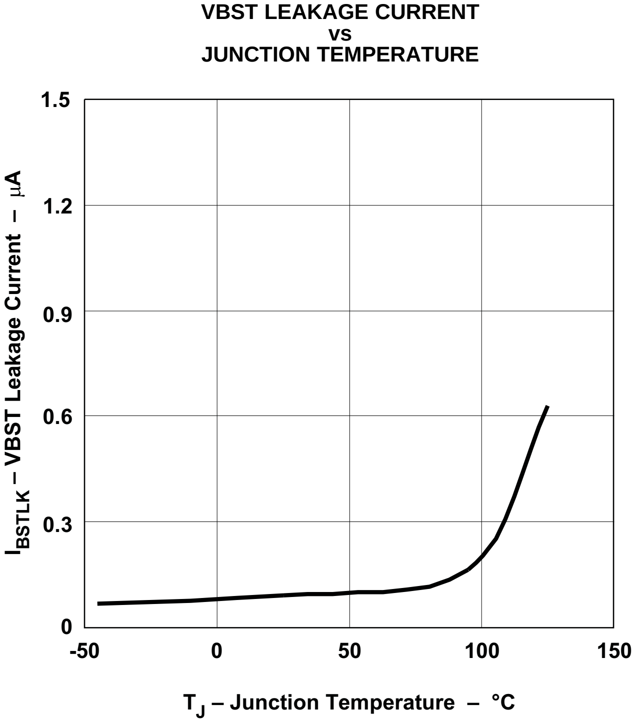


Figure 14.

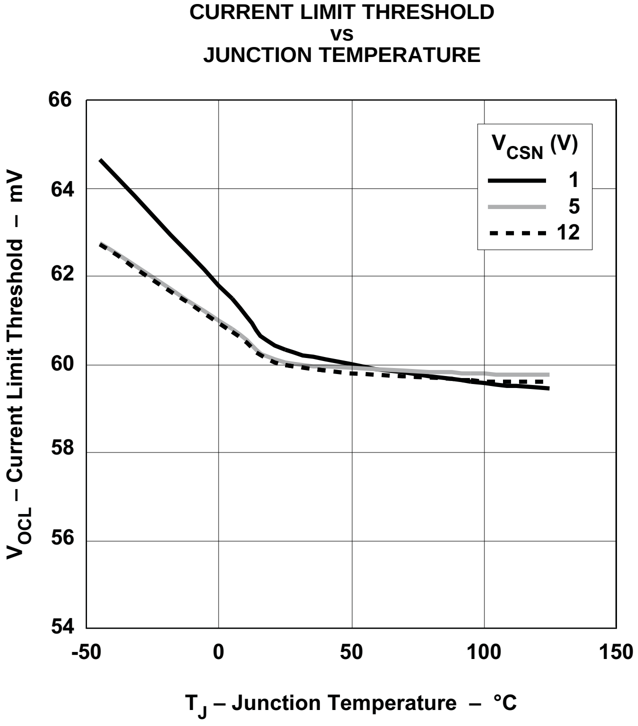


Figure 15.

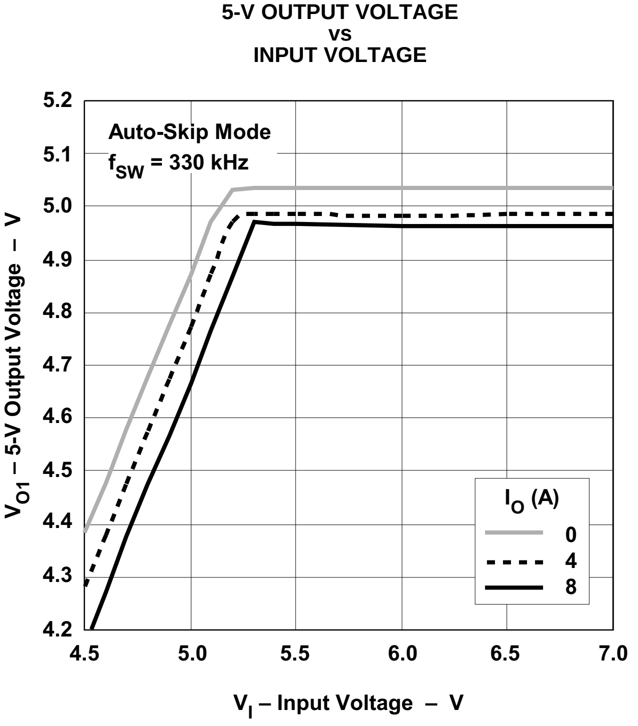


Figure 16.

TYPICAL CHARACTERISTICS (continued)

3.3-V OUTPUT VOLTAGE
vs
INPUT VOLTAGE

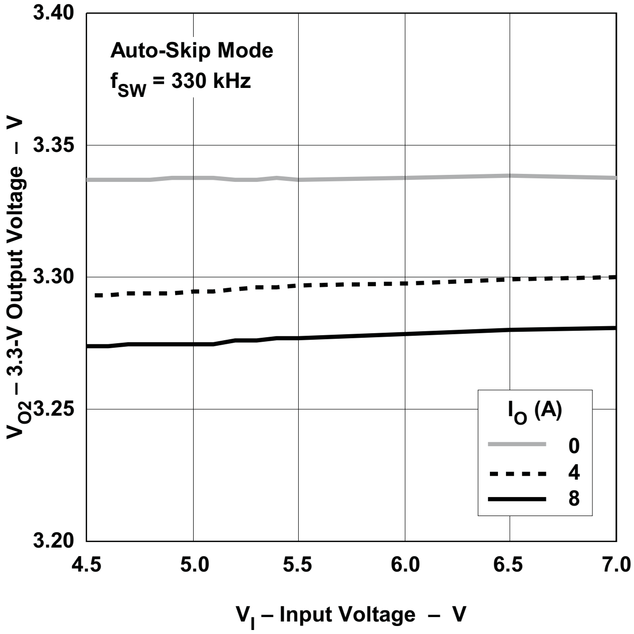


Figure 17.

5-V EFFICIENCY
vs
OUTPUT CURRENT

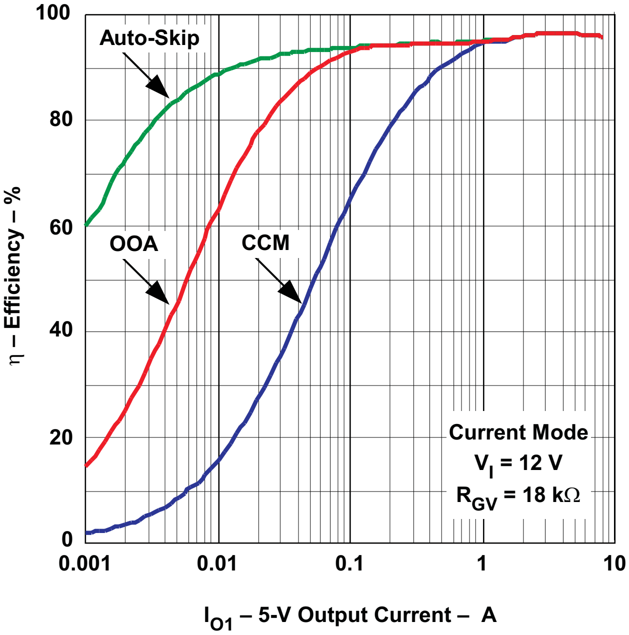


Figure 18.

5-V EFFICIENCY
vs
OUTPUT CURRENT

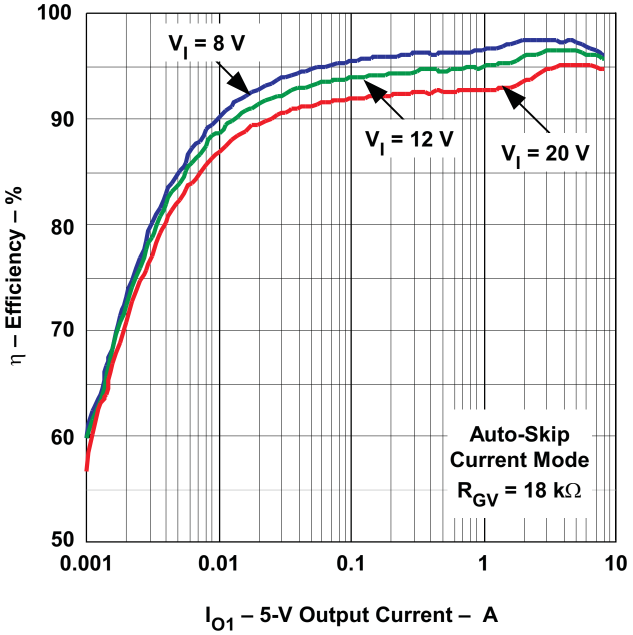


Figure 19.

3.3-V EFFICIENCY
vs
OUTPUT CURRENT

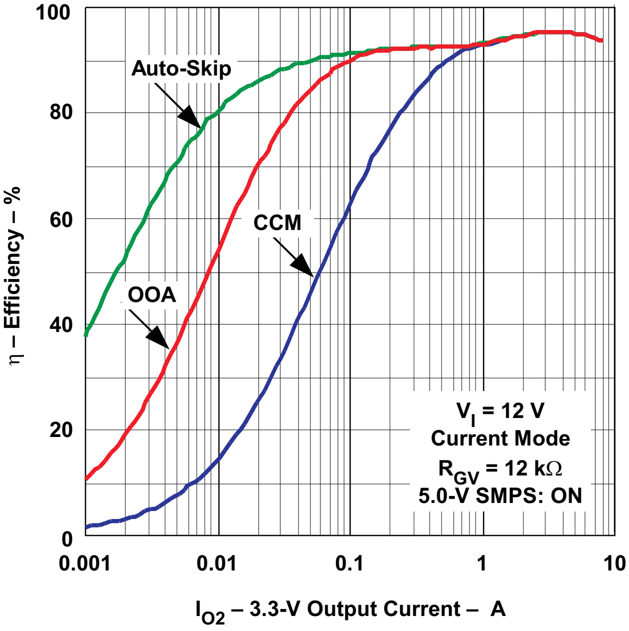


Figure 20.

TYPICAL CHARACTERISTICS (continued)

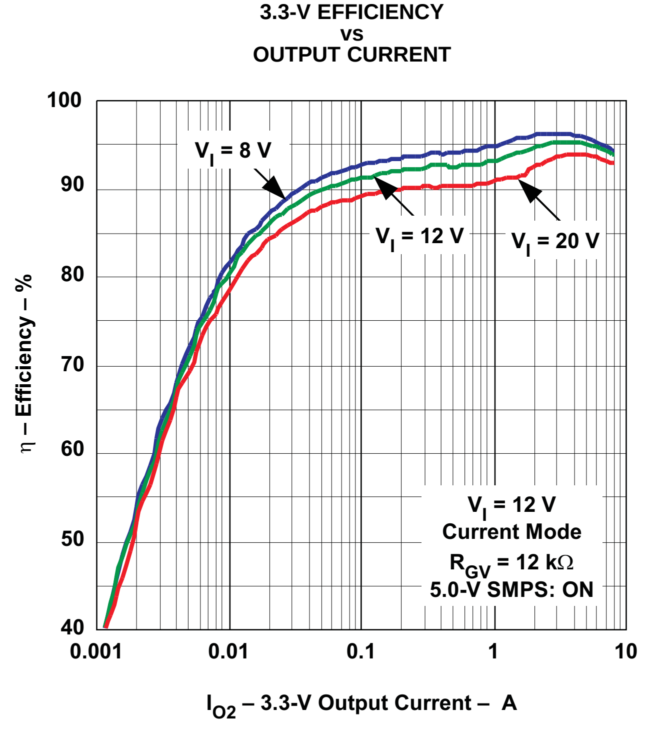


Figure 21.

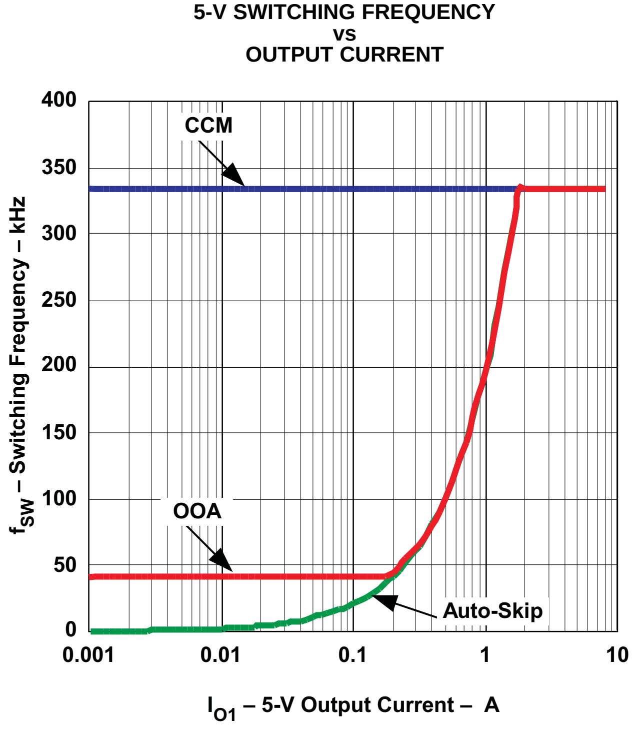


Figure 22.

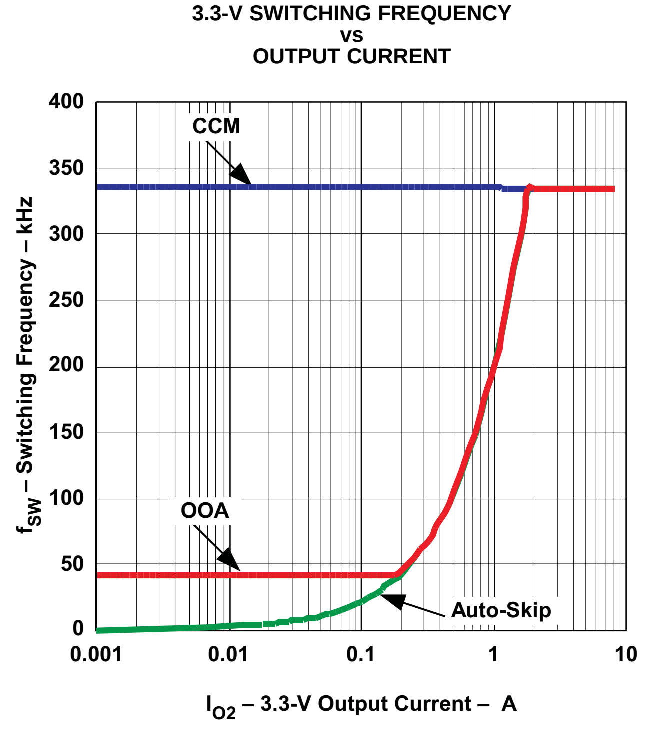


Figure 23.

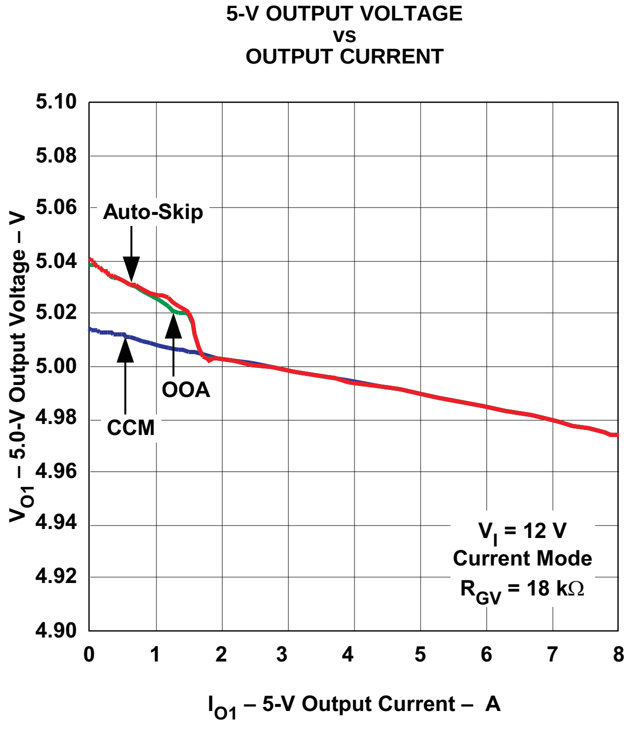


Figure 24.

TYPICAL CHARACTERISTICS (continued)

3.3-V OUTPUT VOLTAGE vs OUTPUT CURRENT

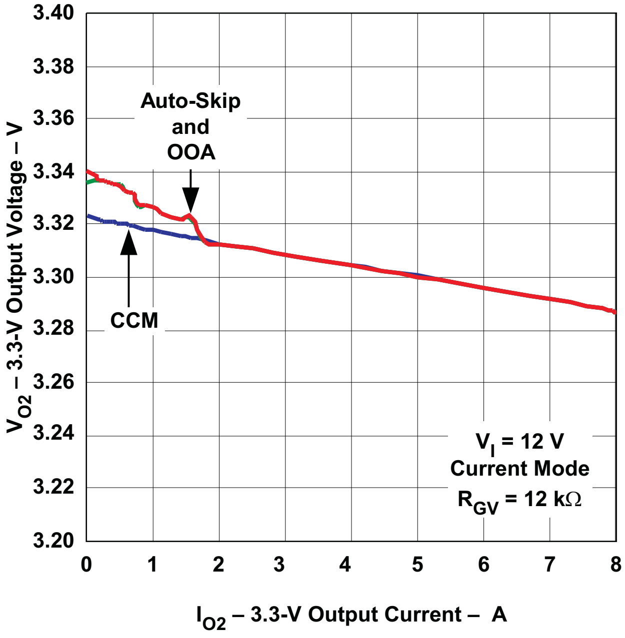


Figure 25.

5-V OUTPUT VOLTAGE vs OUTPUT CURRENT

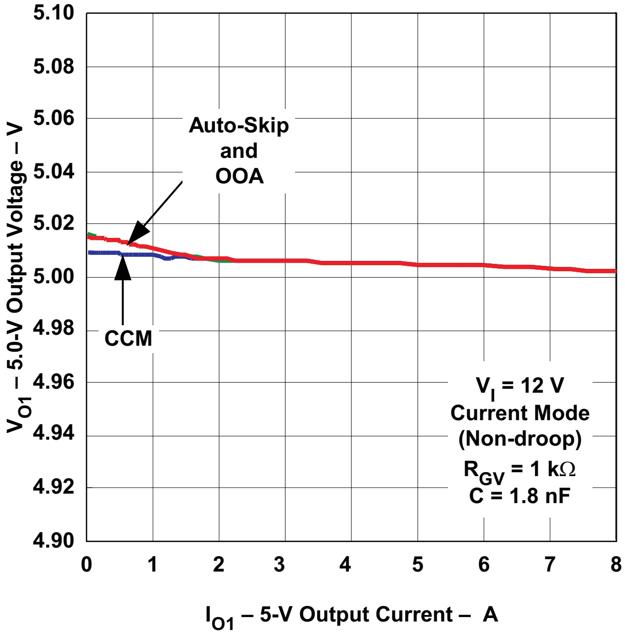


Figure 26.

3.3-V OUTPUT VOLTAGE vs OUTPUT CURRENT

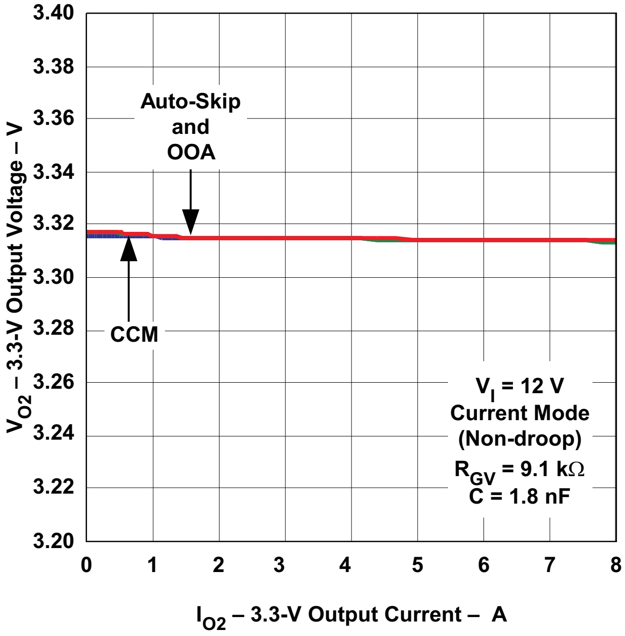


Figure 27.

5.0-V BODE-PLOT – GAIN AND PHASE vs FREQUENCY

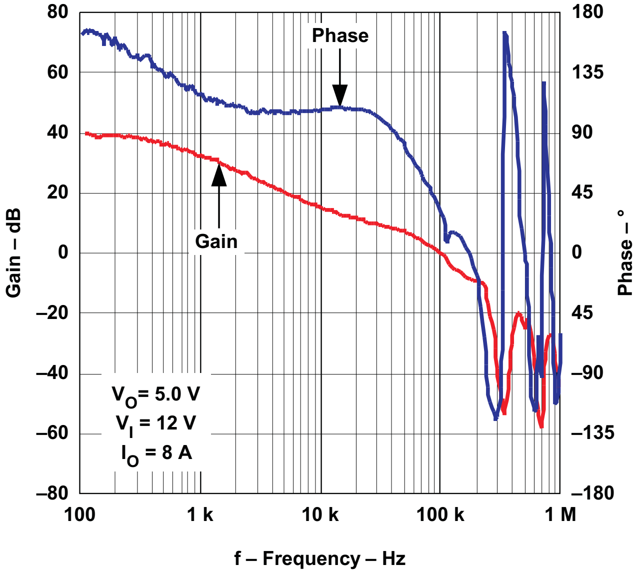


Figure 28.

TYPICAL CHARACTERISTICS (continued)

3.3-V BODE-PLOT – GAIN AND PHASE vs FREQUENCY

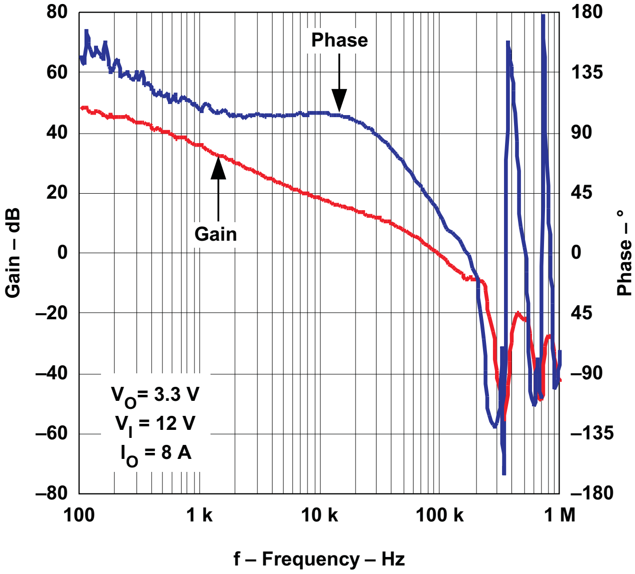


Figure 29.

5.0-V SWITCH-OVER WAVEFORMS

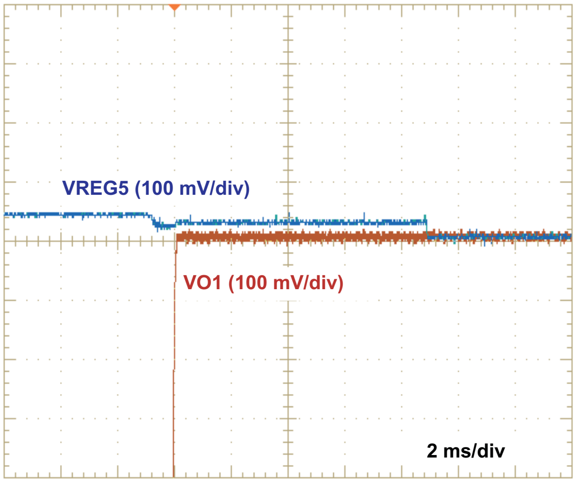


Figure 30.

CURRENT MONITOR VOLTAGE vs OUTPUT CURRENT

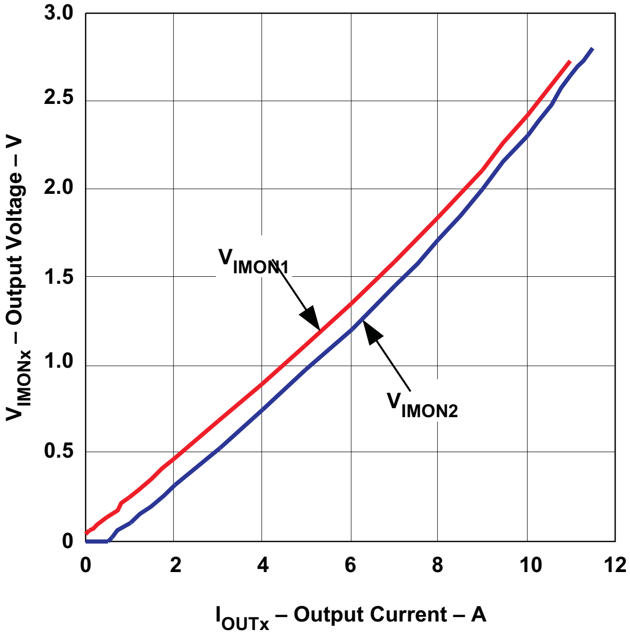


Figure 31.

TYPICAL CHARACTERISTICS

5.0-V START-UP WAVEFORMS

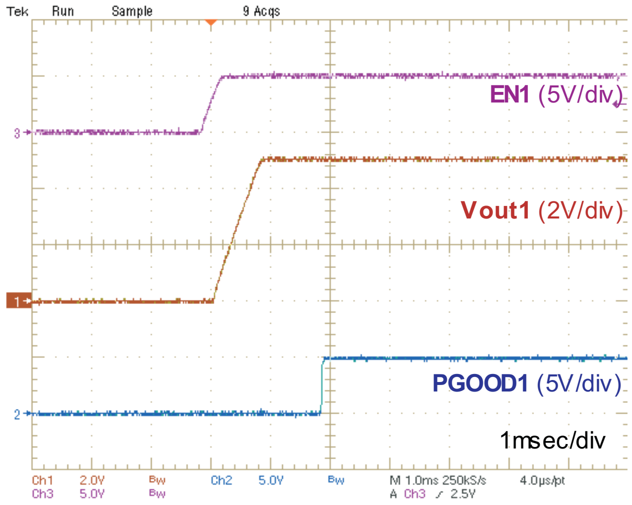


Figure 32.

3.3-V START-UP WAVEFORMS

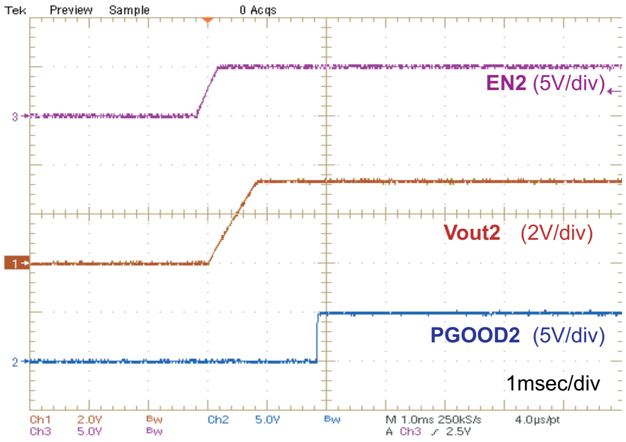


Figure 33.

5.0-V SOFT-STOP WAVEFORMS

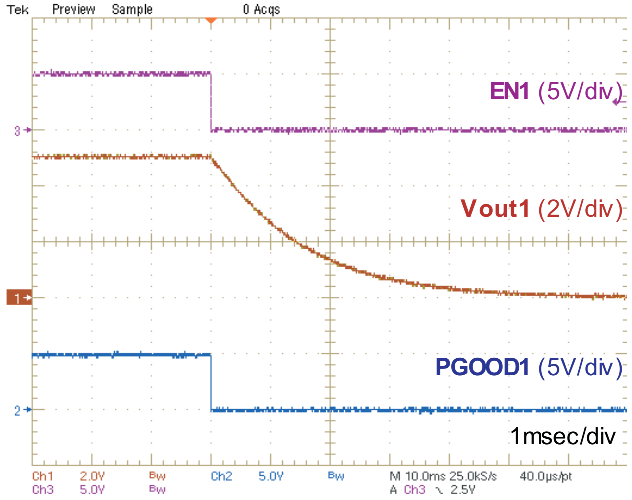


Figure 34.

3.3-V SOFT-STOP WAVEFORMS

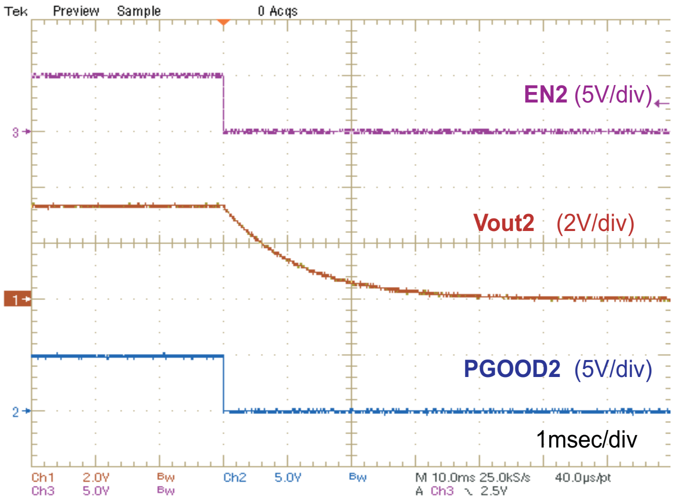


Figure 35.

TYPICAL CHARACTERISTICS (continued)

5.0-V LOAD TRANSIENT RESPONSE

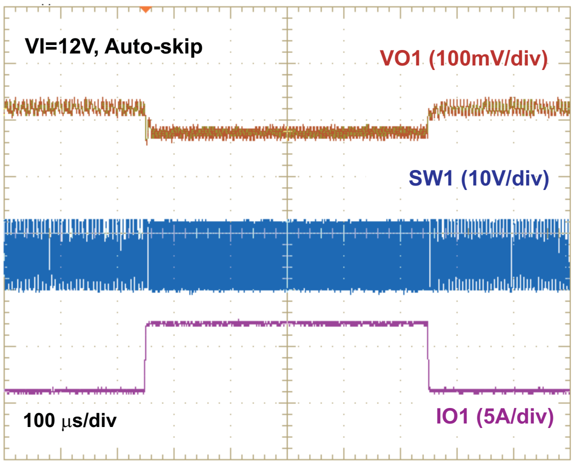


Figure 36.

3.3-V LOAD TRANSIENT RESPONSE

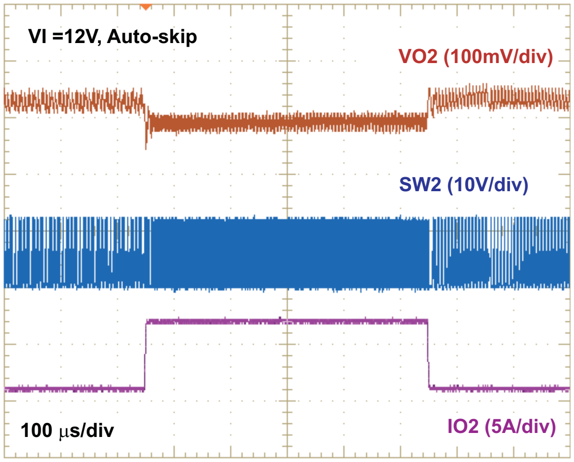


Figure 37.

DETAILED DESCRIPTION

ENABLE AND SOFT START

When EN is *Low*, the TPS51222 is in the shutdown state. Only the 3.3-V LDO stays alive, and consumes 7 µA (typically). When EN becomes *High*, the TPS51222 is in the standby state. The 2-V reference and the 5-V LDO become enabled, and consume about 80 µA with no load condition, and are ready to turn on SMPS channels. Each SMPS channel is turned on when ENx becomes *High*. After ENx is set to high, the TPS51222 begins the softstart sequence, and ramps up the output voltage from zero to the target voltage in 0.96 ms. However, if a slower soft-start is required, an external capacitor can be tied from the ENx pin to GND. In this case, the TPS51222 charges the external capacitor with the integrated 2-µA current source. An approximate external soft-start time would be $t_{EX\text{-}SS} = C_{EX} / I_{EN12}$, which means the time from ENx = 1 V to ENx = 2 V. The recommend capacitance is more than 2.2 nF.

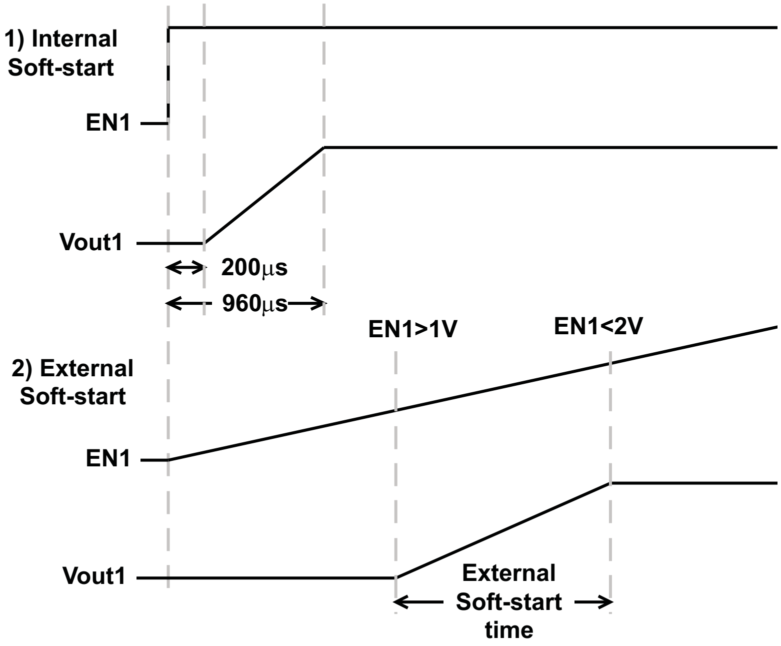


Figure 38. Enable and Soft-start Timing

Table 1. Enable Logic States

EN	EN1	EN2	VREG3	VREF2	VREG5	CH1	CH2
GND	Don't Care	Don't Care	**ON**	Off	Off	Off	Off
Hi	Lo	Lo	**ON**	**ON**	**ON**	Off	Off
Hi	Hi	Lo	**ON**	**ON**	**ON**	**ON**	Off
Hi	Lo	Hi	**ON**	**ON**	**ON**	Off	**ON**
Hi	Hi	Hi	**ON**	**ON**	**ON**	**ON**	**ON**

3.3-V, 10-mA LDO (VREG3)

A 3.3-V, 10-mA, linear regulator is integrated in the TPS51222. This LDO services some of the analog circuit in the device and provides a handy standby supply for 3.3-V *Always On* voltage in the notebook system. Apply a 2.2-µF (at least 1-µF), high quality X5R or X7R ceramic capacitor from VREG3 to (signal) GND in adjacent to the device.

2-V, 100-µA Sink/Source Reference (VREF2)

This voltage is used for the reference of the loop compensation network. Apply a 0.22-µF (at least 0.1-µF), high-quality X5R or X7R ceramic capacitor from VREF2 to (signal) GND in adjacent to the device.

5.0-V, 100-mA LDO (VREG5)

A 5.0-V, 100-mA, linear regulator is integrated in the TPS51222. This LDO services the main analog supply rail and provides the current for gate drivers until switch-over function becomes enable. Apply a 10-µF (at least 4.7-µF), high-quality X5R or X7R ceramic capacitor from VREG5 to (power) GND in adjacent to the device.

VREG5 SWITCHOVER

When EN1 is high, PGOOD1 indicates *GOOD* and a voltage of more than 4.8 V is applied to V5SW, the internal 5V-LDO is shut off and the VREG5 is shorted to V5SW by an internal MOSFET after an 7.7-ms delay. When the V5SW voltage becomes lower than 4.65 V, EN1 becomes low, or PGOOD1 indicates *BAD*, the internal switch is turned off, and the internal 5V-LDO resumes immediately.

BASIC PWM OPERATIONS

The main control loop of the SMPS is designed as a fixed frequency, peak current mode, pulse width modulation (PWM) controller. It achieves stable operation with any type of output capacitors, including low ESR capacitor(s) such as ceramic or specialty polymer capacitors.

The current mode scheme uses the output voltage information and the inductor current information to regulate the output voltage. The output voltage information is sensed by VFBx pin. The signal is compared with the internal 1-V reference and the voltage difference is amplified by a transconductance amplifier (VFB-AMP). The inductor current information is sensed by CSPx and CSNx pins. The voltage difference is amplified by another transconductance amplifier (CS-AMP). The output of the VFB-AMP indicates the target peak inductor current. If the output voltage decreases, the TPS51222 increases the target inductor current to raise the output voltage. Alternatively, if the output voltage rises, the TPS51222 decreases the target inductor current to reduce the output voltage.

At the beginning of each clock cycle, the high-side MOSFET is turned on, or becomes ‘ON’ state. The high-side MOSFET is turned off, or becomes *OFF* state, after the inductor current becomes the target value which is determined by the combination value of the output of the VFB-AMP and a ramp compensation signal. The ramp compensation signal is used to prevent sub-harmonic oscillation of the inductor current control loop. The high-side MOSFET is turned on again at the next clock cycle. By repeating the operation in this manner, the controller regulates the output voltage. The synchronous low-side or the *rectifying* MOSFET is turned on each *OFF* state to keep the conduction loss minimum.

PWM FREQUENCY CONTROL

The TPS51222 has a fixed frequency control scheme with 180° phase shift. The switching frequency can be determined by an external resistor which is connected between RF pin and GND, and can be calculated using Equation 1.

$$f_{SW}\left[\text{kHz}\right] = \frac{1 \times 10^5}{RF\left[\text{k}\Omega\right]} \qquad (1)$$

TPS51222 can also synchronize to more than 2.5 V amplitude external clock by applying the signal to the RF pin. The set timing of channel 1 initiates at the raising edge (1.3 V typ) of the clock and channel 2 initiates at the falling edge (1.1 V typ). Therefore, the 50% duty signal makes both channels 180° phase shift.

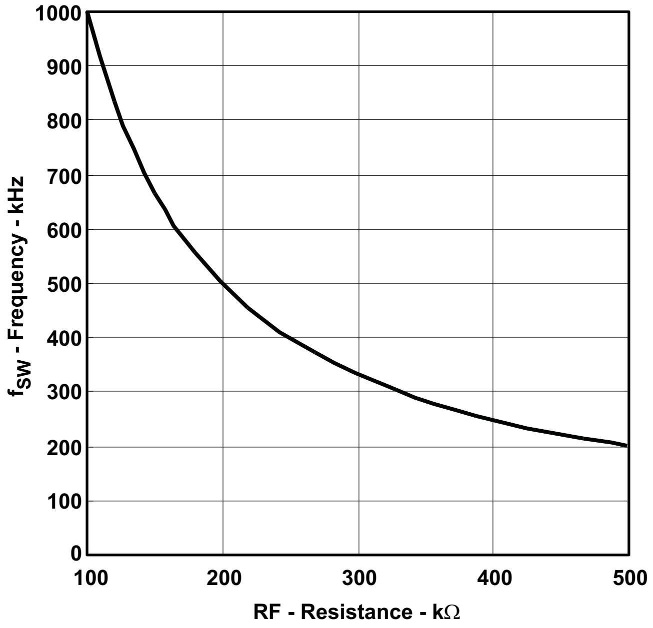


Figure 39. Switching Frequency vs RF

LIGHT LOAD OPERATION

The TPS51222 automatically reduces switching frequency at light load conditions to maintain high efficiency if *Auto Skip* or *Out-of-Audio*™ mode is selected by SKIPSELx. This reduction of frequency is achieved by skipping pulses. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its *peak* reaches a predetermined current, $I_{LL(PEAK)}$, which indicates the boundary between heavy-load condditions and light-load conditions. Once the top MOSFET is turned on, the TPS51222 does not allow it to be turned off until it reaches $I_{LL(PEAK)}$. This eventually causes an overvoltage condition to the output and pulse skipping. From the next pulse after zero-crossing is detected, $I_{LL(PEAK)}$ is limited by the ramp-down signal $I_{LL(PEAK)RAMP}$, which starts from 25% of the overcurrent limit setting ($I_{OCL(PEAK)}$: (see the *Current Protection* section) toward 5% of $I_{OCL(PEAK)}$ over one switching cycle to prevent causing large ripple. The transition load point to the light load operation $I_{LL(DC)}$ can be calculated in Equation 2.

$$I_{LL(DC)} = I_{LL(PEAK)} - 0.5 \times I_{IND(RIPPLE)} \qquad (2)$$

$$I_{IND(RIPPLE)} = \frac{1}{L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \qquad (3)$$

where

- f_{SW} is the PWM switching frequency which is determined by RF resistor setting or external clock

$$I_{LL(PEAK)RAMP} = \left(0.2 - 0.13 \times t_{ON} \times f_{SW}\right) \times t \times I_{OCL(PEAK)} \qquad (4)$$

Switching frequency versus output current in the light load condition is a function of L, f, V_{IN} and V_{OUT}, but it decreases almost proportionally to the output current from the $I_{LL(DC)}$, as described in Equation 2; while maintaining the switching synchronization with the clock. Due to the synchronization, the switching waveform in boundary load condition (close to $I_{LL(DC)}$) appears as a sub-harmonic oscillation; however, it is the intended operation.

If SKIPSELx is tied to GND, the TPS51222 works on a constant frequency of f_{SW} regardless its load current.

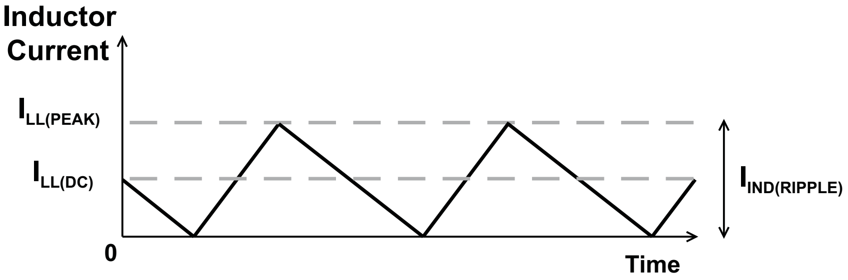


Figure 40. Boundary Between Pulse Skipping and CCM

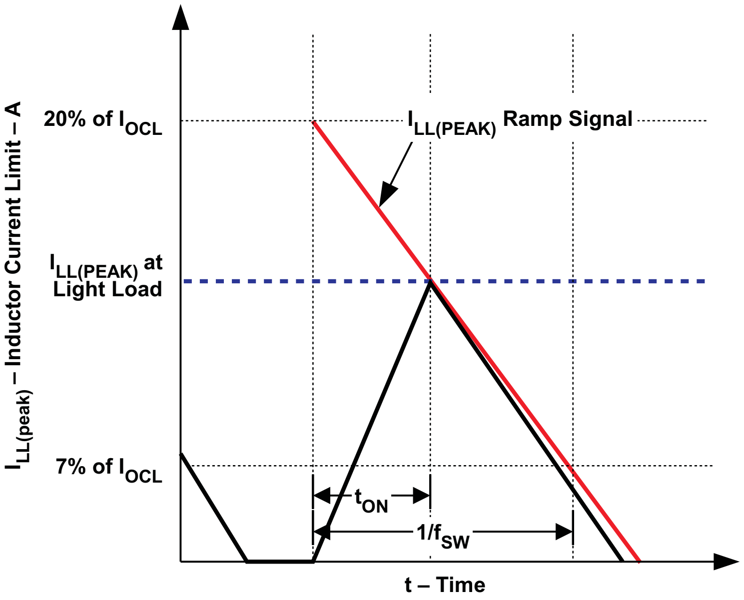


Figure 41. Inductor Current Limit at Pulse Skipping

Table 2. Skip Mode Selection

SKIPSELx	GND	VREF2	VREG3	VREG5
OPERATING MODE	Continuous Conduction	Auto Skip	OOA Skip (maximum 7 skips, for <400 kHz)	OOA Skip (maximum 15 skips, for equal to or greater than 400kHz)

OUT OF AUDIO SKIP OPERATION

Out-Of-Audio™ (OOA) light-load mode is a unique control feature that keeps the switching frequency above acoustic audible frequencies toward virtually no load condition while maintaining state-of-the-art high conversion efficiency. When OOA is selected, the switching frequency is kept higher than audible frequency range in any load condition. The TPS51222 automatically reduced switching frequency at light-load conditions. The OOA control circuit monitors the states of both MOSFETs and forces an *ON* state if the predetermined number of pulses are skipped. The high-side MOSFET is turned on before the output voltage declines down to the target value, so that eventually an overvoltage condition is caused. The OOA control circuit detects this overvoltage condition and begins modulating the skip-mode on time to keep the output voltage.

The TPS51222 supports a wide-switching frequency range, therefore, the OOA skip mode has two selections. See Table 2. When the 300-kHz switching frequency is selected, a maximum of seven (7) skips (SKIPSEL=3.3 V) makes the lowest frequency at 37.5 kHz. If a 15-skip maximum is chosen, it becomes 18.8 kHz, hence the maximum 7 skip is suitable for less than 400 kHz, and the maximum 15 skip is 400 kHz or greater.

99% DUTY CYCLE OPERATION

In a low-dropout condition such as 5-V input to 5-V output, the basic control loop attempts to maintain 100% of the high-side MOSFET *ON*. However, with the N-channel MOSFET used for the top switch, it is not possible to use the 100% on-cycle to charge the boot strap capacitor. TPS51222 detects the 100% *ON* condition and asserts the *OFF* state at the appropriate time.

HIGH-SIDE DRIVER

The high-side driver is designed to drive high current, low $R_{DS(on)}$ N-channel MOSFET(s). The drive capability is represented by its internal resistance, which is 1.7Ω for VBSTx to DRVHx, and 1Ω for DRVHx to SWx. When configured as a floating driver, 5 V of bias voltage is delivered from VREG5 supply. The instantaneous drive current is supplied by the flying capacitor between VBSTx and SWx pins. The average drive current is equal to the gate charge at Vgs = 5V times switching frequency. This gate drive current as well as the low-side gate drive current times 5 V makes the driving power which needs to be dissipated mainly from TPS51222 package. A dead time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on.

LOW-SIDE DRIVER

The low-side driver is designed to drive high-current low-$R_{DS(on)}$ N-channel MOSFET(s). The drive capability is represented by its internal resistance, which are 1.3Ω for VREG5 to DRVLx and 0.7Ω for DRVLx to GND. The 5-V bias voltage is delivered from VREG5 supply. The instantaneous drive current is supplied by an input capacitor connected between VREG5 and GND. The average drive current is also calculated by the gate charge at Vgs = 5 V times switching frequency.

CURRENT SENSING SCHEME

In order to provide both good accuracy and cost effective solution, the TPS51222 supports external resistor sensing and inductor DCR sensing. An RC network with high quality X5R or X7R ceramic capacitor should be used to extract voltage drop across DCR. 0.1µF is a good value to start the design. CSPx and CSNx should be connected to positive and negative terminal of the sensing device respectively. The output signal of the internal current amplifier becomes 100 mV at the OCL setting point. This means that the current sensing amplifier normalize the current information signal based on the OCL setting. Attaching a RC network recommended even with a resistor sensing scheme to get an accurate current sensing; see the *External Components Selection* session for detailed configurations.

ADAPTIVE ZERO CROSSING

TPS51222 has an adaptive zero crossing circuit which performs optimization of the zero inductor current detection at skip mode operation. This function pursues ideal low-side MOSFET turning off timing and compensates inherent offset voltage of the ZC comparator and delay time of the ZC detection circuit. It prevents SW-node swing-up caused by too late detection and minimizes diode conduction period caused by too early detection. As a result, better light load efficiency is delivered.

CURRENT PROTECTION

TPS51222 has cycle-by-cycle overcurrent limiting control. If the inductor current becomes larger than the overcurrent trip level, TPS51222 turns off high-side MOSFET, turns on low-side MOSFET and waits for the next clock cycle.

$I_{OCL(PEAK)}$ sets peak level of the inductor current. Thus, the dc load current at overcurrent threshold, $I_{OCL(DC)}$, can be calculated as follows;

$$I_{OCL(DC)} = I_{OCL(PEAK)} - 0.5 \times I_{IND(RIPPLE)} \quad (5)$$

$$I_{OCL(PEAK)} = \frac{V_{OCL}}{R_{SENSE}} \quad (6)$$

where

- R_{SENSE} is resistance of current sensing device
- $V_{(OCL)}$ is the overcurrent trip threshold voltage

In an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down, and it ultimately crosses the undervoltage protection threshold and shutdown.

POWERGOOD

The TPS51222 has powergood output for both switcher channels. The powergood function is activated after softstart has finished. If the output voltage becomes within ±5% of the target value, internal comparators detect power good state and the powergood signal becomes high after 1ms internal delay. If the output voltage goes outside of ±10% of the target value, the powergood signal becomes low after 1.5µs internal delay. Apply voltage should be less than 6V and the recommended pull-up resistance value is from 100kΩ to 1MΩ.

OUTPUT DISCHARGE CONTROL

The TPS51222 discharges output when ENx is low. The TPS51222 discharges outputs using an internal MOSFET which is connected to CSNx and GND. The current capability of these MOSFETs is limited to discharge the output capacitor slowly. If ENx becomes high during discharge, MOSFETs are turning off, and some output voltage remains. SMPS changes over to soft-start. The PWM initiates after the target voltage overtakes the remaining output voltage.

OVERVOLTAGE/UNDERVOLTAGE PROTECTION

TPS51222 monitors the output voltage to detect overvoltage and undervoltage. When the output voltage becomes 15% higher than the target value, the OVP comparator output goes high and the circuit latches as the high-side MOSFET driver OFF and the low-side MOSFET driver ON, and shuts off another channel.

When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, TPS51222 latches OFF both high-side and low-side MOSFETs, and shuts off another channel. This UVP function is enabled after soft-start has completed. The procedure for restarting from these protection states is:

1. toggle EN
2. toggle EN1 and EN2 or
3. once hit UVLO

UVLO PROTECTION

The TPS51222 has undervoltage lockout protections (UVLO) for VREG5, VREG3 and VREF2. When the voltage is lower than UVLO threshold voltage, TPS51222 shuts off each output as shown inTable 3. This is non-latch protection.

Table 3. UVLO Protection

	CH1/ CH2	VREG5	VREG3	VREF2
VREG5 UVLO	Off	—	On	On
VREG3 UVLO	Off	Off	—	Off
VREF2 UVLO	Off	Off	On	—

THERMAL SHUTDOWN

The TPS51222 monitors the device temperature. If the temperature exceeds the threshold value, TPS51222 shuts off both SMPS and 5V-LDO, and decreases the VREG3 current limitation to 5 mA (typically). This is non-latch protection.

CURRENT MONITOR

TPS51222 monitors the output current as the voltage difference between CSPx and CSNx terminal. The transconductance amplifier (CS-AMP) amplifies this differential voltage by 50 times and sends out from IMONx thermal. Adding RC filter is recommended.

APPLICATION INFORMATION

EXTERNAL COMPONENTS SELECTION

A buck converter using the TPS51222 consists of linear circuits and a switching modulator. Figure 42 shows the basic scheme.

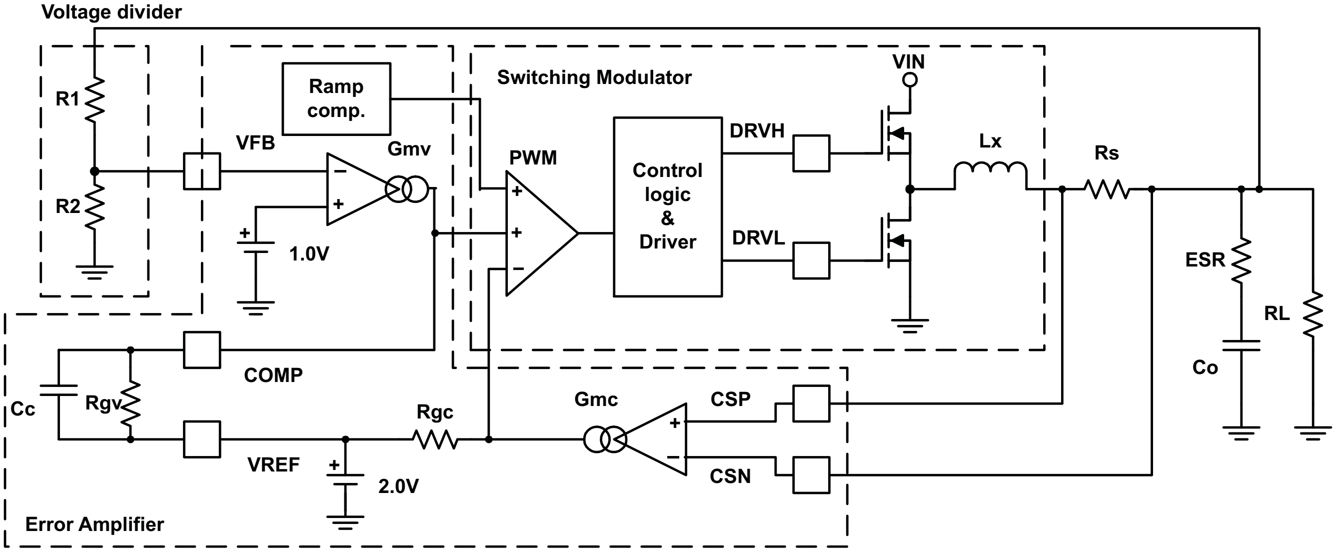


Figure 42. Simplified Current Mode Functional Blocks

The external components can be selected by following manner.

1. Determine output voltage dividing resistors (R1 and R2: shown in Figure 42) using the next equation

$$R1 = \left(V_{OUT} - 1.0\right) \times R2 \tag{7}$$

2. **Determine switching frequency.** Higher frequency allows smaller output capacitances, however, degrade efficiency due to increase of switching loss. Frequency setting resistor for RF-pin can be calculated by;

$$RF[k\Omega] = \frac{1 \times 10^5}{f_{sw}\ [kHz]} \tag{8}$$

3. **Choose the inductor.** The inductance value should be determined to give the ripple current of approximately 25% to 50% of maximum output current. Recommended ripple current rate is about 30% to 40% at the typical input voltage condition, next equation uses 33%.

$$L = \frac{1}{0.33 \times I_{OUT(MAX)} \times f_{SW}} \times \frac{(V_{IN(TYP)} - V_{OUT}) \times V_{OUT}}{V_{IN(TYP)}} \tag{9}$$

   The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation.

4. Determine the sensing resistor.

   Determine the sensing resistor using next equation. $I_{OCL(PEAK)}$ should be approximately 1.5 × $I_{OUT(MAX)}$ to 1.7 × $I_{OUT(MAX)}$.

$$R_{SENSE} = \frac{V_{OCL}}{I_{OCL(PEAK)}} \tag{10}$$

5. **Determine Rgv.** Rgv should be determined from preferable droop compensation value and is given by next equation based on the typical number of Gmv = 500µS.

$$Rgv = 0.1 \times \frac{I_{OUT(MAX)}}{I_{OCL(PEAK)}} \times V_{OUT} \times \frac{1}{Gmv \times Vdroop} \tag{11}$$

$$Rgv[k\Omega] = 200 \times \frac{I_{OUT(MAX)}}{I_{OCL(PEAK)}} \times \frac{V_{OUT}[V]}{Vdroop[mV]} \tag{12}$$

If no-droop is preferred, attach a series RC network circuit instead of single resistor. Series resistance is determined using Equation 12 . Series capacitance can be arbitrarily chosen to meet the RC time constant, but should be kept under 1/10 of f_o.

6. Determine output capacitance *Co* to achieve a stable operation using the next equation. The 0 dB frequency, f_o, should be kept under 1/3 of the switching frequency.

$$f_0 = \frac{5}{\pi} \times I_{OCL(PEAK)} \times \frac{1}{V_{OUT}} \times \frac{Gmv \times Rgv}{Co} < \frac{fsw}{3} \tag{13}$$

$$Co > \frac{15}{\pi} \times I_{OCL(PEAK)} \times \frac{1}{V_{OUT}} \times \frac{Gmv \times Rgv}{fsw} \tag{14}$$

7. **Calculate Cc.** The purpose of this capacitance is to cancel zero caused by *ESR* of the output capacitor. If ceramic capacitor(s) is used, there is no need for Cc. If a combination of different capacitors is used, attach a RC network circuit instead of single capacitance to cancel zeros and poles caused by the output capacitors. With single capacitance, Cc is given in Equation 15.

$$Cc = Co \times \frac{ESR}{Rgv} \tag{15}$$

8. **Choose MOSFETs** Generally, the on resistance affects efficiency at high load conditions as conduction loss. For a low output voltage application, the duty ratio is not high enough so that the on resistance of high-side MOSFET does not affect efficiency; however, switching speed (t_r and t_f) affects efficiency as switching loss. As for low-side MOSFET, the switching loss is usually not a main portion of the total loss.

RESISTOR CURRENT SENSING

For more accurate current sensing with an external resistor, the following technique is recommended. Adding an RC filter to cancel the parasitic inductance of resistor, this filter value is calculated using Equation 16.

$$Cx \times Rx = \frac{Lx}{Rs} \tag{16}$$

This equation means time-constant of Cx and Rx should match the one of Lx (ESL) and Rs.

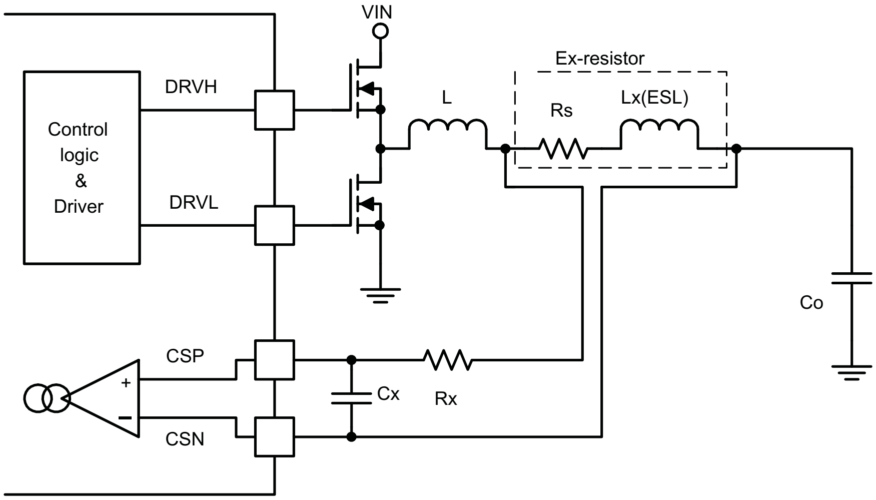


Figure 43. External Resistor Current Sensing

INDUCTOR DCR CURRENT SENSING

To use inductor DCR as current sensing resistor (Rs), the configuration needs to change as below. However, the equation that must be satisfied is the same as the one for the resistor sensing.

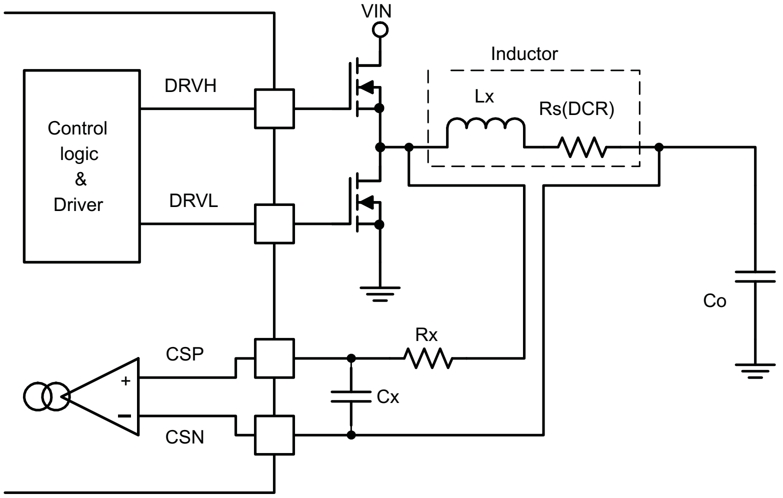


Figure 44. Inductor DCR Current Sensing

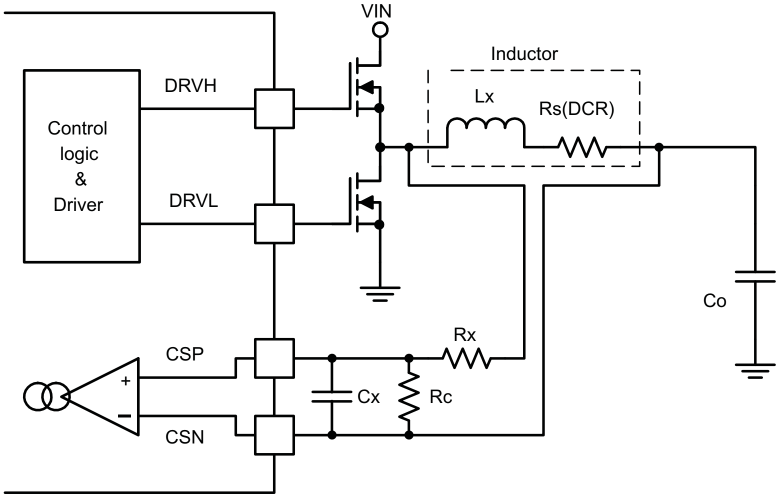


Figure 45. Inductor DCR Current Sensing With Voltage Divider

TPS51222 has a fixed $V_{(OCL)}$ point (60 mV). In order to adjust for DCR, a voltage divider can be configured a described in Figure 45.

For Rx, Rc and Cx can be calculated as shown below, and overcurrent limitation value can be calculated as follows:

$$Cx \times \left(Rx \parallel Rc\right) = \frac{Lx}{Rs} \qquad (17)$$

$$I_{OCL(PEAK)} = V_{OCL} \times \frac{1}{Rs} \times \frac{Rx + Rc}{Rc} \qquad (18)$$

Figure 46 shows the compensation technique for the temperature drifts of the inductor DCR value. This scheme assumes the temperature rise at the thermistor (R_{NTC}) is directly proportional to the temperature rise at the inductor.

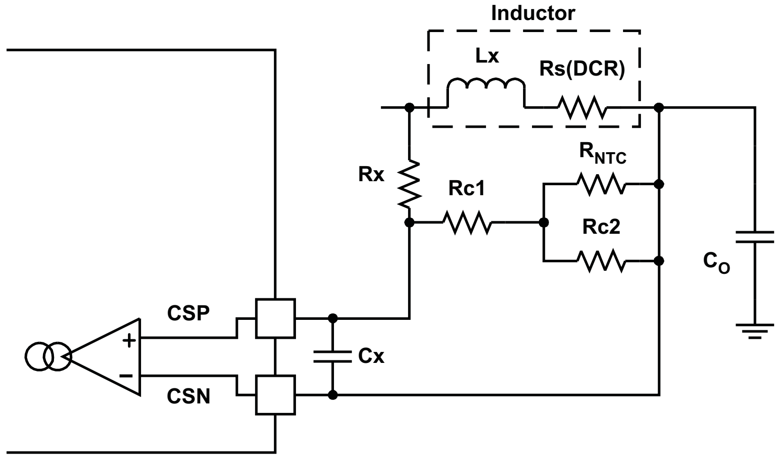


Figure 46. Inductor DCR Current Sensing With Temperature Compensate

LAYOUT CONSIDERATIONS

Certain points must be considered before starting a PCB layout work using the TPS51222.

Placement

- Place RC network for CSP1 and CSP2 close to the device pins.
- Place bypass capacitors for VREG5, VREG3 and VREF2 close to the device pins.
- Place frequency-setting resistor close to the device pin.
- Place the compensation circuits for COMP1 and COMP2 close to the device pins.
- Place the voltage setting resistors close to the device pins.

Routing (sensitive analog portion)

- Use separate traces for; see Figure 47
  - Output voltage sensing from current sensing (negative-side)
  - Output voltage sensing from V5SW input (when V_{OUT} = 5V)
  - Current sensing (positive-side) from switch-node

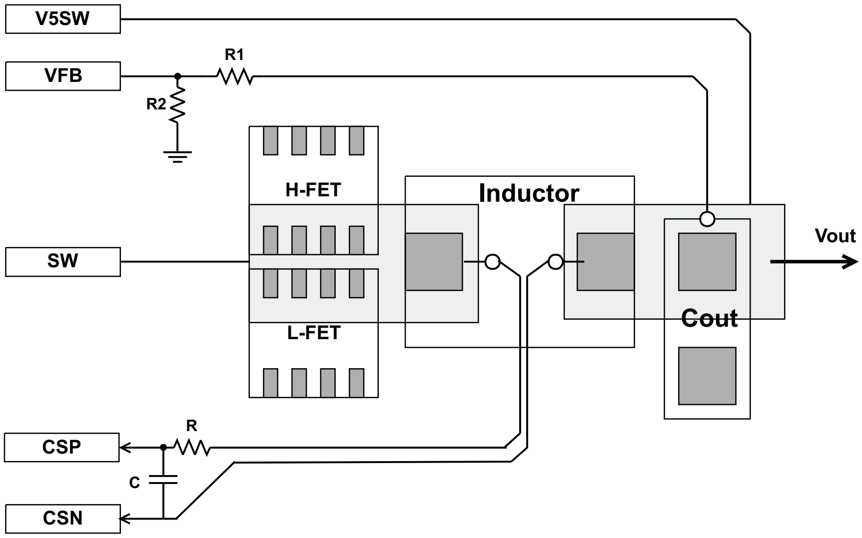


Figure 47. Sensing Trace Routings

- Use Kelvin sensing traces from the solder pads of the current sensing device (inductor or resistor) to current sensing comparator inputs (CSPx and CSNx). (See Figure 48)

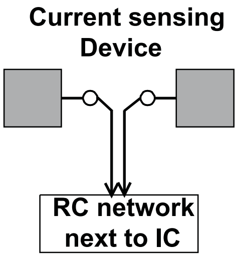


Figure 48. Current Sensing Traces

- Use small copper space for VFBx. These are short and narrow traces to avoid noise coupling
- Connect VFB resistor trace to the positive node of the output capacitor.
- Use signal GND for VREF2 and VREG3 capacitors, RF and VFB resistors, and the other sensitive analog components. Placing a signal GND plane (underneath the IC, and fully covered peripheral components) on the internal layer for shielding purpose is recommended. (See Figure 49)
- Use a thermal land for PowerPAD™. Five or more vias, with 0.33-mm (13-mils) diameter connected from the thermal land to the internal GND plane, should be used to help dissipation. Do NOT connect the GND-pin to this thermal land on the surface layer, underneath the package.

Routing (power portion)

- Use wider/shorter traces of DRVL for low-side gate drivers to reduce stray inductance.
- Use the parallel traces of SW and DRVH for high-side MOSFET gate drive, and keep them away from DRVL.
- Connect SW trace to source terminal of the high-side MOSFET.
- Use power GND for VREG5, VIN and V_{OUT} capacitors and low-side MOSFETs. Power GND and signal GND should be connected near the device GND terminal. (See Figure 49)

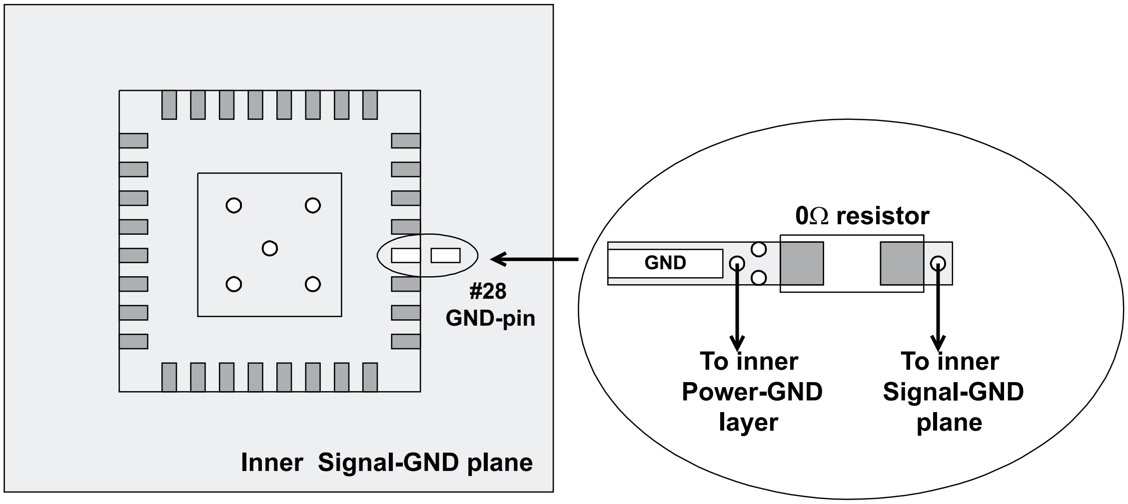


Figure 49. GND Layout Example

APPLICATION CIRCUITS

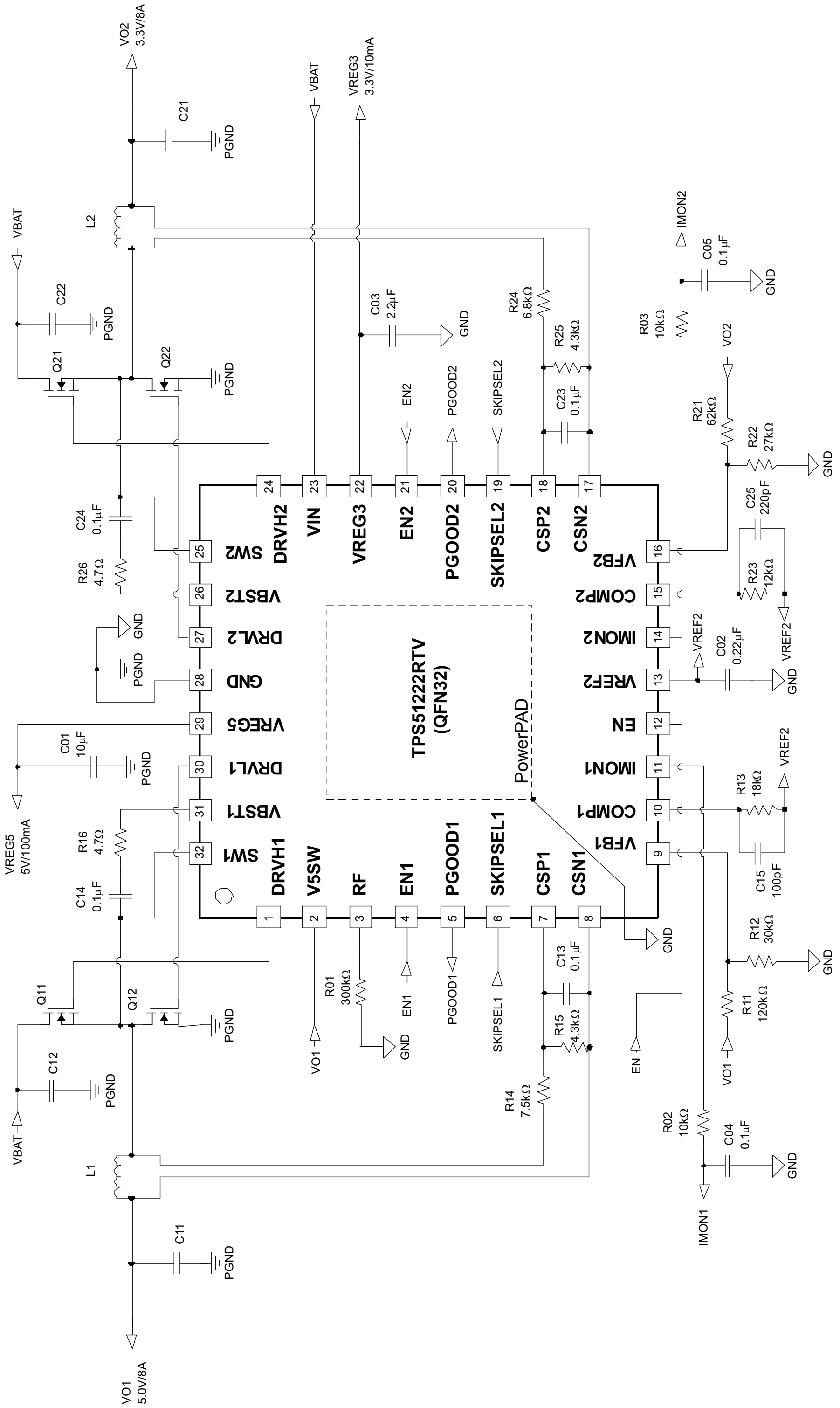


Figure 50. Current Mode, DCR Sensing, 5.0-V/8-A, 3.3-V/8-A, 330-kHz

Table 4. Current Mode, DCR Sensing, 5.0-V/8-A, 3.3-V/8-A, 330-kHz

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C11	2 × 330 µF, 6.3 V, 18 mΩ	Sanyo	6TPE330MIL
C12	2 × 10 µF, 25 V	Murata	GRM32DR71E106K
C21	470 µF, 4.0V, 15 mΩ	Sanyo	4TPE470MFL
C22	2 × 10 µF, 25 V	Murata	GRM32DR71E106K
L1	3.3 µH, 10.7 A, 10.5 mΩ	TOKO	FDV1040-3R3M
L2	3.3 µH, 10.7 A, 10.5 mΩ	TOKO	FDV1040-3R3M
Q11, Q21	30-V, 12 A, 10.5 mΩ	Fairchild	FDMS8692
Q12, Q22	30 V, 18 A, 5.4 mΩ	Fairchild	FDMS8672AS

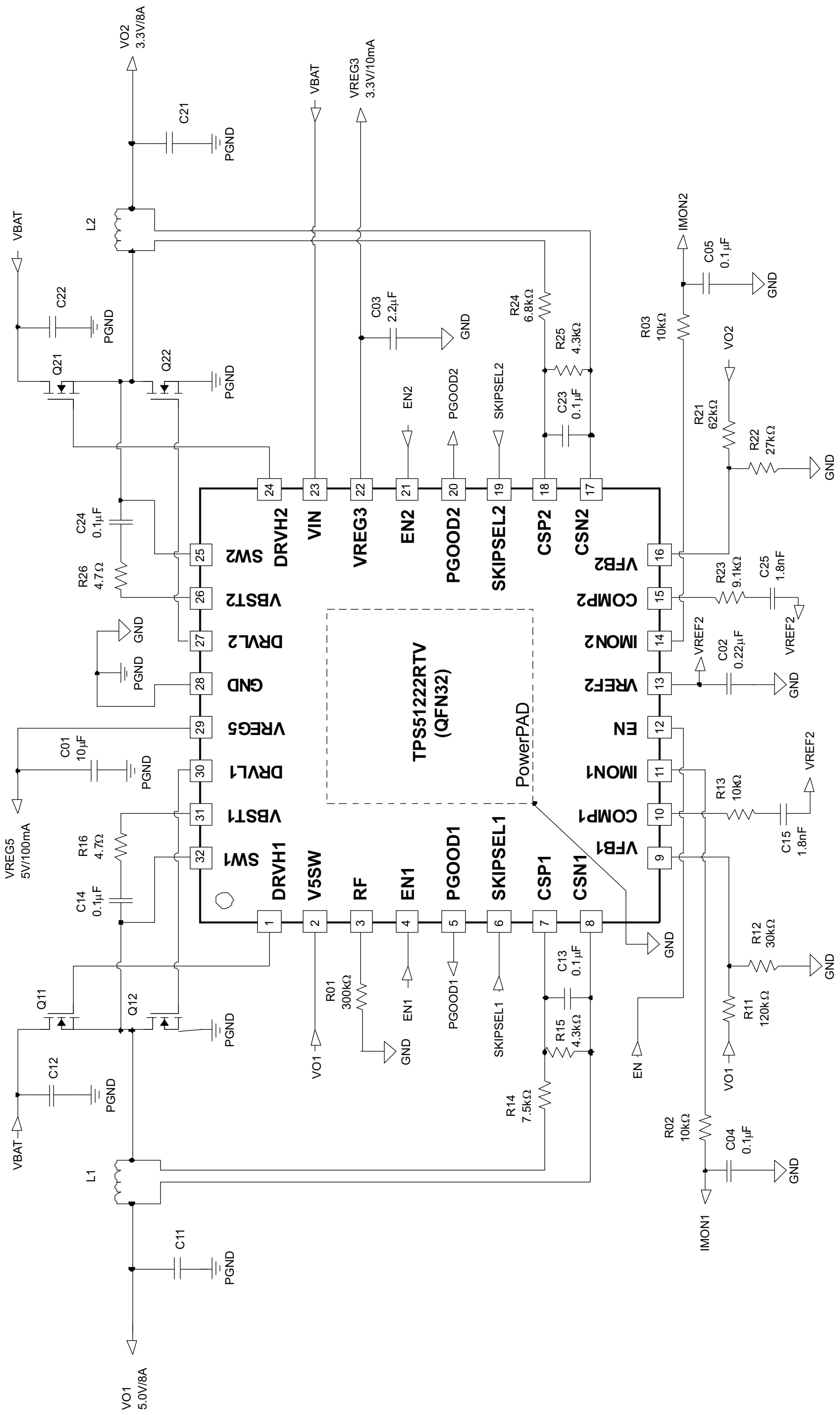


Figure 51. Current Mode (Non-Droop), DCR Sensing, 5.0-V/8-A, 3.3-V/8-A, 330-kHz

Table 5. Current Mode (Non-droop), DCR Sensing, 5.0-V/8-A, 3.3-V/8-A, 330-kHz

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C11	2 x 330 µF, 6.3 V 18 mΩ	Sanyo	6TPE330MIL

Table 5. Current Mode (Non-droop), DCR Sensing, 5.0-V/8-A, 3.3-V/8-A, 330-kHz (continued)

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C12	2 x 10 µF, 25 V	Murata	GRM32DR71E106K
C21	470 µF, 4.0V, 15 mΩ	Sanyo	4TPE470MFL
C22	2 x 10 µF, 25 V	Murata	GRM32DR71E106K
L1	3.3 µH, 10.7 A, 10.5 mΩ	TOKO	FDV1040-3R3M
L2	3.3 µH, 10.7 A, 10.5 mΩ	TOKO	FDV1040-3R3M
Q11, Q21	30-V, 12-A, 10.5 mΩ	Fairchild	FDMS8692
Q12, Q22	30-V, 18-A, 5.4 mΩ	Fairchild	FDMS8672AS

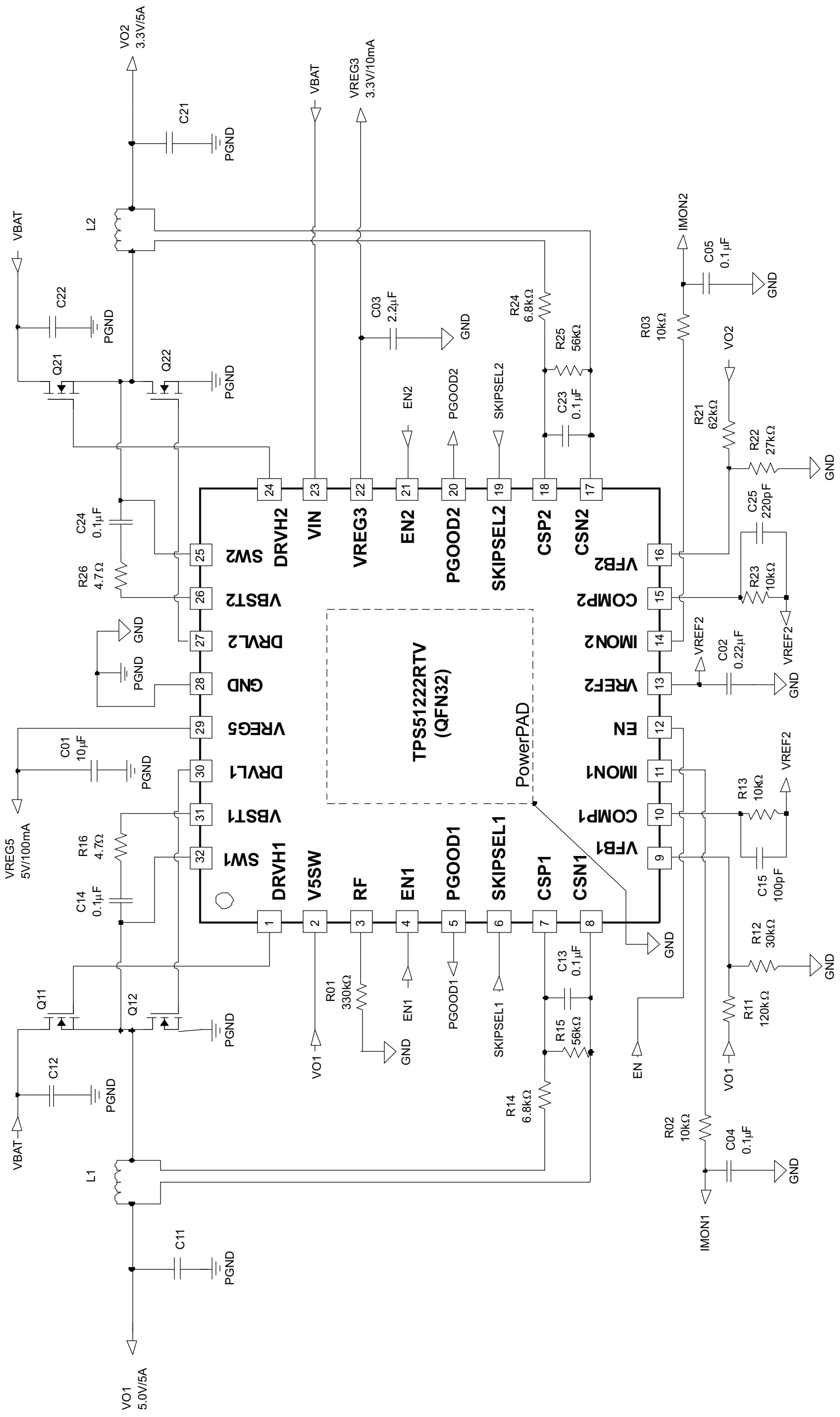


Figure 52. Current Mode, DCR Sensing, 5.0-V/5-A, 3.3-V/5-A, 300-kHz

Table 6. Current Mode, DCR Sensing, 5.0-V/5-A, 3.3-V/5-A, 300-kHz

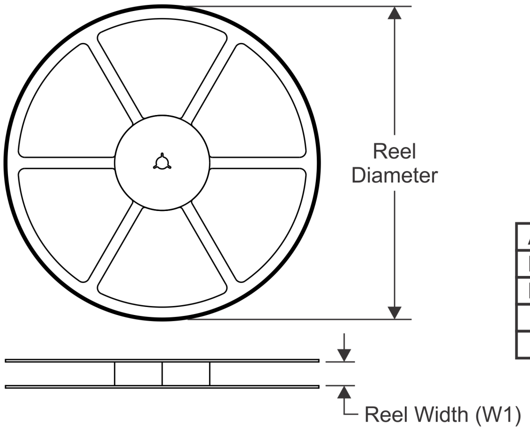
SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C11	2 × 120 µF, 6.3V, 15 mΩ	Panasonic	EEFCX0J121R

Table 6. Current Mode, DCR Sensing, 5.0-V/5-A, 3.3-V/5-A, 300-kHz (continued)

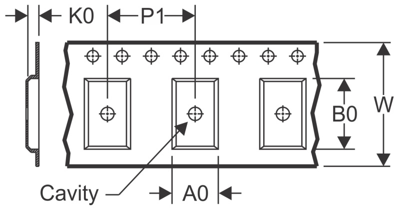
SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C12	2 × 10 µF, 25 V	Murata	GRM32DR71E106K
C21	2 × 220 µF, 4.0 V, 15 mΩ	Panasonic	EEFCX0G221R
C22	2 × 10 µF, 25 V	Murata	GRM32DR71E106K
L1	4.0 µH, 10.3 A, 6.6 mΩ	Sumida	CEP125-4R0MC-H
L2	4.0 µH, 10.3 A, 6.6 mΩ	Sumida	CEP125-4R0MC-H
Q11, Q21	30 V, 13.6 A, 9.5 mΩ	IR	IRF7821
Q12, Q22	30 V, 13.8 A, 5.8 mΩ	IR	IRF8113

TAPE AND REEL INFORMATION

REEL DIMENSIONS

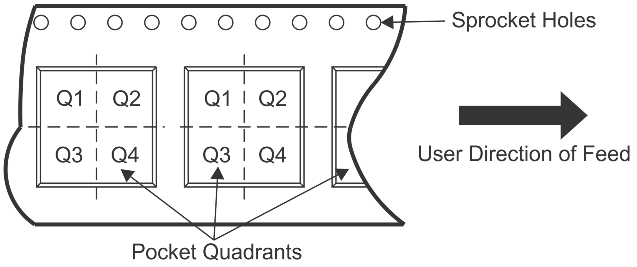


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

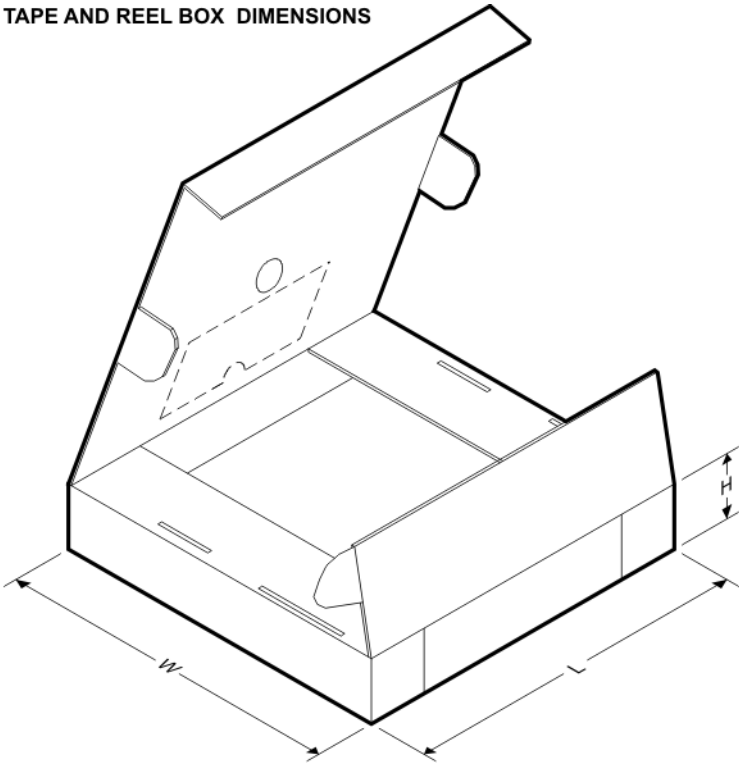
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51222RTVR	WQFN	RTV	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS51222RTVR	WQFN	RTV	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS51222RTVT	WQFN	RTV	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS51222RTVT	WQFN	RTV	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

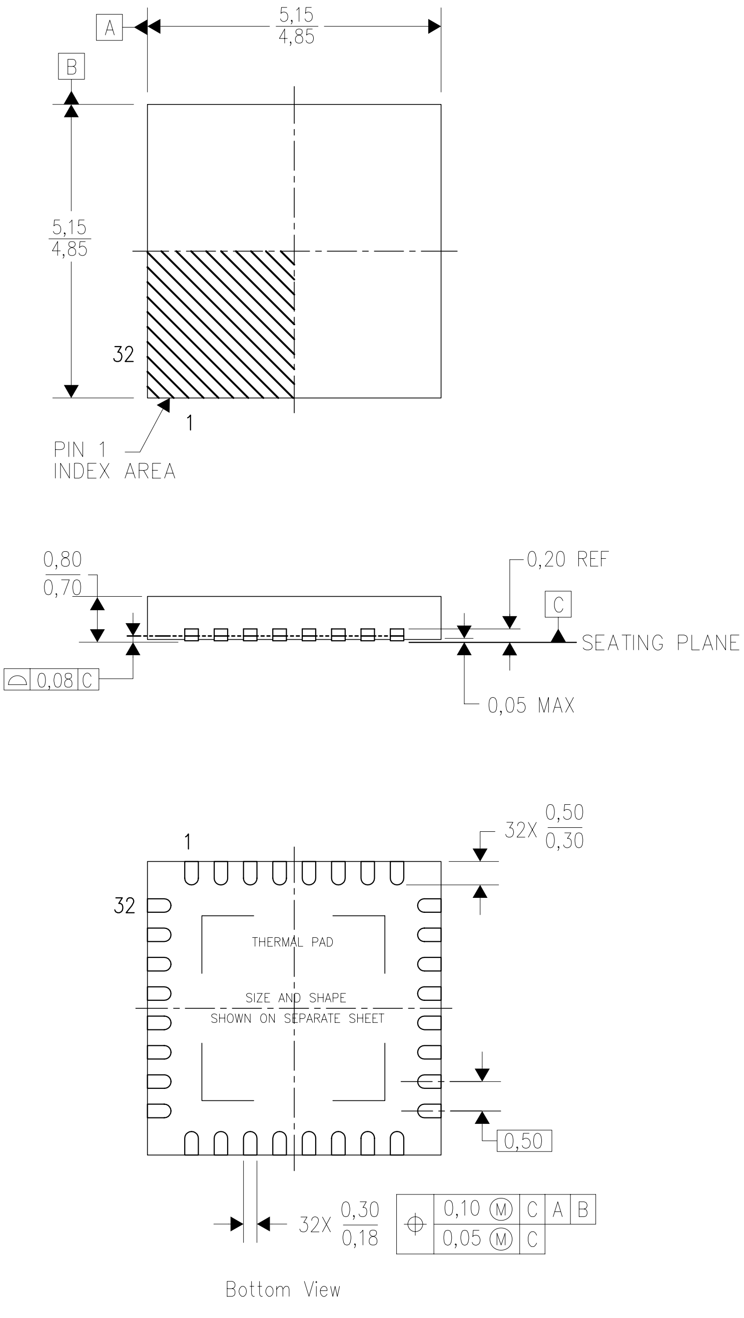
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51222RTVR	WQFN	RTV	32	3000	367.0	367.0	35.0
TPS51222RTVR	WQFN	RTV	32	3000	367.0	367.0	35.0
TPS51222RTVT	WQFN	RTV	32	250	210.0	185.0	35.0
TPS51222RTVT	WQFN	RTV	32	250	210.0	185.0	35.0

RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4206245/C 10/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–Leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–220.

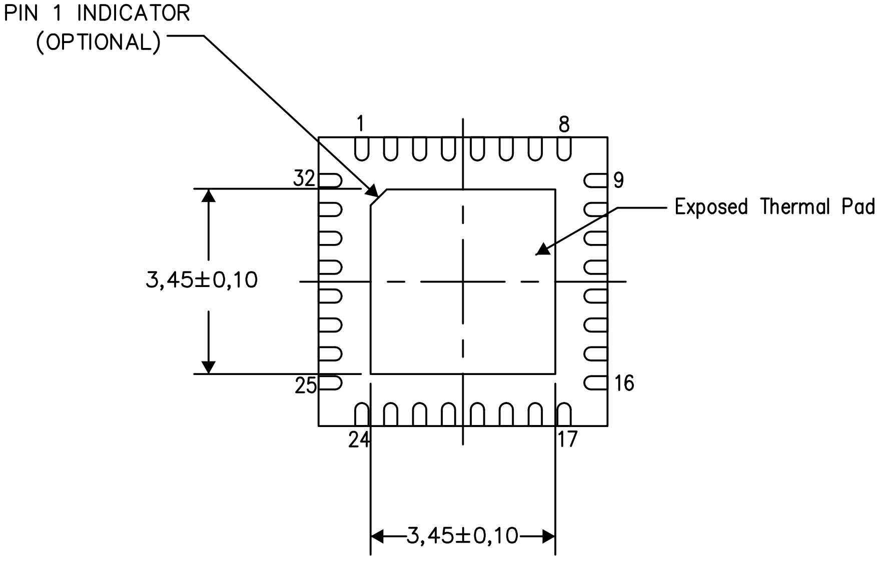
RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



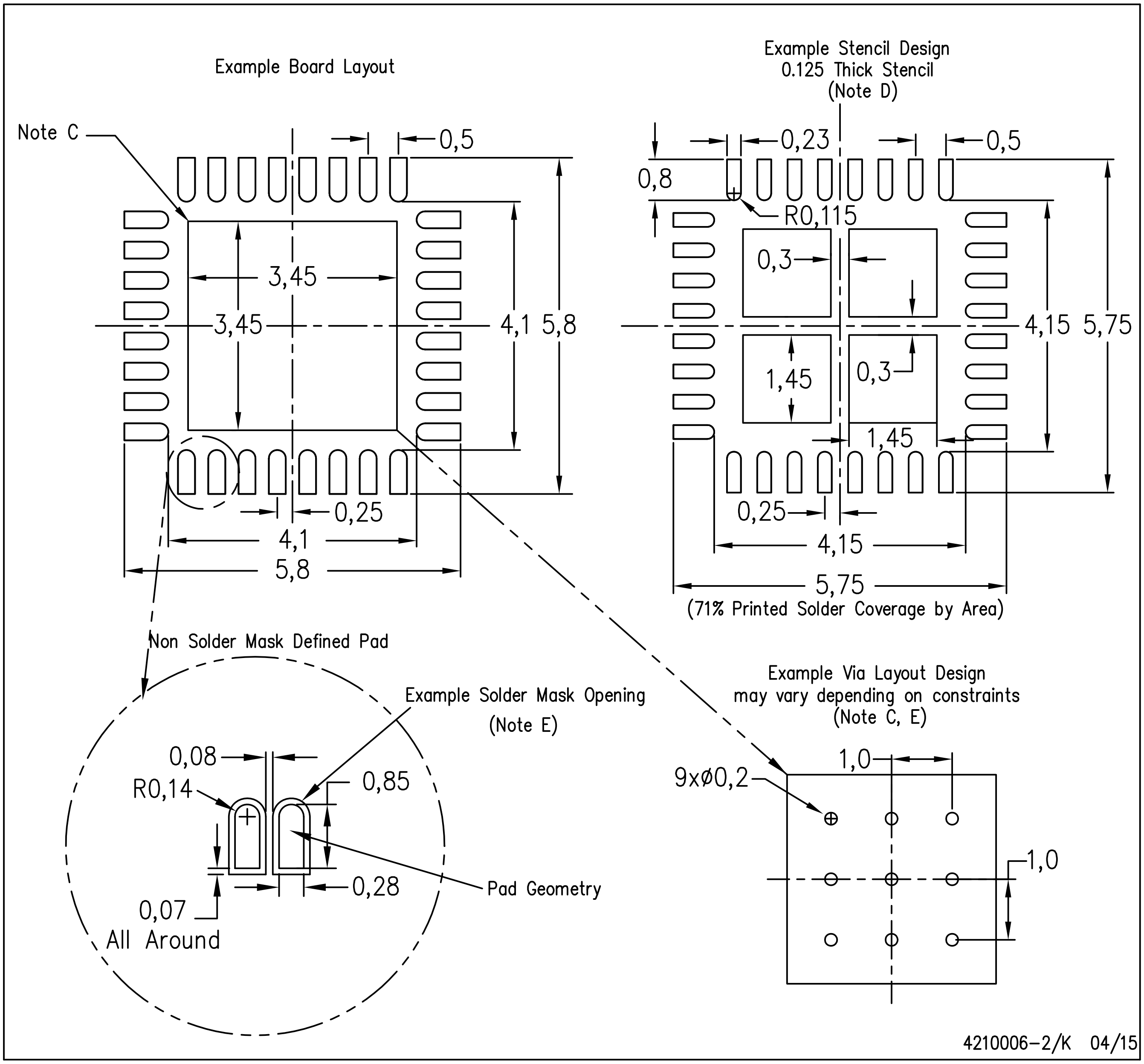
Bottom View

Exposed Thermal Pad Dimensions

4206250–2/Q 05/15

NOTE: All linear dimensions are in millimeters

RTV (S-PWQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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