TPS61181A White-LED Driver For Notebook Display

1 Features

- 4.5-V to 24-V Input Voltage
- 38-V Maximum Output Voltage
- Integrated 1.5-A/40-V MOSFET
- 1-MHz Switching Frequency
- Adaptive Boost Output to WLED Voltages
- Small External Components
- Integrated Loop Compensation
- Six Current Sinks of 30 mA
- Up to 10 WLED in Series
- 1% Typical Current Matching and Accuracy
- Up to 1000:1 PWM Brightness Dimming
- Minimized Output Ripple Under PWM Dimming
- Driver for Input/Output Isolation PFET
- True Shutdown
- Overvoltage Protection
- WLED Open and Short Protection
- Built-in Soft Start

2 Applications

- Notebook LCD Display Backlight
- UMPC LCD Display Backlight
- Backlight for Media Form Factor LCD Display

3 Description

The TPS61181A device provides highly integrated solutions for media-size LCD backlighting. The six current sink regulators provide high-precision current regulation and matching. In total, the device can support up to 60 WLEDs.

The devices support pulse width modulation (PWM) brightness dimming. During dimming, the WLED current is turned on/off at the duty cycle and frequency, determined by the PWM signal input to the DCRTL pin. The TPS61181A device is designed to minimize the output AC ripple across a wide dimming duty cycle and frequency range and also reduces the audible noise from the output ceramic capacitors.

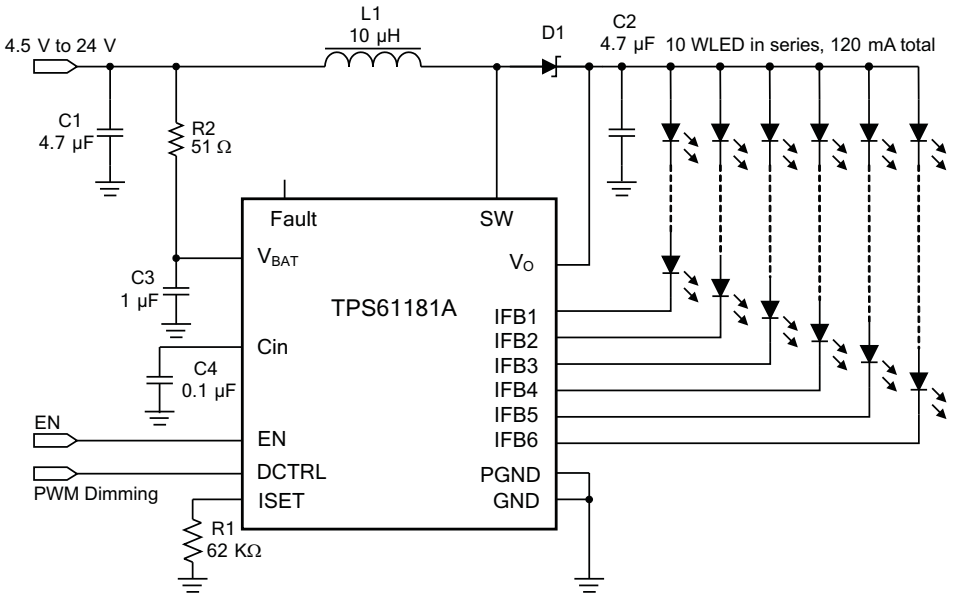
The TPS61181A device provides a driver output for an external PFET connected between the input and inductor. During short circuit or overcurrent conditions, the device turns off the external PFET and disconnects the battery from the WLEDs. The PFET is also turned off during device shutdown (thereby giving *true* shutdown) to prevent any leakage current from the battery. The device integrates overvoltage protection, soft-start and thermal shutdown and has a built-in linear regulator for the device supply.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61181A	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TPS61181A Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2011) to Revision B — **Page**

- Added *Device Information* and *Pin Configuration and Functions* sections, *Device Comparison and ESD Ratings* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; minor changes to page 1 to delete redundant content ... 1
- Deleted the *Ordering Information* table, see POA at the end of the data sheet ... 1

Changes from Original (February) to Revision A — **Page**

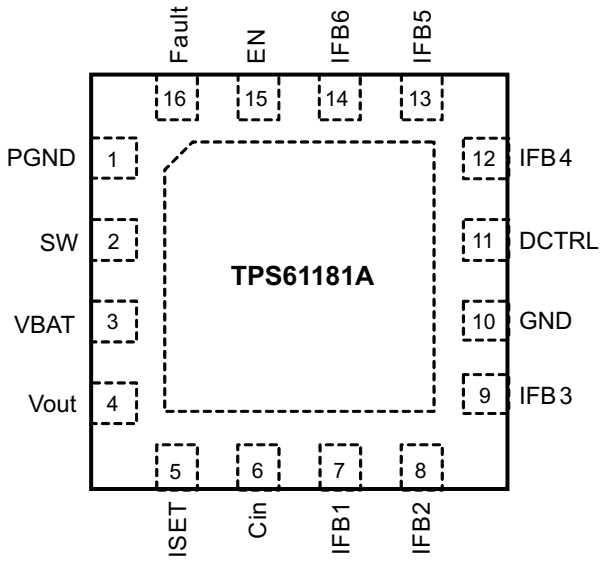
- Deleted Voltage Range spec for "all other pins" in the Absolute Maximum Ratings table. ... 4
- Added F_{PWM} spec. for PWM dimming frequency at $D_{PWM} \geq 1\%$ and $D_{PWM} \geq 5\%$ ... 4

5 Device Comparison Table

	TPS61181A	TPS61180
Input voltage range	5 V to 24 V	5 V to 24 V
Number of LED channels	6	6
LED current/channel	30	25
I2C/SPI support	No	No

6 Pin Configuration and Functions

RTE Package
16-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	PGND	I	Power ground of the device. Internally, it connects to the source of the PWM switch.
2	SW	I	This pin connects to the drain of the internal PWM switch, external Schottky diode and inductor.
3	V_{BAT}	I	This pin is connected to the battery supply. It provides the pullup voltage for the Fault pin and battery voltage signal. This is also the input to the internal LDO.
4	V_O	O	This pin monitors the output of the boost regulator. Connect this pin to the anode of the WLED strings.
5	ISET	I	The resistor on this pin programs the WLED output current.
6	Cin	I	Supply voltage of the device. It is the output of the internal LDO. Connect 0.1-μF bypass capacitor to this pin.
7, 8, 9 12, 13, 14	IFB1-IFB3 IFB4-IFB6	I	Current sink regulation inputs. They are connected to the cathode of WLEDs. The PWM loop regulates the lowest V_{IFB} to 400 mV. Each channel is limited to 30-mA current.
10	GND	I	Signal ground of the device.
11	DCTRL	I	Dimming control logic input. The dimming frequency range is 100 Hz to 1 kHz.
15	EN	I	The enable pin to the device. A logic high signal turns on the internal LDO and enables the device. Therefore, do not connect the EN pin to the Cin pin.
16	Fault	I	Gate driver output for an external PFET used for fault protection. It can also be used as signal output for system fault report.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage range(2)	V_{BAT} and Fault	–0.3	24	V
	C_{IN} and ISET	–0.3	3.6	
	SW and V_O	–0.3	40	
	IFB1 to IFB6, EN and DCTRL	–0.3	20	
Continuous power dissipation		See *Thermal Information*		
Operating junction temperature range		–40	150	°C
Storage temperature range		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	
		Machine mode (MM)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{BAT}	Battery input voltage range	4.5		24	V
V_O	Output voltage range	Vin		38	V
L	Inductor	4.7		10	µH
C_O	Output capacitor	2.2		10	µF
F_{PWM}	PWM dimming frequency at D_{PWM} ≥ 1%	0.1		1	kHz
	PWM dimming frequency at D_{PWM} ≥ 5%	1		5	
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS61181A RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.1	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	38.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.6	°C/W
$R_{\psi JT}$	Junction-to-top characterization parameter	0.4	°C/W
$R_{\psi JB}$	Junction-to-board characterization parameter	14.4	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

V_{BAT} = 10.8 V, 0.1 µF at Cin, EN = logic high, IFB current = 20 mA, IFB voltage = 500 mV, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{BAT}	Battery input voltage range		4.5		24	V
V_{cin}	Cin pin output voltage		2.7	3.15	3.6	V
I_{q_bat}	Operating quiescent current into V_{BAT}	Device enable, switching no load, V_{IN} = 24 V			3	mA
I_{Q_sw}	Operating quiescent current into V_O	V_O = 35 V			60	µA
I_{SD}	Shutdown current	EN=GND		2	18	µA
V_{bat_UVLO}	V_{BAT} undervoltage lockout threshold	V_{BAT} rising			4.45	V
		V_{BAT} falling	3.9			
V_{bat_hys}	V_{BAT} undervoltage lockout hysteresis	V_{BAT} rising – V_{BAT} falling		220		mV
EN AND DCTRL						
V_H	EN pin logic high voltage		2			V
V_L	EN pin logic low voltage				0.8	V
V_H	DCTRL pin logic high voltage		2			V
V_L	DCTRL pin logic low voltage				0.8	V
R_{PD}	Pulldown resistor on both pins	$V_{EN,\ DCTRL}$ = 2 V	400	800	1600	kΩ
CURRENT REGULATION						
V_{ISET}	ISET pin voltage		1.204	1.229	1.253	V
K_{ISET}	Current multiple Iout/ISET	ISET current = 20 µA	970	1000	1030	
IFB	Current accuracy	ISET current = 20 µA	19.4	20	20.6	mA
K_m	$(I_{max} – I_{min}) / I_{AVG}$	ISET current = 20 µA		1%	2.5%	
I_{leak}	IFB pin leakage current	IFB voltage = 20 V on all pins			3	µA
I_{IFB_MAX}	Current sink max output current	IFB = 500 mV	30			mA
BOOST OUTPUT REGULATION						
V_{IFB_L}	V_O dial up threshold	ISET current = 20 µA		400		mV
V_{IFB_H}	V_O dial down threshold	ISET current = 20 µA		700		mV
V_{reg_L}	Min V_O regulation voltage				16	V
V_{o_step}	V_O stepping voltage			100	150	mV
POWER SWITCH						
R_{PWM_SW}	PWM FET on-resistance			0.2	0.45	Ω
R_{start}	Start up charging resistance	V_O = 0 V	100		300	Ω
V_{start_r}	Isolation FET start-up threshold	$V_{IN} – V_O$, V_O ramp up		1.2	2	V
I_{LN_NFET}	PWM FET leakage current	V_{SW} = 35 V			1	µA

Electrical Characteristics (continued)

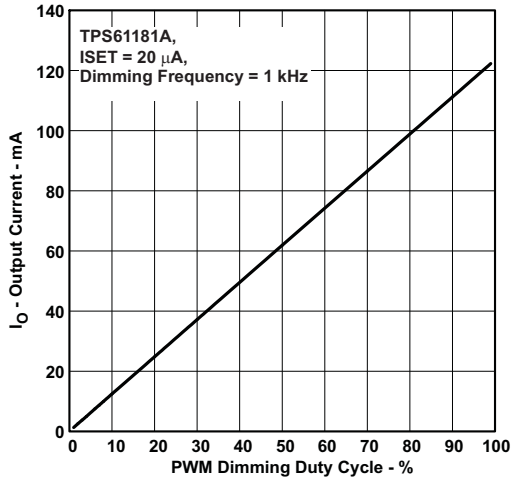
V_{BAT} = 10.8 V, 0.1 µF at Cin, EN = logic high, IFB current = 20 mA, IFB voltage = 500 mV, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
f_S	Oscillator frequency		0.9	1	1.2	MHz
D_{max}	Maximum duty cycle	IFB = 0 V		94%		
D_{min}	Minimum duty cycle				7%	
OS, SC, OVP AND SS						
I_{LIM}	N-channel MOSFET current limit	D = D_{max}	1.5		3	A
V_{ovp}	V_O overvoltage threshold	Measured on the V_O pin	38	39	40	V
V_{ovp_IFB}	IFB overvoltage threshold	Measured on the IFBx pin	15	17	20	V
V_{sc}	Short-circuit detection threshold	V_{IN} – V_O, V_O ramp down		1.7	2.5	V
V_{sc_dly}	Short-circuit detection delay during start up			32		ms
FAULT OUTPUT						
V_{fault_high}	Fault high voltage	Measured as V_{BAT} – V_{Fault}		0.1		V
V_{fault_low}	Fault low voltage	Measured as V_{BAT} – V_{Fault}, sink 0.1 mA V_{IN} = 15 V	6	8	10	V
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
$T_{hysteresis}$	Thermal shutdown threshold hysteresis			15		°C

7.6 Typical Characteristics

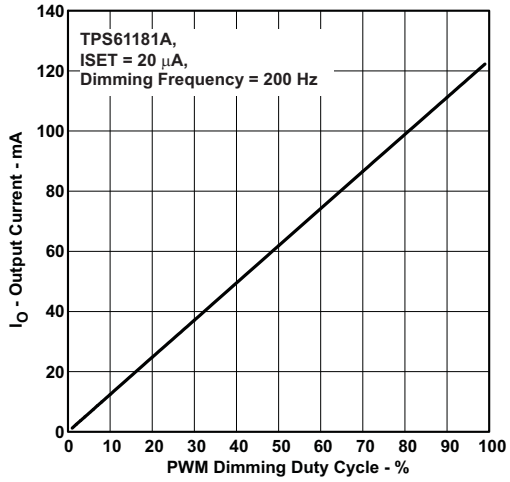
Table 1. Table of Graphs

Description (Reference to application circuit in Figure 16)		Figure
Dimming Linearity	V_{bat} = 10.8 V; V_O=28.6 V, 9 LEDs; I_{set}= 20 µA; PWM Freq = 1 kHz	Figure 1
Dimming Linearity	V_{bat} = 10.8 V; V_O=28.6 V, 9 LEDs; I_{set}= 20 µA; PWM Freq = 200 Hz	Figure 2
Output Ripple	V_O = 28.6 V; I_{set}= 20 µA; PWM Freq = 200 Hz; Duty = 50%	Figure 3
Switching Waveform	V_{bat} = 10.8 V; I_{set}= 20µA	Figure 4
Output Ripple at PWM Dimming	V_{bat} = 10.8 V; I_{set} = 20 µA; PWM Freq = 200 Hz; Duty = 50%; C_O = 4.7 µF	Figure 5
Short Circuit Protection	V_{bat} = 10.8 V; I_{set} = 20 µA	Figure 6
Open WLED Protection	V_{bat} = 10.8 V; I_{set} = 20 µA	Figure 7
Startup Waveform	V_{bat} = 10.8 V; I_{set} = 20 µA	Figure 8
DC Load Efficiency	V_{bat} = 5 V, 10.8 V, 19 V; V_O = 28.6 V, 9 LEDs; L = 10 µH	Figure 10
DC Load Efficiency	V_{bat} = 5V, 10.8 V, 19 V; V_O = 31.7 V, 10 LEDs; L =10 µH	Figure 11
PWM Dimming Efficiency	V_{bat} = 5V, 10.8 V and 19 V; V_O = 25.5 V, 8 LEDs; PWM Freq = 1 kHz	Figure 12
PWM Dimming Efficiency	V_{bat} = 5V, 10.8 V and 19 V; V_O = 28.6 V, 9 LEDs; PWM Freq = 1 kHz	Figure 13
PWM Dimming Efficiency	V_{bat} = 5V, 10.8 V and 19 V; V_O = 31.7 V, 10 LEDs; PWM Freq = 1 kHz	Figure 14
PWM Dimming Efficiency	V_{bat} = 5V, 10.8 V and 19 V; V_O=34.8 V, 11 LEDs; PWM Freq = 1 kHz	Figure 15



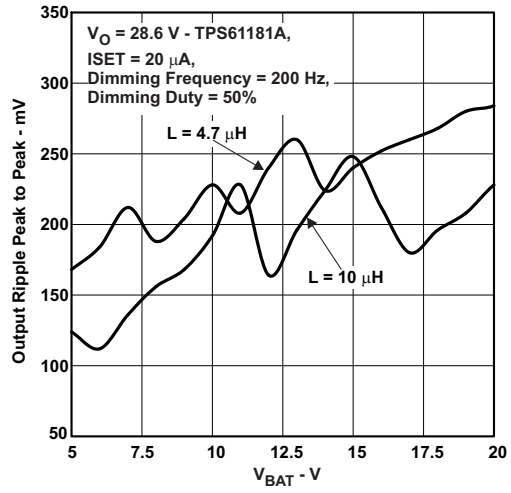
1 kHz

Figure 1. PWM Dimming Linearity



200 Hz

Figure 2. PWM Dimming Linearity



C_{OUT} = 4.7 µF

Figure 3. PWM Dimming Output Ripple vs Input Voltage

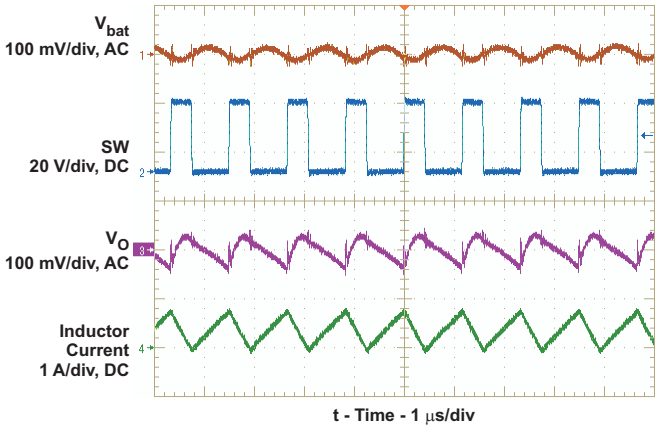
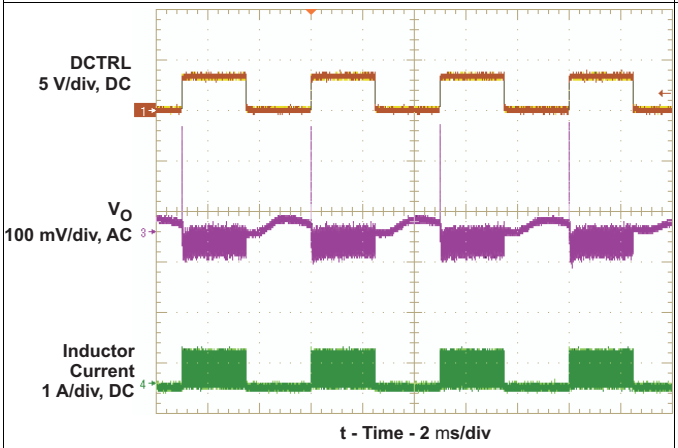


Figure 4. Switching Waveform



C_{OUT} = 4.7 µF

Figure 5. Output Ripple at PWM Dimming

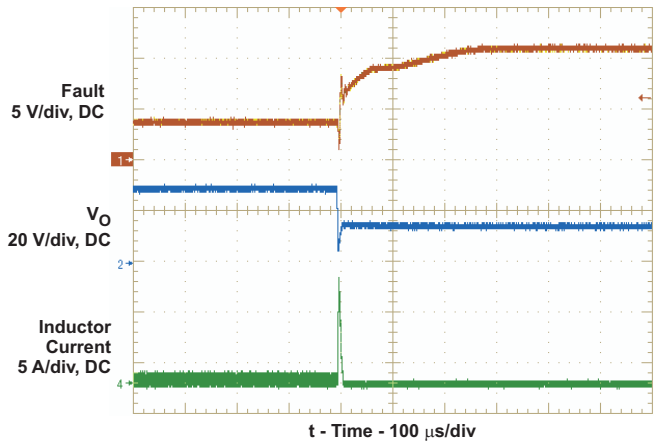


Figure 6. Output Short Protection

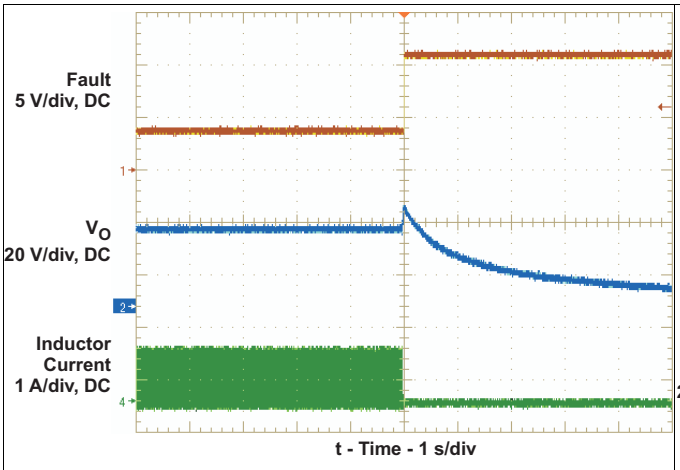


Figure 7. Open WLED Protection

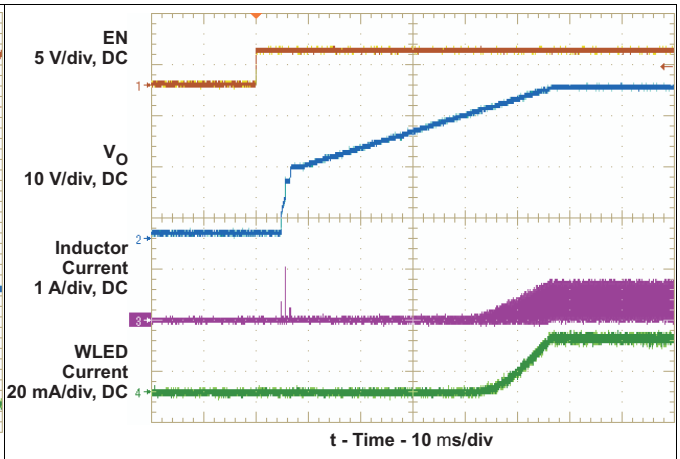


Figure 8. Start-up Waveform

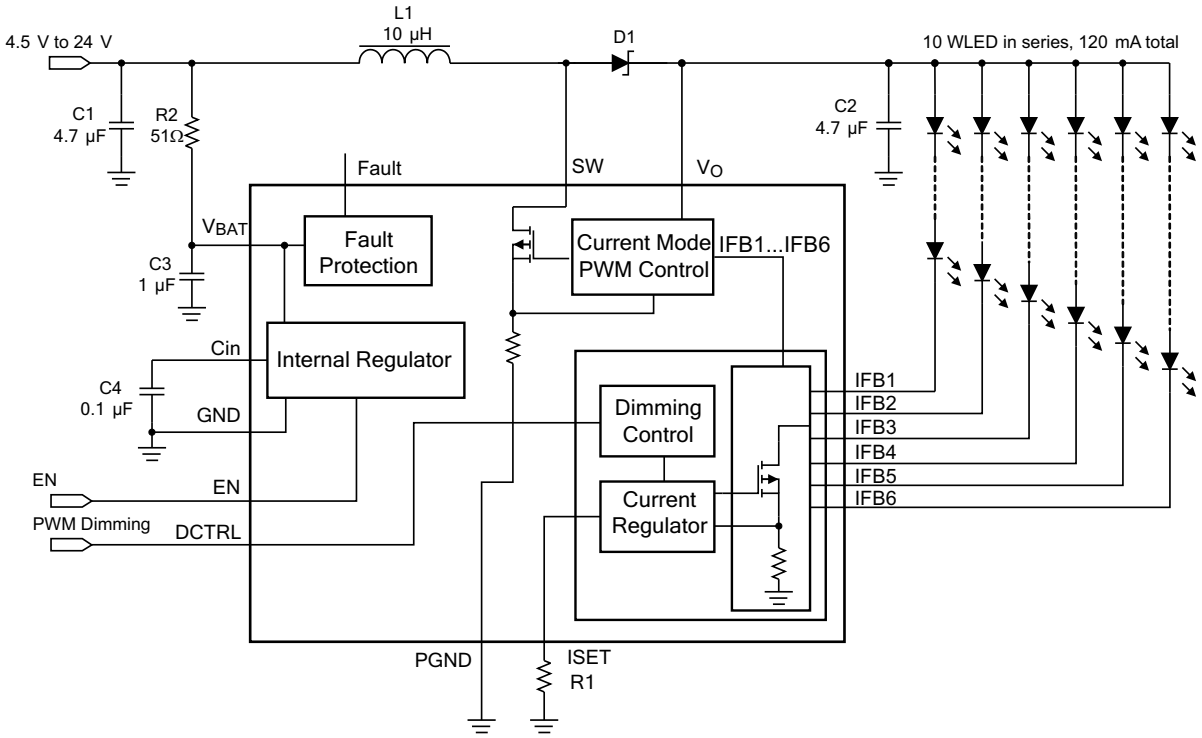
8 Detailed Description

8.1 Overview

Recently, WLEDs have gained popularity as an alternative to CCFL for backlighting media-size LCD displays. The advantages of WLEDs are power efficiency and low profile design. Due to the large number of WLEDs, they are often arranged in series and parallel, and powered by a boost regulator with multiple current sink regulators. Having more WLEDs in series reduces the number of parallel strings and therefore improves overall current matching. However, the efficiency of the boost regulator declines due to the need for high output voltage. Also, there have to be enough WLEDs in series to ensure the output voltage stays above the input voltage range. Otherwise, a buck-boost (for example, SEPIC) power converter has to be adopted which could be more expensive and complicated.

The TPS61181A device has integrated all the key function blocks to power and control up to 60 WLEDs. The devices include a 40-V/1.5-A boost regulator, six 30-mA current sink regulators and protection circuit for overcurrent, overvoltage, and short-circuit failures. The key advantages of the devices are small solution size, low output AC ripple during PWM dimming control, and the capability to isolate the input and output during fault conditions.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Supply Voltage

The TPS61181A has built-in LDO linear regulator to supply the device analog and logic circuits. The LDO is powered up when the EN pin is high. The output of the LDO is connected to the Cin pin. A 0.1-μF bypass capacitor is required for stable operation of the LDO. Do not connect the Cin pin to the EN pin because this prevents the device from starting up. In addition, avoid connecting the Cin pin to any other circuit as this could introduce noise into the device supply voltage.

The V_{BAT} connects to the input of the internal LDO, and powers the device. The voltage on the V_{BAT} pin is also the reference for the pull-up circuit of the Fault pin. In addition, it serves as the input signal to the short-circuit protection. There is an undervoltage lockout on the V_{BAT} pin which disables the device when its voltage reduces to 4.2 V (typical). The device restarts when the V_{BAT} pin voltage recovers by 220 mV.

8.3.2 Boost Regulator

The boost regulator is controlled by current mode PWM, and loop compensation is integrated inside the device. The internal compensation ensures stable output over the full input and output voltage range. The TPS61181A switches at 1 MHz which optimize boost converter efficiency and voltage ripple with a small form factor inductor and output capacitor.

The output voltage of the boost regulator is automatically set by the device to minimize the voltage drop across the IFB pins. The device automatically regulates the lowest IFB pin to 400 mV, and consistently adjusts the boost output voltage to account for any changes of the LED forward voltages.

When the output voltage is too close to the input, the boost regulator may not be able to regulate the output due to the limitation of minimum duty cycle. In this case, increase the number of WLED in series or include series ballast resistors in order to provide enough headroom for the boost operation.

The TPS61181A boost regulator cannot regulate its output to voltages below 15 V.

8.3.3 Enable and Start-Up

A logic high signal on the EN pin turns on the device. For the TPS61181A, taking EN high turns on the internal LDO linear regulator which provides supply to the device current. Then, an internal resistor, R_{start} (start up charging resistor) is connected between the V_{BAT} pin and V_O pin to charge the output capacitor toward the V_{BAT} pin voltage. The Fault pin outputs high during this time, and thus the external isolation PFET is turned off. Once the V_O pin voltage is within 2 V (isolation FET start up threshold) of the V_{BAT} pin voltage, R_{start} is open, and the Fault pin pulls down the gate of the PFET and connects the V_{BAT} voltage to the boost regulator. This operation is to prevent the in-rush current due to charging the output capacitor.

Once the isolation FET is turned on, the device starts PWM switching to raise the output voltage above V_{BAT}. Soft-start is implemented by gradually ramping up the reference voltage of the error amplifier to prevent voltage overshoot and in-rush current. See the start-up waveform of a typical example, Figure 8.

Pulling the EN pin low immediately shuts down the device, resulting in the device consuming less than 50 μA in the shutdown mode.

8.3.4 Overcurrent, Overvoltage, and Short-Circuit Protection

The TPS61181A has pulse-by-pulse over-current limit of 1.5 A (minimum). The PWM switch turns off when the inductor current reaches this current threshold. The PWM switch remains off until the beginning of the next switching cycle. This protects the device and external components under overload conditions. When there is sustained over-current condition for more than 16 ms (under 100% dimming duty cycle), the device turns off and requires POR or the EN pin toggling to restart.

Under severe overload and/or short circuit conditions, the V_O pin can be pulled below the input (V_{BAT} pin). Under this condition, the current can flow directly from V_{BAT} to the WLED through the inductor and schottky diode. Turning off the PWM switch alone does not limit current anymore. In this case, the TPS61181A detects the output voltage is 1.7 V (V_{sc},short circuit detection threshold) below the input voltage, turns off the isolation FET, and shuts down the device. The device restarts after input power-on reset (V_{BAT} POR) or EN pin logic toggling.

Feature Description (continued)

During device start up, if there is short-circuit condition on the boost converter output, the output capacitor will not be charged to within 2 V of V_{BAT} through R_{start}. After 32 ms (V_{sc_dly}short circuit detection delay during start-up), the TPS61181A shuts down and does not restart until there is V_{BAT} POR or EN pin toggling. The isolation FET is never turned on under the condition.

If one of the WLED strings is open, the boost output rises to overvoltage threshold (39V typical). The TPS61181A detects the open WLED string by sensing no current in the corresponding IFB pin. As a result, the device removes the open IFB pin from the voltage feedback loop. Subsequently, the output voltage drops down and is regulated to a voltage for the connected WLED strings. The IFB current of the connected WLED strings keep in regulation during the whole transition. The device only shuts down if it detects that all of the WLED strings are open.

If the overvoltage threshold is reached, but the current sensed on the IFB pin is below the regulation target, the device regulates the boost output at the overvoltage threshold. This operation could occur when the WLED is turned on under cold temperature, and the forward voltages of the WLEDs exceed the overvoltage threshold. Maintaining the WLED current allows the WLED to warm up and their forward voltages to drop below the over-voltage threshold.

If any IFB pin voltage exceeds IFB overvoltage threshold (17 V typical), the device turns off the corresponding current sink and removes this IFB pin from V_O regulation loop. The current regulation of the remaining IFB pins is not affected. This condition often occurs when there are several shorted WLEDs in one string. WLED mismatch typically does not create such large voltage difference among WLED strings.

8.3.5 IFB Pin Unused

If the application requires less than 6 WLED strings, one can easily disable unused IFB pins. The TPS61181A simply requires leaving the unused IFB pin open or shorting it to ground. If the IFB pin is open, the boost output voltage ramps up to V_O overvoltage threshold during start up. The device then detects the zero current string, and removes it from the feedback loop. If the IFB pin is shorted to ground, the device detects the short immediately after device enable, and the boost output voltage does not go up to V_O overvoltage threshold. Instead, it ramps to the regulation voltage after soft start.

8.4 Device Functional Modes

8.4.1 Current Program and PWM Dimming

The six current sink regulators can each provide a maximum of 30 mA. The IFB current must be programmed to maximum WLED current using the ISET pin resistor and Equation 1.

$$I_{FB} = K_{ISET} \frac{V_{ISET}}{R_{ISET}} \quad (1)$$

where

- K_{ISET} = Current multiple (1000 typical)
- V_{ISET} = ISET pin voltage (1.229 V typical)
- R_{ISET} = ISET pin resistor

The TPS61181A has six built-in precise current sink regulators. The current matching among the current sinks at 20-mA current through is below 2.5%. This means the differential value between the maximum and minimum current of the six current sinks divided by the average current of the six is less than 2.5%.

The WLED brightness is controlled by the PWM signal on the DCTRL pin. The frequency and duty cycle of the DCTRL signal is replicated on the IFB pin current. Keep the dimming frequency in the range of 100 Hz to 1 kHz to avoid screen flickering and maintain dimming linearity. Screen flickering may occur if the dimming frequency is below the range. The minimum achievable duty cycle increases with the dimming frequency. For example, while a 0.1% dimming duty cycle, giving a 1000:1 dimming range, is achievable at 100 Hz dimming frequency, only 1% duty cycle, giving a 100:1 dimming range, is achievable with a 1-KHz dimming frequency, and 5% dimming duty cycle is achievable with 5-KHz dimming frequency. The device could work at high dimming frequency like 20 KHz, but then only 15% duty cycle could be achievable. The TPS61181A is designed to minimize the AC ripple on the output capacitor during PWM dimming. Careful passive component selection is also critical to minimize AC ripple on the output capacitor. See *Application and Implementation* for more information.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS61176 provides a high-performance LED lighting solution for tablets, notebooks and other low power LCD backlit displays. The device can drive 6 strings of 10 series LEDs in a compact and high efficient solution. The LED current is controlled via a logic level PWM input and the LED current level is set using an ISET resistor.

9.2 Typical Application

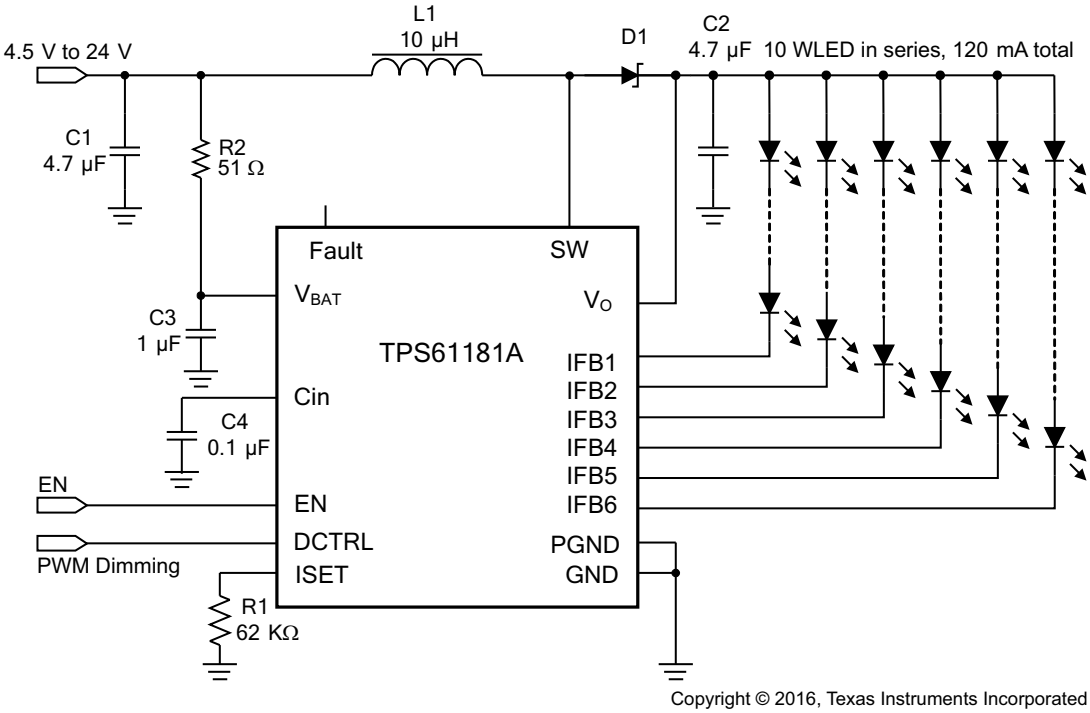


Figure 9. TPS61181A Typical Application

9.2.1 Design Requirements

For typical LED driver applications, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	4.5 V
Output voltage	Vin to 38 V
Current accuracy	20 mA (typical)
Oscillator frequency	1 MHz (typical)

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

Because the selection of the inductor affects the steady-state operation of a power supply, transient behavior and loop stability, the inductor is the most important component in switching power regulator design. There are three specifications most important to the performance of the inductor: inductor value, DC resistance, and saturation current. The TPS61181A device is designed to work with inductor values between 4.7 μH and 10 μH. A 4.7-μH inductor may be available in a smaller or lower profile package, while 10 μH may produce higher efficiency due to lower inductor ripple. If the boost output current is limited by the overcurrent protection of the device, using a 10-μH inductor can offer higher output current.

The internal loop compensation for the PWM control is optimized for the recommended component values, including typical tolerances. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20 to 35% from the zero current value depending on how the inductor vendor defines saturation

In a boost regulator, the inductor DC current can be calculated as:

$$I_{dc} = \frac{V_O \times I_O}{V_{in} \times \eta}$$

where

- V_O = boost output voltage
- Io = boost output current
- V_{in} = boost input voltage
- η = power conversion efficiency, use 90% for TPS61181A applications (2)

The inductor current peak-to-peak ripple can be calculated as:

$$I_{pp} = \frac{1}{L \times \left(\frac{1}{V_O - V_{bat}} + \frac{1}{V_{bat}} \right) \times F_S}$$

where

- I_{pp} = inductor peak-to-peak ripple
- L = inductor value
- F_s= switching frequency
- V_{bat}= boost input voltage (3)

Therefore, the peak current seen by the inductor is

$$I_p = I_{dc} + \frac{I_{pp}}{2} \quad (4)$$

Select the inductor with saturation current at least 25% higher than the calculated peak current. To calculate the worse case inductor peak current, use minimum input voltage, maximum output voltage and maximum load current.

Regulator efficiency is dependent on the resistance of its high current path, switching losses associated with the PWM switch and power diode. Although the TPS61181A device have optimized the internal switch resistance, the overall efficiency still relies on the DC resistance (DCR) of the inductor; lower DCR improves efficiency. However, there is a trade off between DCR and inductor footprint. Furthermore, shielded inductors typically have a higher DCR than unshielded ones. Table 3 lists recommended inductor models.

Table 3. Recommended Inductors for TPS61181A

	L (μH)	DCR TYPICAL (mΩ)	I_{sat} (A)	SIZE (L×W×H mm)
TOKO				
A915AY-4R7M	4.7	38	1.87	5.2 × 5.2 × 3
A915AY-100M	10	75	1.24	5.2 × 5.2 × 3
TDK				
SLF6028T-4R7M1R6	4.7	28.4	1.6	6 × 6 × 2.8
SLF6028T-100M1R3	10	53.2	1.3	6 × 6 × 2.8

9.2.2.2 Output Capacitor Selection

During PWM brightness dimming, the load transient causes voltage ripple on the output capacitor. Since the PWM dimming frequency is in the audible frequency range, the ripple can produce audible noises on the output ceramic capacitor. There are two ways to reduce or eliminate this audible noise. The first option is to select PWM dimming frequency outside the audible range. This means the dimming frequency needs be to lower than 200 Hz or higher than 30 KHz. The potential issue with a very low dimming frequency is that WLED on/off can become visible and thus cause a flickering effect on the display. On the other hand, high dimming frequency can compromise the dimming range since the LED current accuracy and current match are difficult to maintain at low dimming duty cycle. The second option is to reduce the amount of the output ripple, and therefore minimize the audible noise.

The TPS61181A adopts a patented technology to limit output ripple even with small output capacitance. In a typical application, the output ripple is less than 200 mV during PWM dimming with a 4.7-μF output capacitor, and the audible noise is not noticeable. The devices are designed to be stable with output capacitor down to 1 μF. However, the output ripple will increase with lower output capacitor.

Care must be taken when evaluating the derating of a ceramic capacitor due to applied dc voltage, aging and over frequency. For example, larger form factor capacitors (in 1206 size) have their self resonant frequencies in the switching frequency range of the TPS61181A. So the effective capacitance is significantly lower. Therefore, it may be necessary to use small capacitors in parallel instead of one large capacitor.

9.2.2.3 Audible Noise Reduction

Ceramic capacitors can produce audible noise if the frequency of its AC voltage ripple is in the audible frequency range. In TPS61181A applications, both input and output capacitors are subject to AC voltage ripple during PWM brightness dimming. The device integrates a patented technology to minimize the ripple voltage, and thus audible noises.

To further reduce the audible noise, one effective way is to use two or three small size capacitors in parallel instead of one large capacitor. The application circuit in Figure 16 uses two 2.2-μF/25-V ceramic capacitors at the input and two 1-μF/50-V ceramic capacitors at the output. All of the capacitors are in 0805 package. Although the output ripple during PWM dimming is higher than with one 4.7 μF in a 1206 package, the overall audible noise is lower.

In addition, connecting a 10-nF/50V ceramic capacitor between the V_O pin and IFB1 pin can further reduce the output AC ripple during the PWM dimming. Since this capacitor is subject to large AC ripple, choose a small package such as 0402 to prevent it from producing noise.

9.2.2.4 Isolation MOSFET Selection

The TPS61181A provides a gate driver to an external P-channel MOSFET which can be turned off during device shutdown or fault condition. This MOSFET can provide a true shutdown function, and also protect the battery from output short circuit conditions. The source of the PMOS must be connected to the input, and a pullup resistor is required between the source and gate of the FET to keep the FET off during device shutdown. To turn on the isolation FET, the Fault pin is pulled low, and clamped at 8 V below the V_{BAT} pin voltage.

During device shutdown or fault condition, the isolation FET is turned off, and the input voltage is applied on the isolation MOSFET. During a short circuit condition, the catch diode (D2 in typical application circuit) is forward biased when the isolation FET is turned off. The drain of the isolation FET swings below ground. The voltage across the isolation FET can be momentarily greater than the input voltage. Therefore, select a 30-V MOSFET for a 24-V maximum input. The on resistance of the FET has a large impact on power conversion efficiency since the FET carries the input voltage. Select a MOSFET with $R_{ds(on)}$ less than 100 mΩ to limit the power losses.

9.2.3 Application Curves

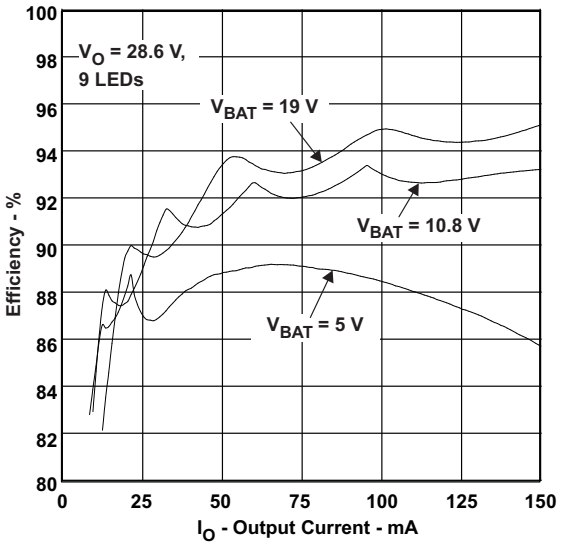


Figure 10. Efficiency vs Output Current

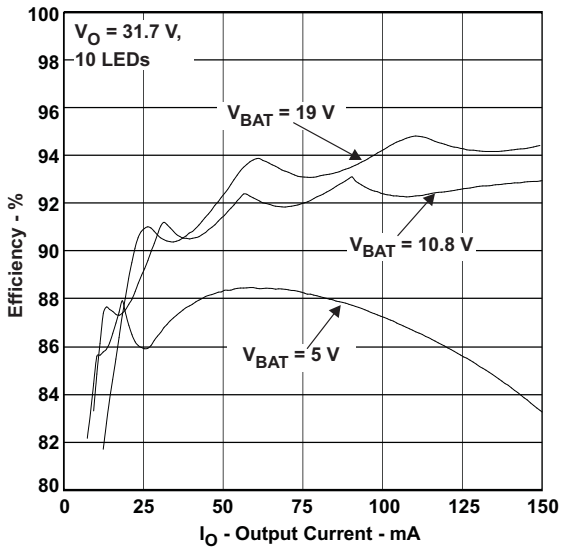


Figure 11. Efficiency vs Output Current

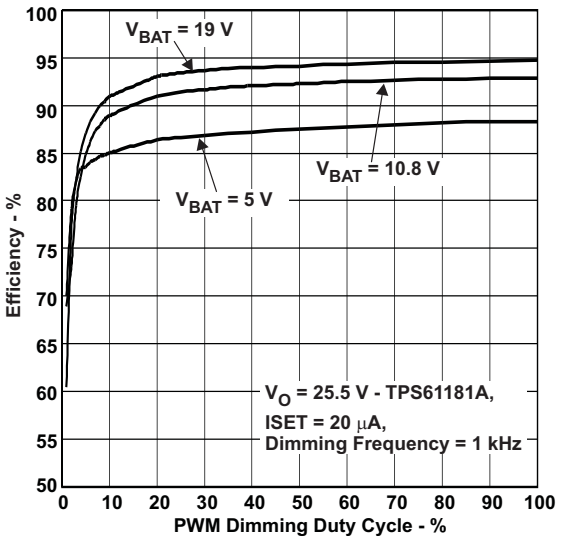


Figure 12. Efficiency vs Dimming Duty Cycle

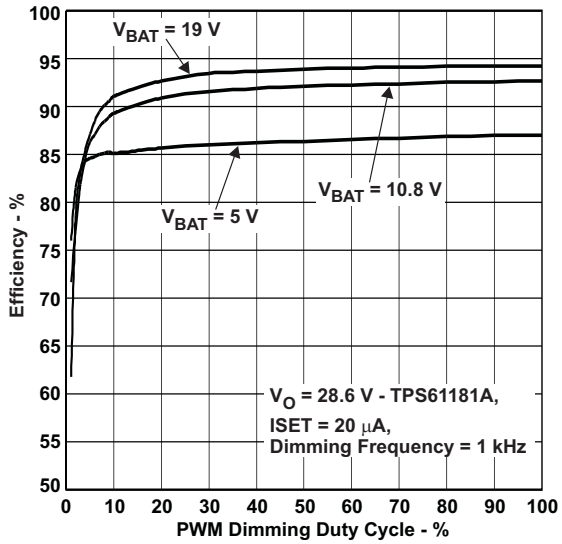


Figure 13. Efficiency vs Dimming Duty Cycle

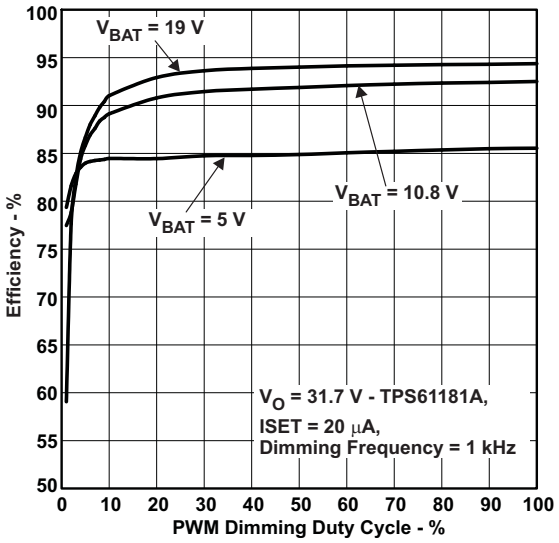


Figure 14. Efficiency vs Dimming Duty Cycle

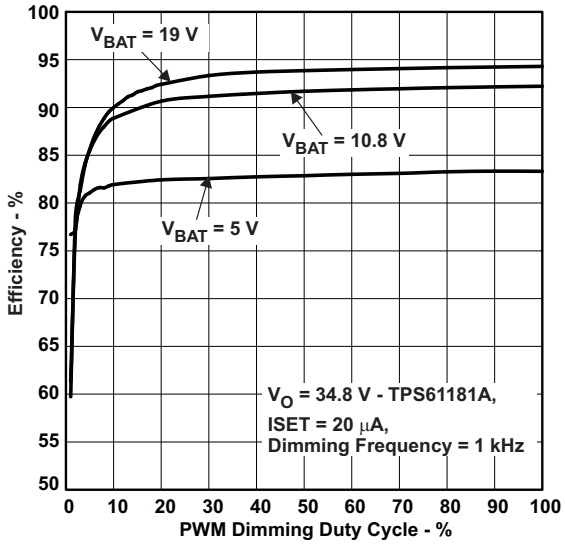
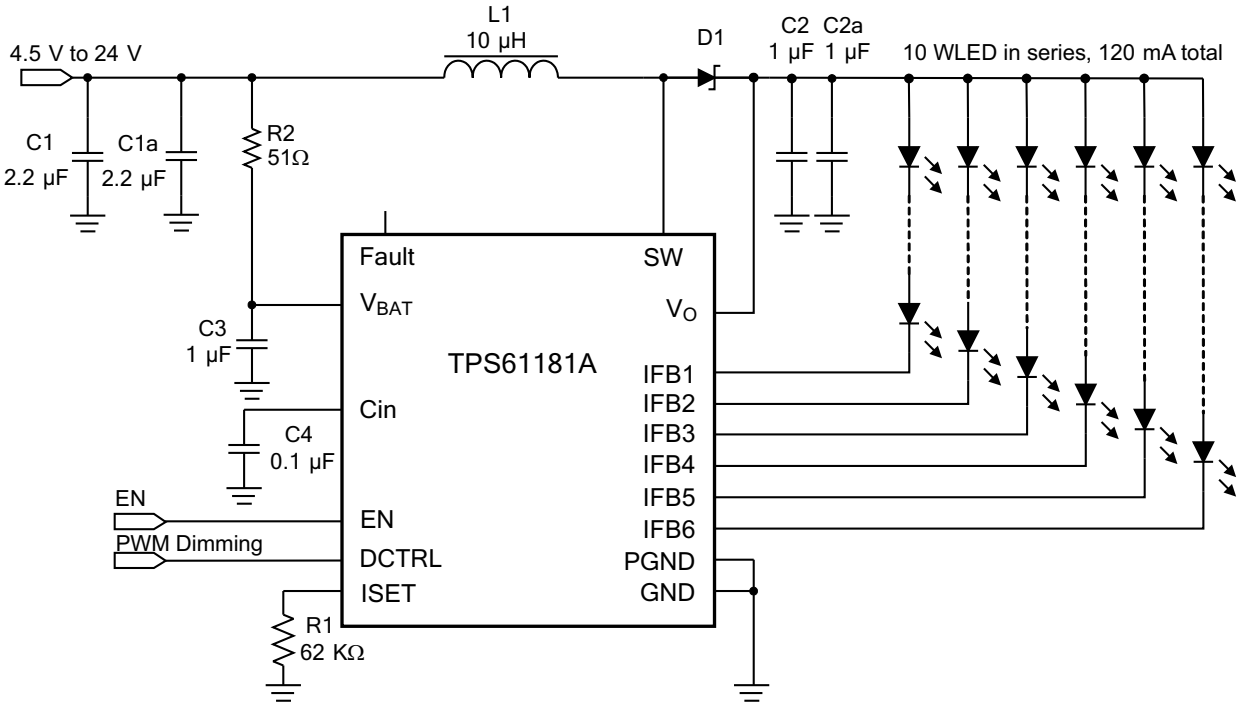


Figure 15. Efficiency vs Dimming Duty Cycle

9.3 Additional Application Circuits



C1, C1a: Murata GRM 219R61E225K
C2, C2a: Murata GRM 21BR71H105K
C3: Murata GRM 21BR71H105K
C4: Murata GRM 185R61A105K

L1: TOKO A 915AY-100 M
D1: VISHAY SS 2P5-E3/84A

Figure 16. Audible Noise-Reduction Circuit

Additional Application Circuits (continued)

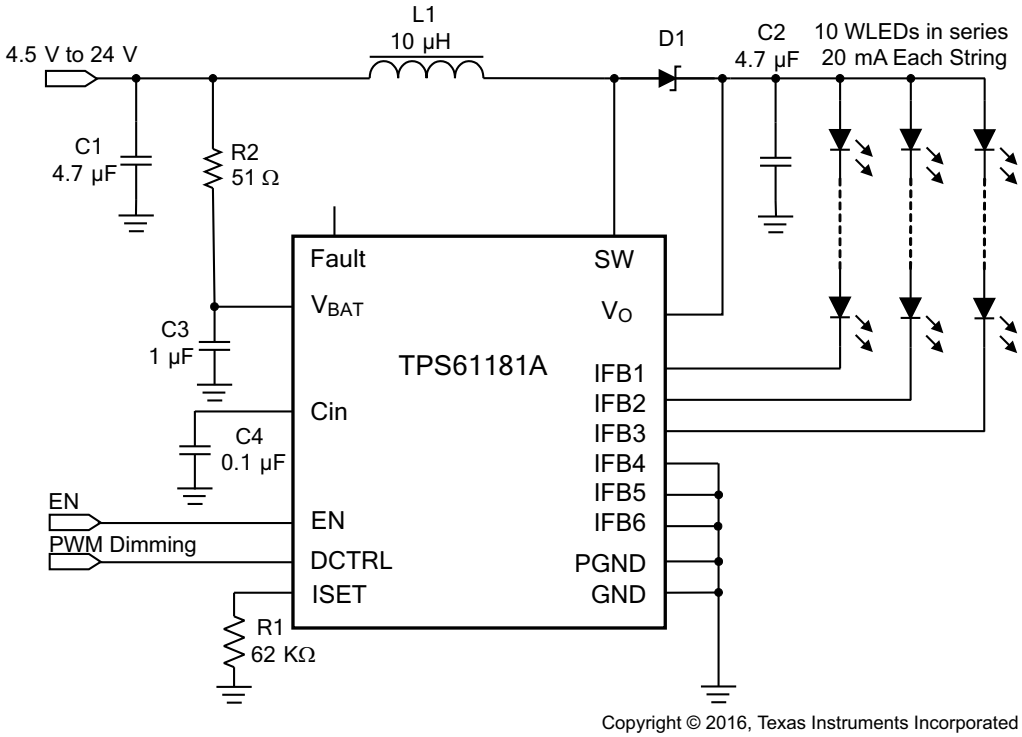


Figure 17. TPS61181A for Three Strings of LEDs

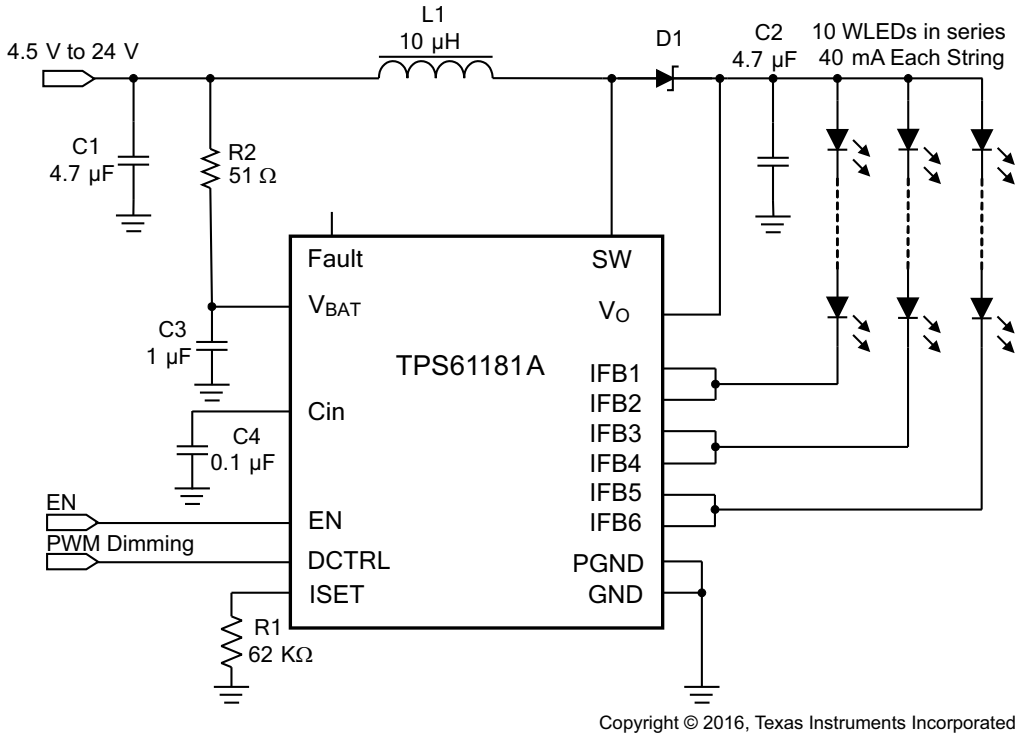


Figure 18. TPS61181A for Three Strings of LEDs With Double Current

Additional Application Circuits (continued)

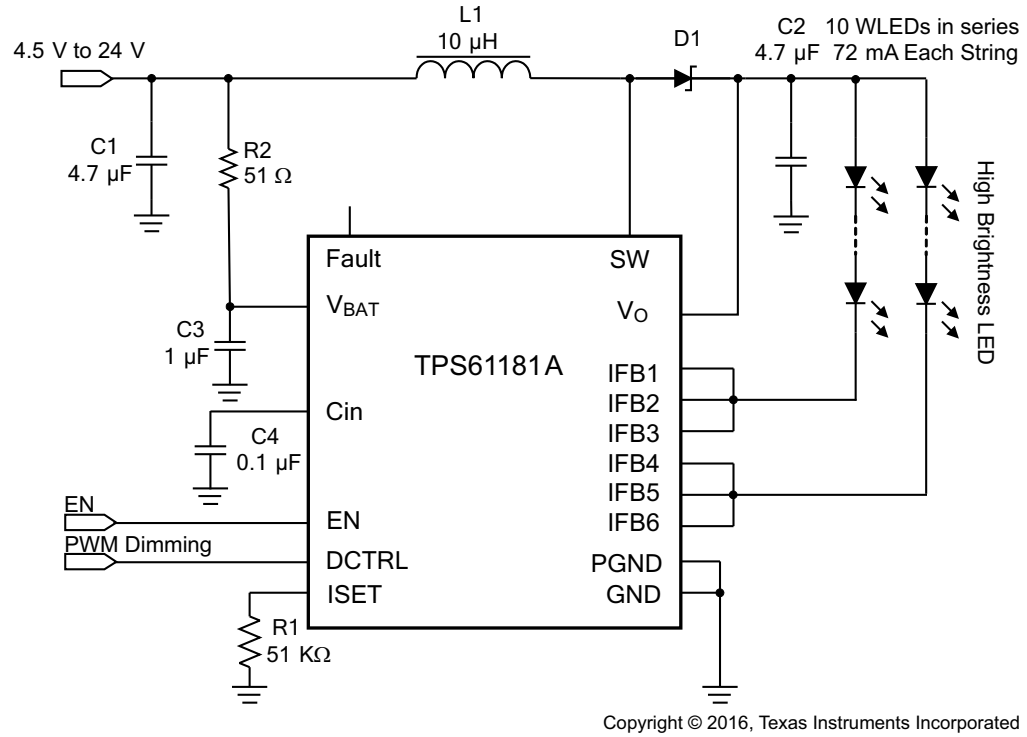


Figure 19. TPS61181A for Two Strings, High-Brightness LEDs Application

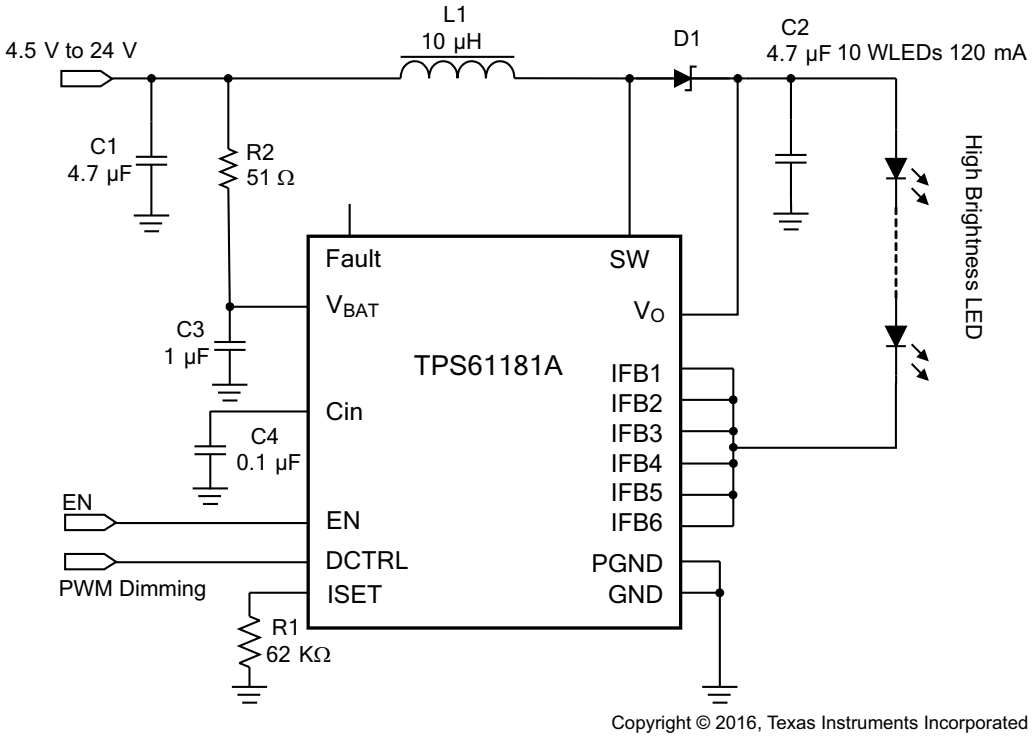


Figure 20. TPS61181A for One-String, High-Brightness LED Application

Additional Application Circuits (continued)

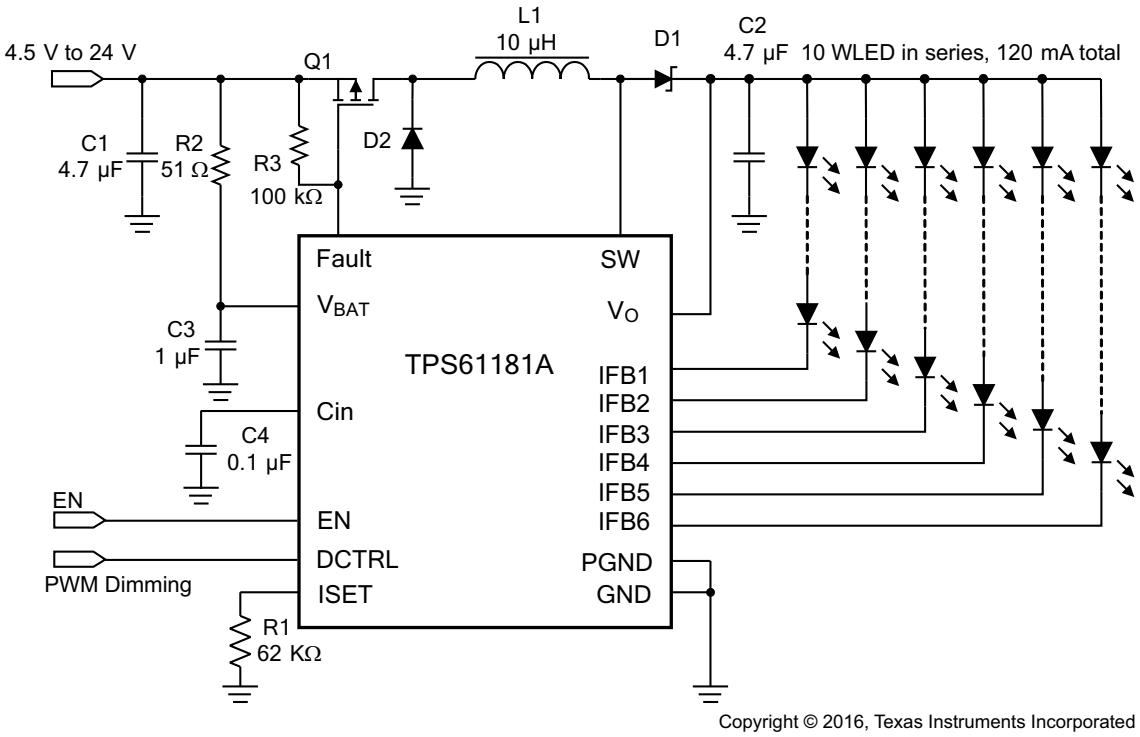


Figure 21. TPS61181A Driving External PFET for True Shutdown Application

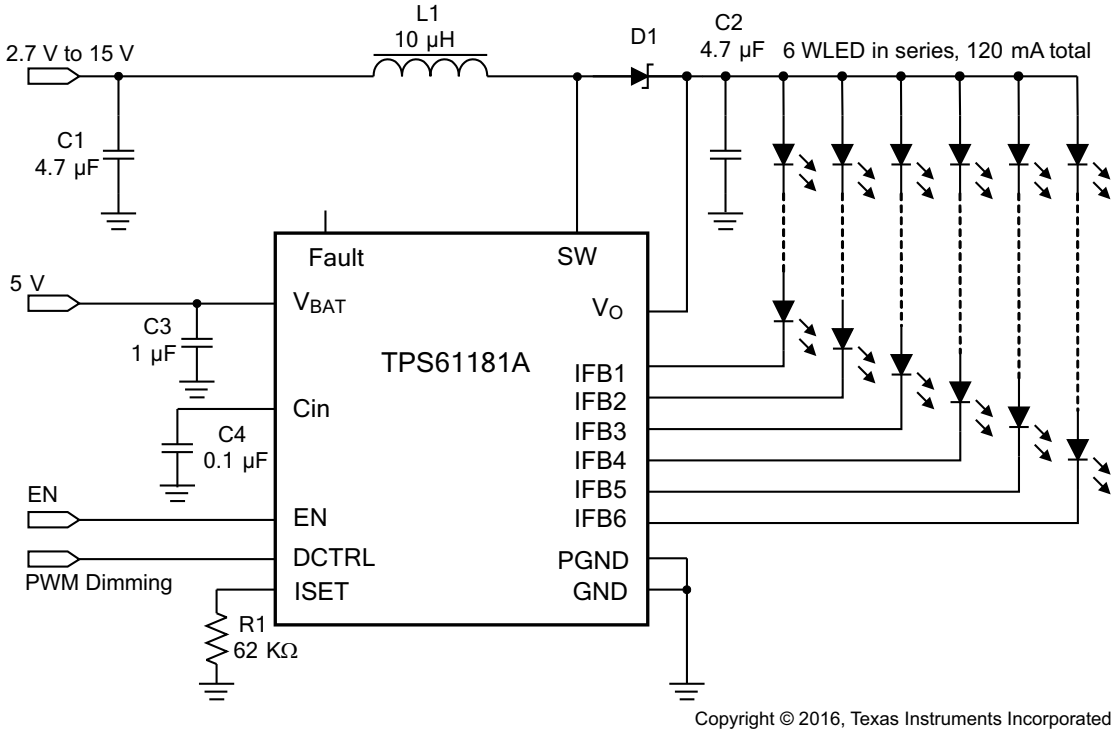


Figure 22. TPS61181A With Separate V_{BAT} Power for Low Voltage-Input Application

Additional Application Circuits (continued)

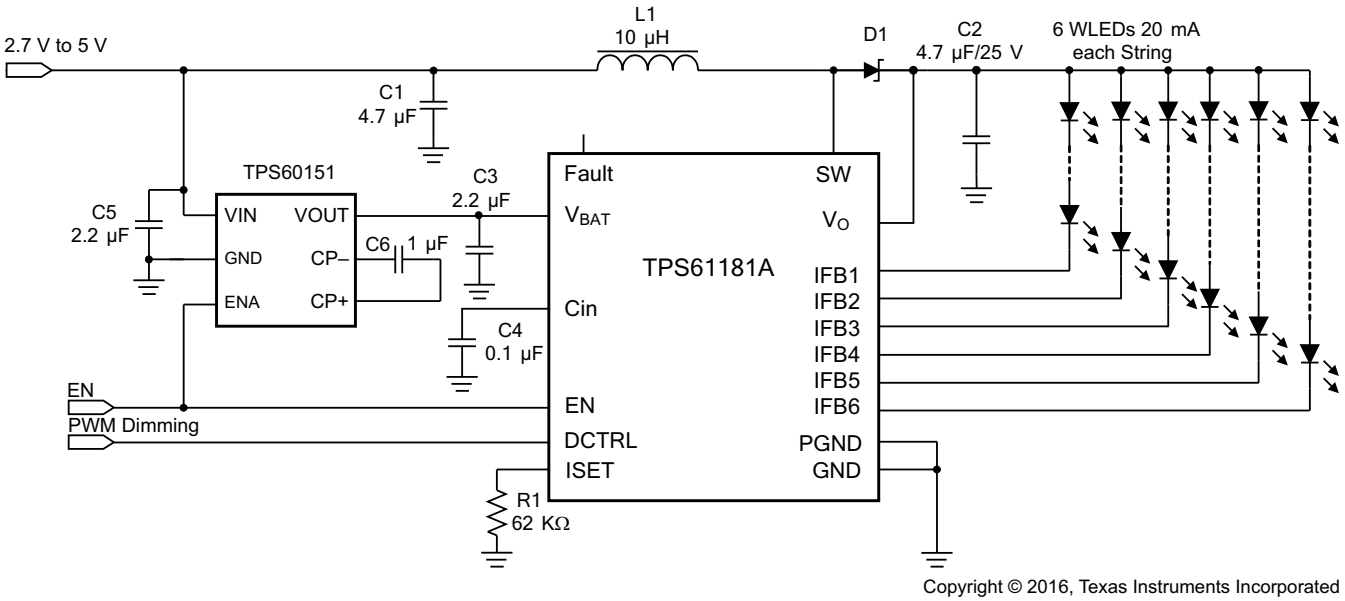


Figure 23. TPS61181A + TPS60151 for One Cell Li-Ion Battery Power Application

10 Power Supply Recommendations

The TPS61181A device requires a V_{BAT} pin supply from 4.5 V to 24 V.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor, C3 in the typical application circuit, needs not only to be close to the V_{BAT} pin, but also to the GND pin in order to reduce the input ripple detected by the device. The input capacitor, C1 in Figure 9 , must be placed close to the inductor. The SW pin carries high current with fast rising and falling edges. Therefore, keep the connection between the pin to the inductor and Schottky as short and wide as possible. It is also beneficial to have the ground of the output capacitor C2 close to the PGND pin because there is large ground return current flowing between them. When laying out signal ground, TI recommends using short traces separated from power ground traces, connecting these short traces together at a single point, for example on the thermal pad.

Thermal pad must be soldered on to the PCB and connected to the GND pin of the TPS61181A device. Additional thermal via can significantly improve power dissipation of the device.

11.2 Layout Example

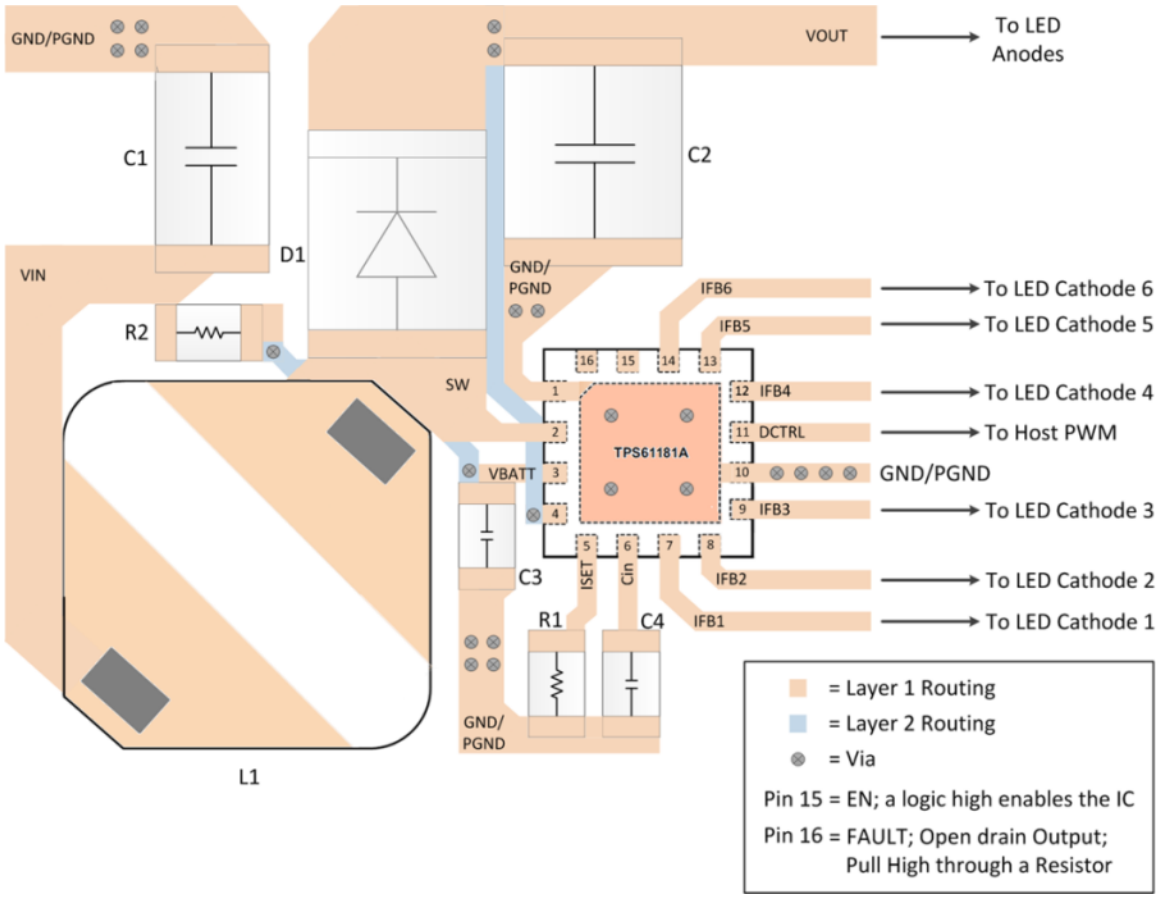


Figure 24. TPS61181A Layout

12 Device And Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61181ARTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QWF	Samples
TPS61181ARTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QWF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

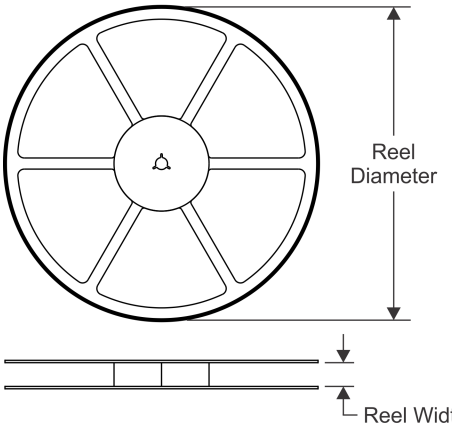
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

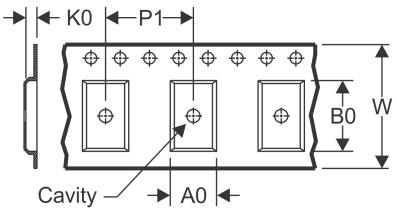
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

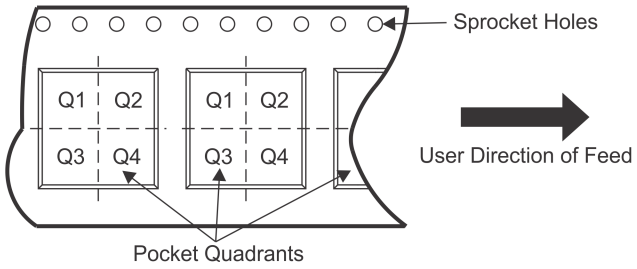


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

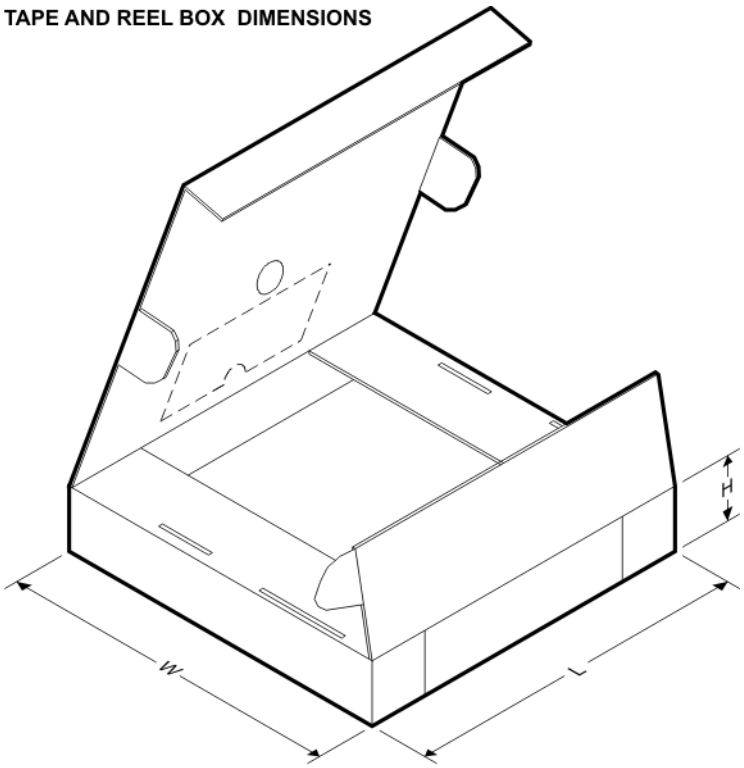
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61181ARTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61181ARTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

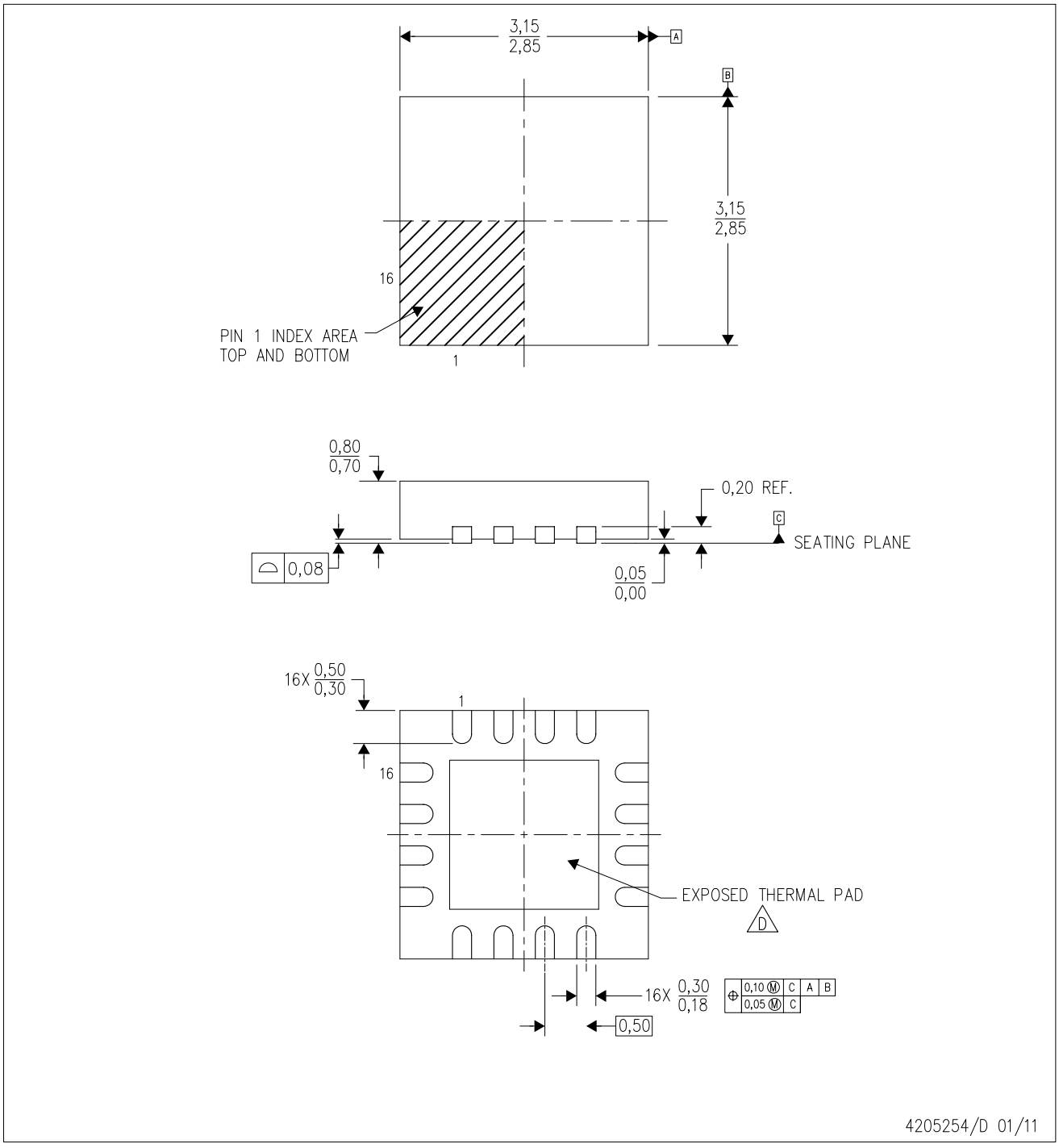
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61181ARTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS61181ARTET	WQFN	RTE	16	250	210.0	185.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

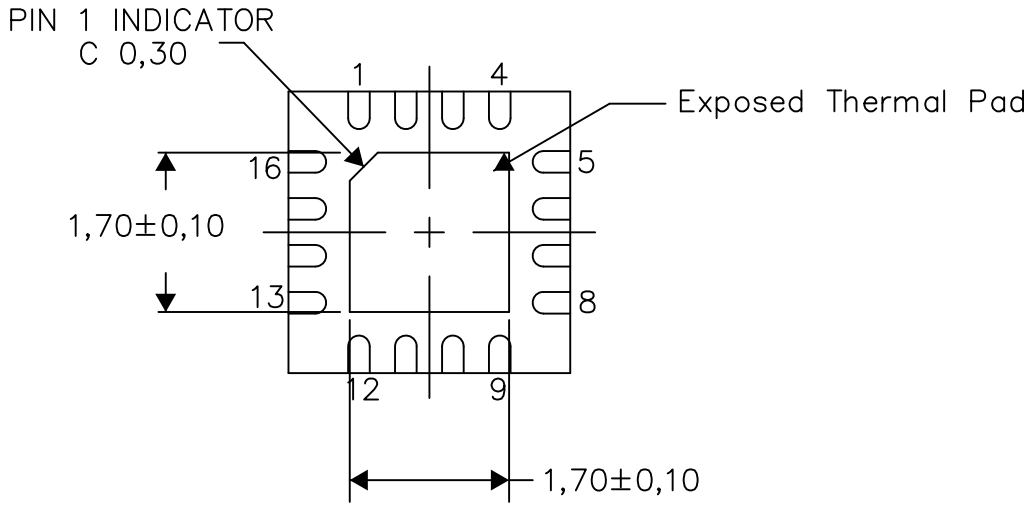
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



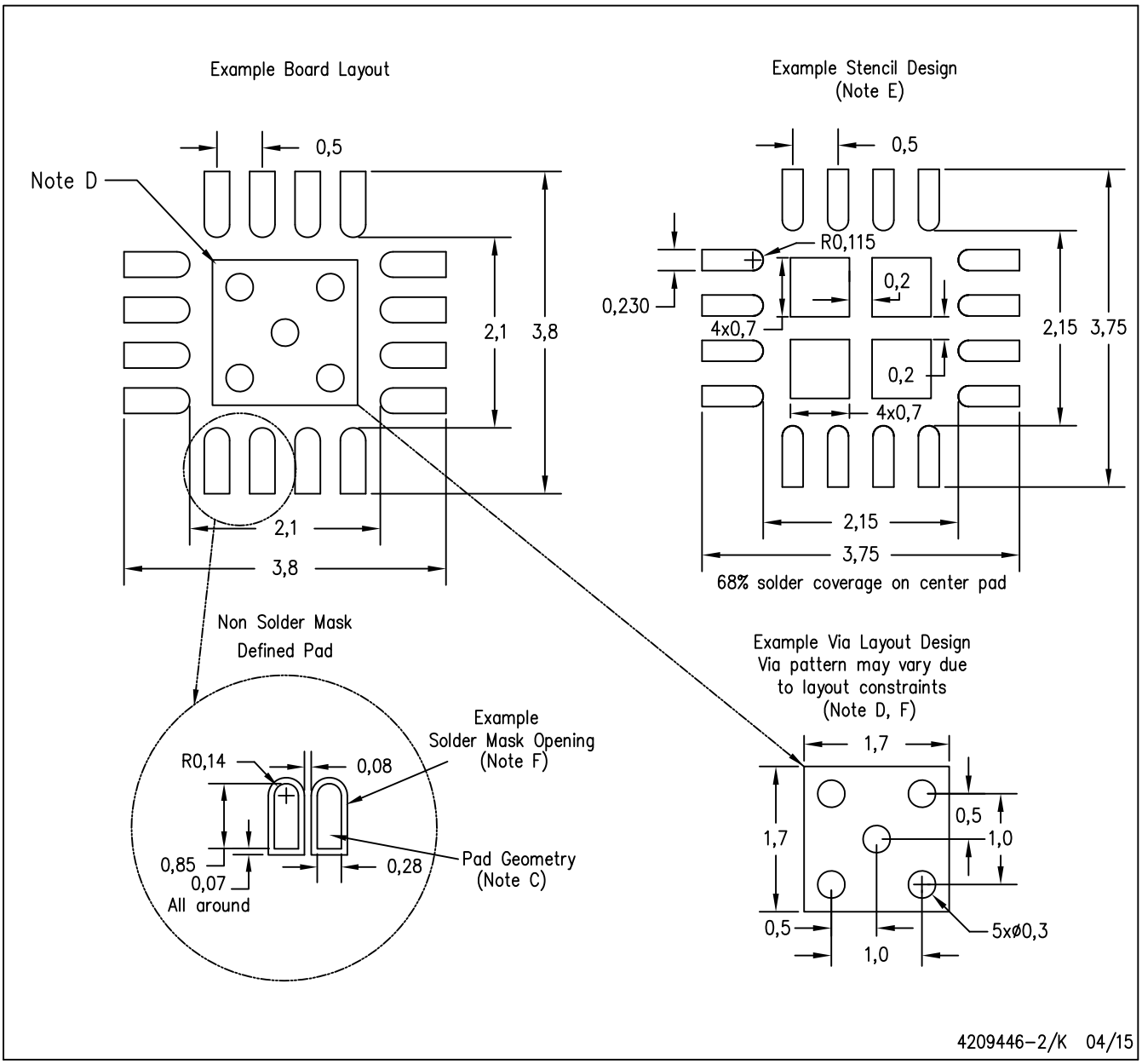
Bottom View

Exposed Thermal Pad Dimensions

4206446–3/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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