High Efficiency Step-Down Converter for USB Applications

Check for Samples :TPS62750, TPS62751

FEATURES

- Efficiency > 90% at Nominal Operating Conditions
- Programmable Average Input Current Limits for USB Applications
  - 50mA to 300mA for Low Current Limit Range
  - 300mA to 1.3A for High Current Limit Range
    - ±10% Current Accuracy
- Stable Output Voltage for Load Transients to Minimize Overshoot at Load Step Response
- Hot Plug and Reverse Current Protection
- Automatic PFM/PWM Mode transition (TPS62750)
- Forced PWM for Noise Sensitive Applications (TPS62751)
- V_{IN} Range From 2.9V to 6V
- Adjustable V_{OUT} From 0.8V to 0.85×VIN
- Softstart for Inrush Current Prevention
- 2.25 MHz Fixed Frequency Operation
- Short Cicruit and Thermal Shutdown Protection
- Available in a 2.5 × 2.5 10 pin SON Package

APPLICATIONS

- USB Wireless Modems
- Portable USB peripherals
- Handheld Computers

DESCRIPTION

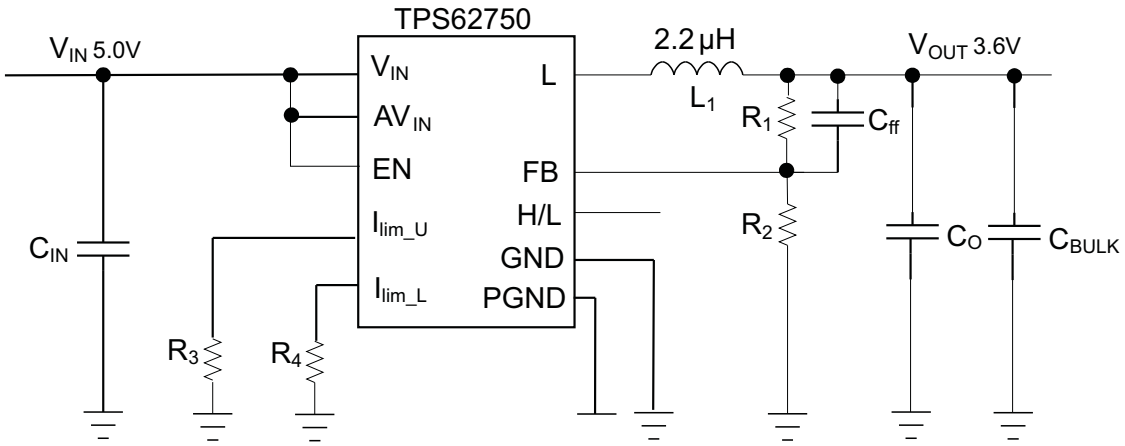
The TPS6275x device is a highly efficient synchronous step down dc-dc converter optimized for USB powered portable applications. It can provide up to 1300mA average input current and is ideal for applications connected to a USB host.

With an input voltage range of 2.9 V to 6.0V, the device supports batteries with extended voltage range and is ideal for powering USB applications where USB compliance is required.

The TPS62750 operates at 2.25-MHz fixed switching frequency and enters Power Save Mode operation at light load currents to maintain high efficiency over the entire load current range. The TPS62751 operates in Forced PWM mode allowing use in applications that are noise sensitive. An output discharge allows the load to discharge in shutdown.

The 10% accurate average input current limit can be programmed with an external resistor, allowing use in applications such as USB, where the current drawn from the bus must be limited to 500mA.

The TPS6275x allows the use of small inductors and capacitors to achieve a small solution size. The TPS6275x is available in a 2,5mm × 2,5mm 10-pin SON package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION(1)

T_A	PART NUMBER (2)	OUTPUT VOLTAGE (3)	PACKAGE	PACKAGE DESIGNATOR	ORDERING	PACKAGE MARKING
-40°C to 85°C	TPS62750	Adjustable	SON 2.5×2.5 -10	DSK	TPS62750DSK	NXJ
	TPS62751				TPS62751DSK	DAL

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com
(2) The DSK (SON-10) package is available in tape on reel. Add R suffix to order quantities of 3000 parts per reel.
(3) Contact TI for other fixed output voltage options

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Input voltage range V_{IN}, AV_{IN} (2)		–0.3 to 7.0	V
Voltage range at EN, H/L, FB		–0.3 to VIN +0.3, ≤7.0	V
Voltage on L, I_{Lim_U}, I_{Lim_L}		–0.3 to 7.0	V
Peak output current		Internally limited	A
ESD rating(3)	HBM Human body model	4	kV
	CDM Charge device model	1.5	
	Machine model	200	V
Maximum operating junction temperature, T_J		–40 to 125	°C
Storage temperature range, T_{stg}		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

DISSIPATION RATINGS(1) (2)

PACKAGE	THERMAL RESISTANCE $R_{\theta JA}$	THERMAL RESISTANCE $R_{\theta JP}$	THERMAL RESISTANCE $R_{\theta JC}$	POWER RATING FOR $T_A \le 25°C$	DERATING FACTOR ABOVE $T_A = 25°C$
DSK	60.6°C/W	6.3°C/W	40°C/W	1650mW	17mW/°C

(1) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = [T_{J(max)} - T_A]/\theta_{JA}$
(2) This thermal data is measured with a high-K board (4 layer board according to JESD51-7 JEDEC standard).

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{IN}	2.9		6	V
Output voltage range for adjustable voltage	0.8		0.85 × VIN	V
Operating ambient temperature, T_A	–40		85	°C
Operating virtual junction temperature, T_J	–40		125	°C

ELECTRICAL CHARACTERISTICS

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 5.0V. External components C_{IN} = 10µF 0603, C_O = 10µF 0603, C_{BULK} = 1.5mF, L = 2.2µH, refer to parameter measurement information.

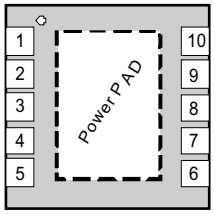
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input Voltage Range		2.9		6.0	V
I_Q	Operating Quiescent Current	I_{OUT} = 0 mA, device not switching (TPS62750) (1)		745	960	µA
		I_{OUT} = 0 mA, device not switching (TPS62751) (1)			30	mA
I_{SD}	Shutdown Current	EN = GND		0.2	3.0	µA
V_{UVLO}	Undervoltage Lockout Threshold	Falling	2.4			V
		Rising			2.9	V
ENABLE, H/L						
V_{IH}	High Level Input Voltage	2.9 V ≤ V_{IN} ≤ 6.0V	1.0			V
V_{IL}	Low Level Input Voltage	2.9 V ≤ V_{IN} ≤ 6.0 V			0.4	V
I_{IN}	Input bias Current	Pin tied to GND or VIN		0.01	1.0	µA
POWER SWITCH						
$R_{DS(ON)}$	High side MOSFET On-Resistance (H/L=HI)	V_{IN} = 5.0 V, V_{GS} = 6.5 V		130	290	mΩ
	High side MOSFET On-Resistance (H/L=LO)	V_{IN} = 5.0 V, V_{GS} = 6.5 V		282	550	mΩ
	Low Side MOSFET On-Resistance	V_{IN} = V_{GS} = 5.0 V		58	125	mΩ
I_{LIMF}	Forward Current Limit High-Side and Low side	V_{IN} = V_{GS} = 5.0 V	1200	1500	1800	mA
$I_{IN(MAX)}$	Programmable Input current Range	I_{LIM_U} selected, H/L = High	300		1300	mA
		I_{LIM_L} selected, H/L = Low	50		300	
		I_{LIM_U} selected, Current limit accuracy	–10		10	%
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shudown hysteresis	Decreasing junction temperature		20		°C
OSCILLATOR						
f_{SW}	Oscillator Frequency	2.9 V ≤ V_{IN} ≤ 6.0 V	2.0	2.25	2.5	MHz
OUTPUT						
V_{OUT}	Adjustable Output Voltage Range		0.8		0.85 × V_{IN}	V
V_{ref}	Reference Voltage			600		mV
$V_{FB(PWM)}$	Feedback Voltage	PWM operation, 2.9 V ≤ V_{IN} ≤ 6.0V (2)	–1.5%		1.5%	
$R_{(DIS\_CH)}$	Internal discharge resistor	Activated with EN = GND	85	235	300	Ω

(1) In PFM mode, the internal reference voltage is set to typ. 1.01 × V_{ref}. See the parameter measurement information.

DEVICE INFORMATION

PIN ASSIGNMENTS

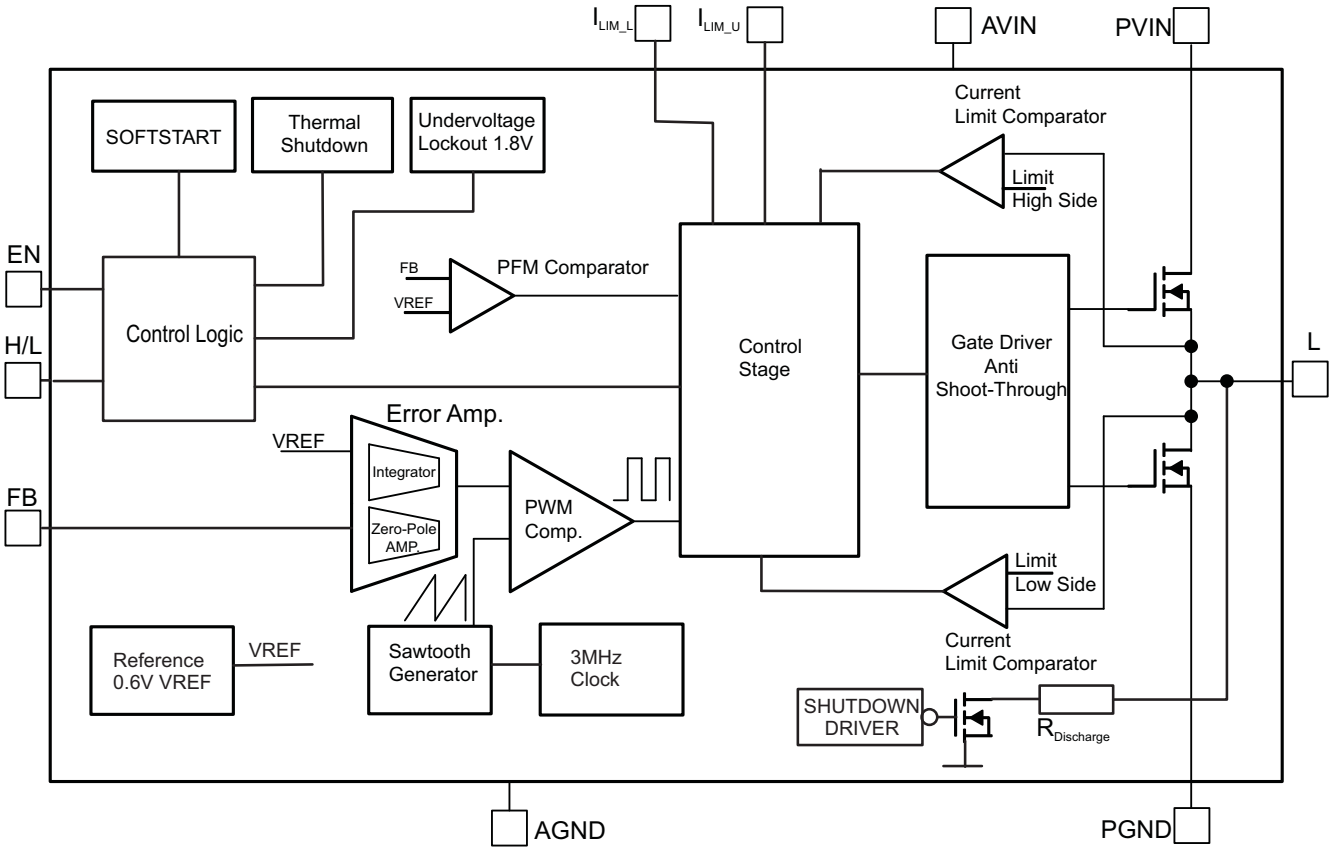
DSK PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
PGND	1		Power GND Pin for the N-MOSFET
L	2	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
H/L	3	IN	H/L pin = high enables the upper current limit threshold set by R_{SET_H}. H/L pin = low enables the lower current limit threshold set by R_{SET_L}. This pin must be terminated.
EN	4	IN	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
FB	5	IN	Feedback Pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output voltage option, connect this pin directly to the output capacitor
AGND	6		Analog GND Pin for the internal analog circuitry.
ISET_L	7	IN	Sets the lower average input current limit by external resistor.
ISET_U	8	IN	Sets the upper average input current limit by external resistor.
PVIN	9	IN	VIN power supply pin for the Output stage
AVIN	10	IN	VIN low noise analog supply for the internal analog circuitry. This pin must be connected to PVIN

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION

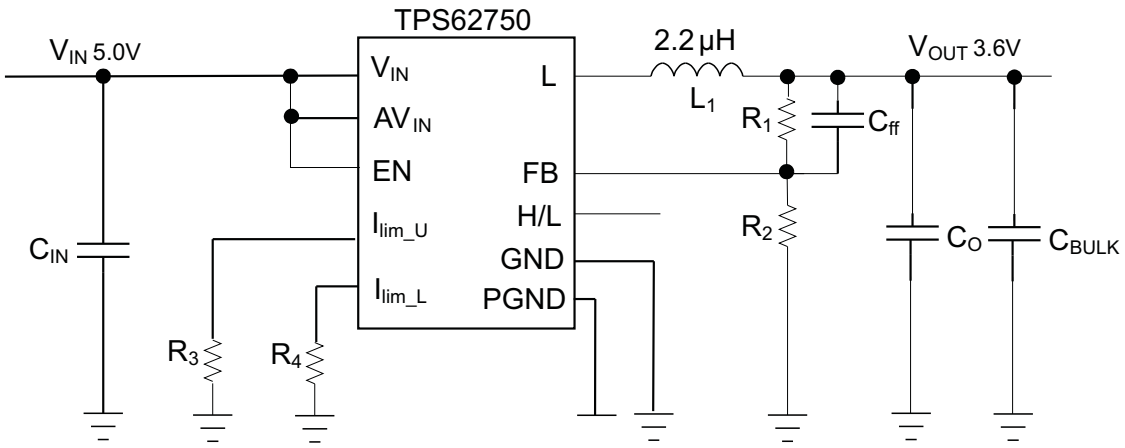


Table 2. List of Components

COMPONENT REFERENCE	PART NUMBER	MANUFACTURER	VALUE
CIN	GRM188R60J106M	Murata	10µF
COUT	GRM188R60J106M	Murata	10µF
C_{ff}	C1608C0G1H471J	TDK	470pF
C_{BULK}	6TPG150M	Sanyo POSCAP	10 × 150µF
	592D158X06R3X2T25H	Vishay	1.5mF
L1	LPS3015-222ML	Coilcraft	2.2µH
R1, R2	Depending on output voltage required. Equation 1 can be used to calculate the output voltage with different R1 and R2 values.		
R3, R4	Depending on the upper and lower current limits required. Equations 7 and 8 can be used for these calculations.		

TYPICAL CHARACTERISTICS

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Maximum Output Current	vs Input voltage	Figure 1
Efficiency	vs Output Current, Vin = [4.0V; 4.5V; 5.0V; 5.5V], Vout = 3.6V, H/L = High	Figure 2
	vs Output Current, Vin = [4.0V; 4.5V; 5.0V; 5.5V], Vout = 3.6V, H/L = Low	Figure 3
	vs Output Current, Vin = [4.0V; 4.5V; 5.0V; 5.5V], Vout = 2.5V, H/L = High	Figure 4
	vs Output Current, Vin = [4.0V; 4.5V; 5.0V; 5.5V], Vout = 2.5V, H/L = Low	Figure 5
	vs Input Voltage, Vout = 3.6V, Iout = [200mA, 400mA, 500mA, 700mA, 1000mA]	Figure 6
Input Current	vs Output Current, Vout =3.6V, Vin = [4.0V; 4.5V; 5.0V; 5.5V]	Figure 7
Output Voltage	vs Output Current, Vout = 3.6V, Vin = [4.5V; 5.0V; 5.5V], H/L = High	Figure 8
	vs Output Current, Vout = 3.6V, Vin = [4.5V; 5.0V; 5.5V], H/L = Low	Figure 9
	vs Input Voltage, Iload = 300mA, Vout = 3.6V H/L=high	Figure 10
	vs Input Voltage, Iload = 500mA, Vout = 3.6V H/L=high	Figure 11
	vs Input Voltage, Iload = 100µA, Vout = 3.6V H/L=low	Figure 12
	vs Input Voltage, Iload = 80mA, Vout = 3.6V H/L=low	Figure 13
Waveforms	Output Voltage Ripple, PFM Mode Iout = 50mA	Figure 14
	Output Voltage Ripple, PWM Mode Iout = 500mA	Figure 15
	Load Transient Vin = 5.0V, Vout = 3.6V, H/L = High, 50mA - 2A & 2A - 50mA, Pulse Load period = 4.6ms, duty cycle 12.5%	Figure 16
	Load Transient Vin = 5.0V, Vout = 3.6V, H/L = High, 50mA - 2A & 2A - 50mA, Pulse Load period = 4.6ms, duty cycle 25%	Figure 17
	Line Transient, Vin = 4.5V - 5.0V, Iout = 80mA, H/L = Low	Figure 18
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	Average Input current Limit vs R_{LIM_L}	Figure 21
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	Startup after Enable, Vin = 5.0V, Vout = 3.6V, Load = 80mA, H/L=Low	Figure 23
	Startup after Enable, Vin = 5.0V, Vout = 3.6V, Load = 500mA, H/L=High	Figure 24
	Output Discharge, Vin = 5.0V, Vout = 3.6V, No Load	Figure 25

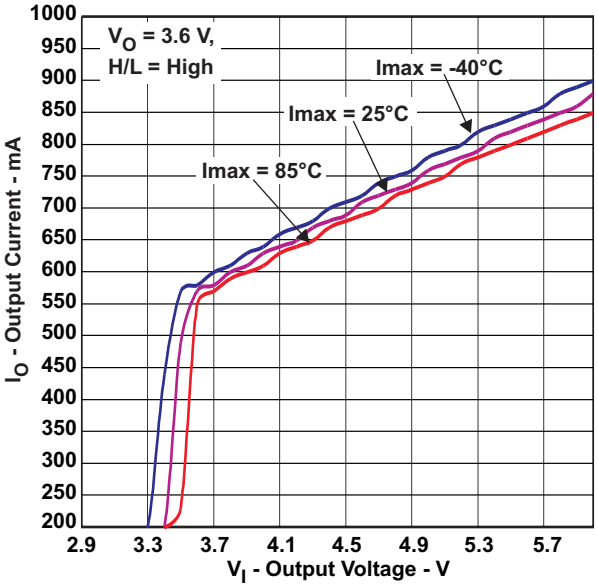


Figure 1. Maximum Output Current

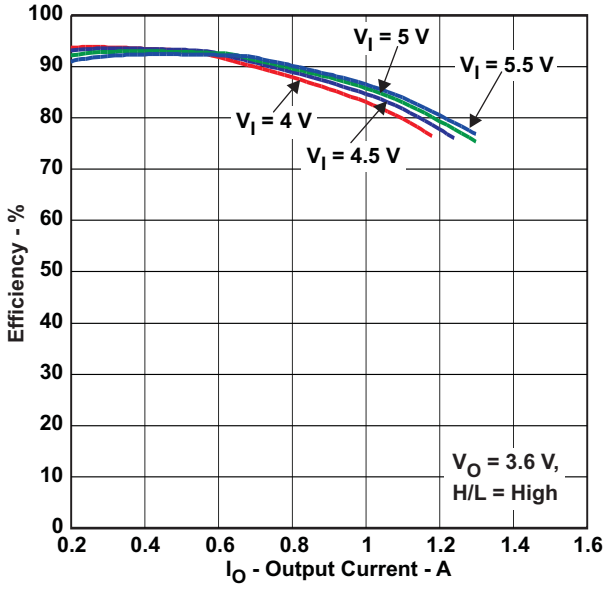


Figure 2. Efficiency vs Output Current

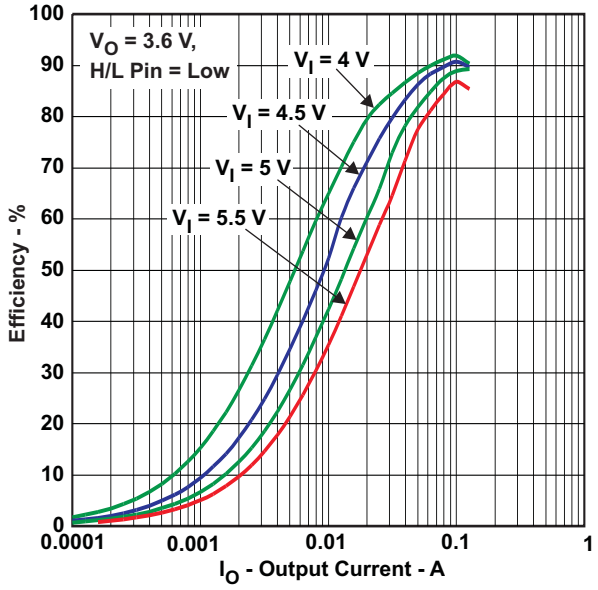


Figure 3. Efficiency vs Output Current

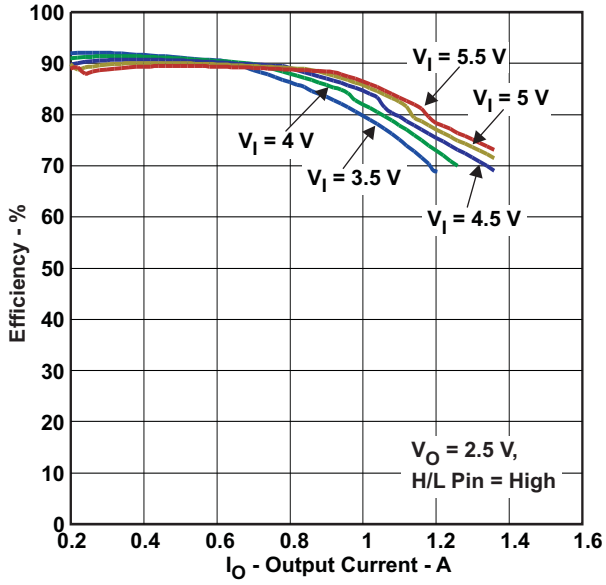


Figure 4. Efficiency vs Output Current

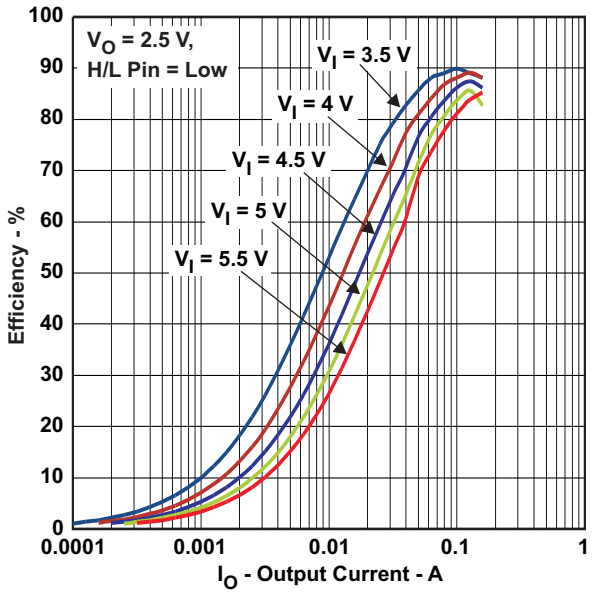


Figure 5. Efficiency vs Output Current

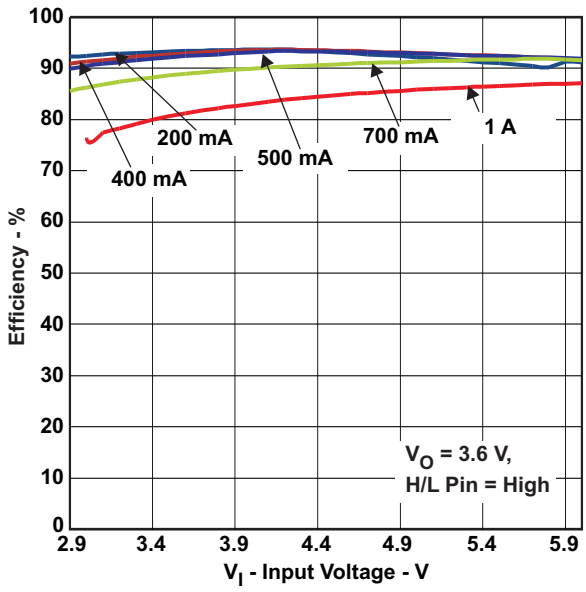


Figure 6. Efficiency vs Input Voltage

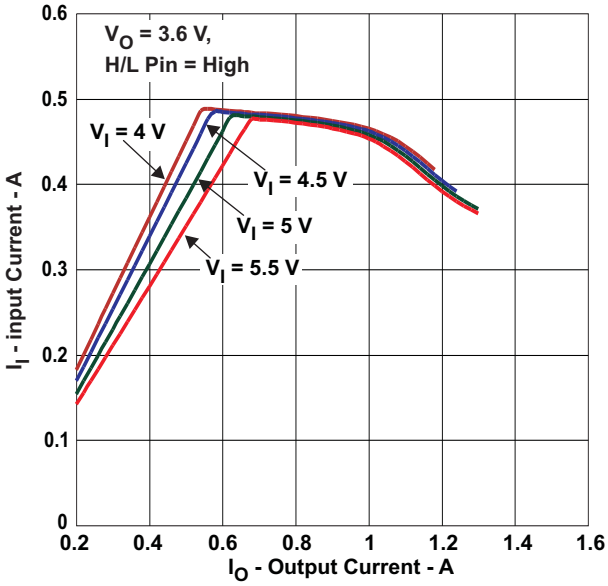


Figure 7. Input Current vs Output Current

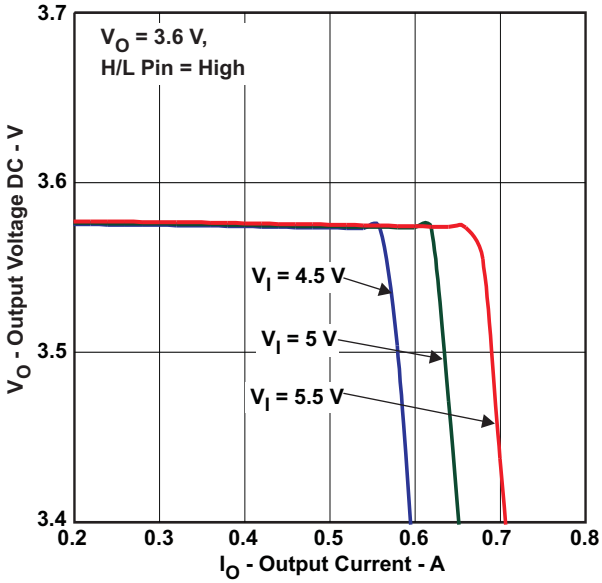


Figure 8. Output Voltage vs Output Current

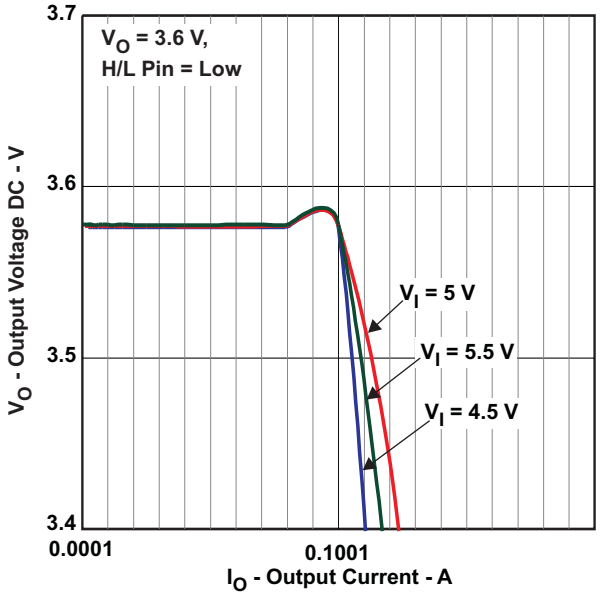


Figure 9. Output Voltage vs Output Current

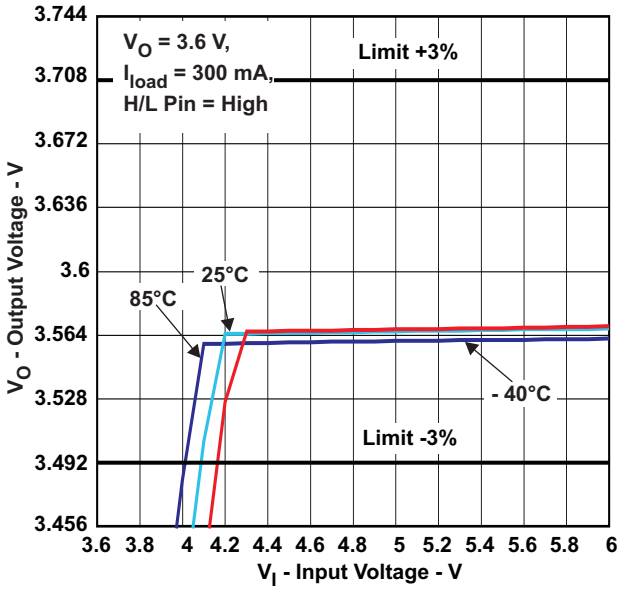


Figure 10. Output Voltage vs Input Voltage

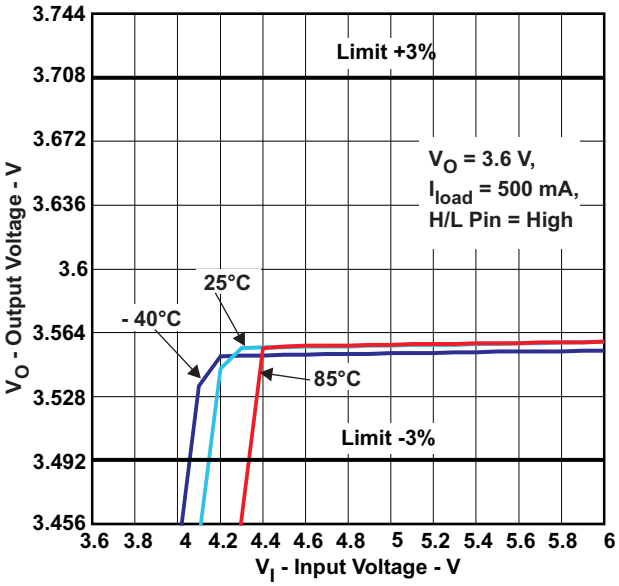


Figure 11. Output Voltage vs Input Voltage

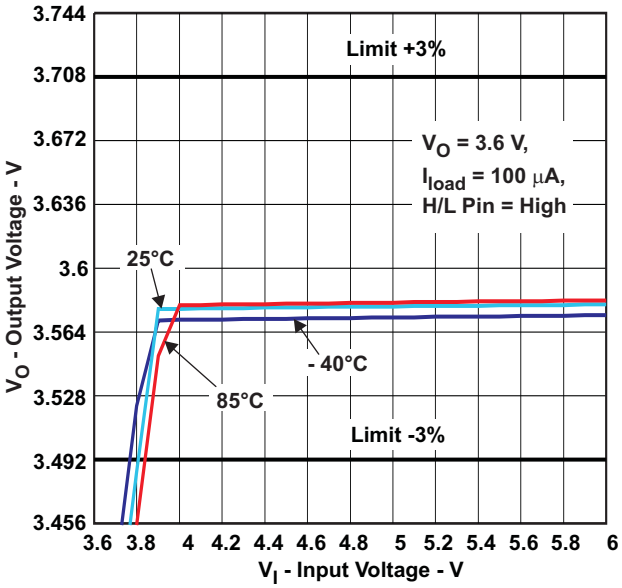


Figure 12. Output Voltage vs Input Voltage

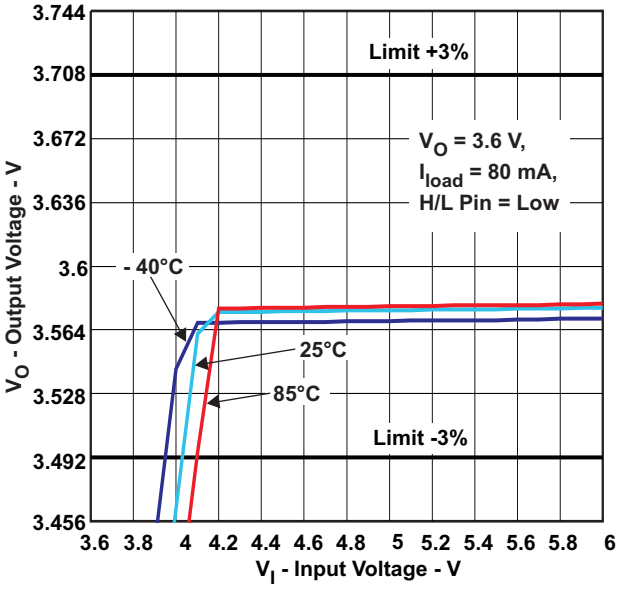


Figure 13. Output Voltage vs Input Voltage

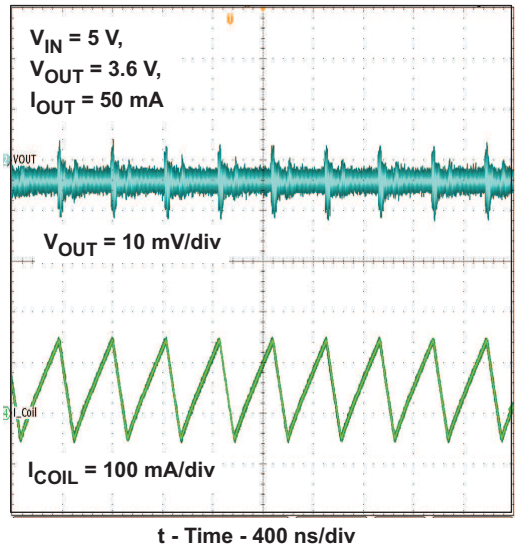


Figure 14. Output Voltage Ripple – PFM Mode

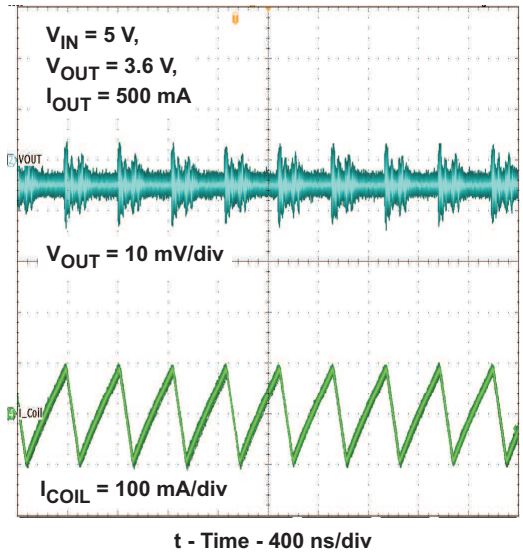


Figure 15. Output Voltage Ripple – PWM Mode

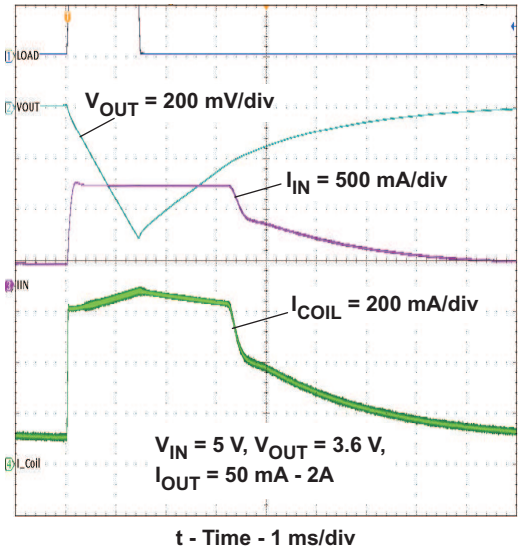


Figure 16. Load Transient

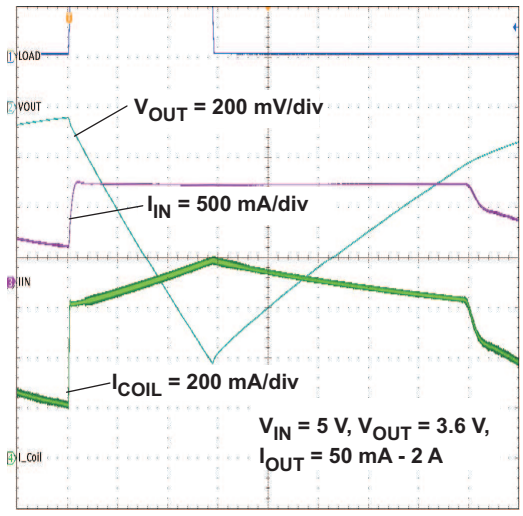


Figure 17. Load Transient

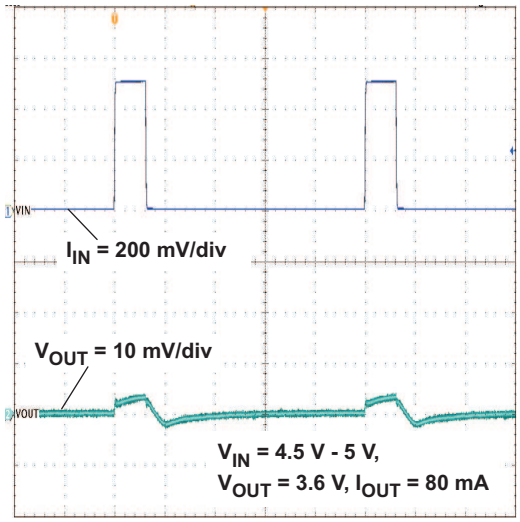


Figure 18. Line Transient

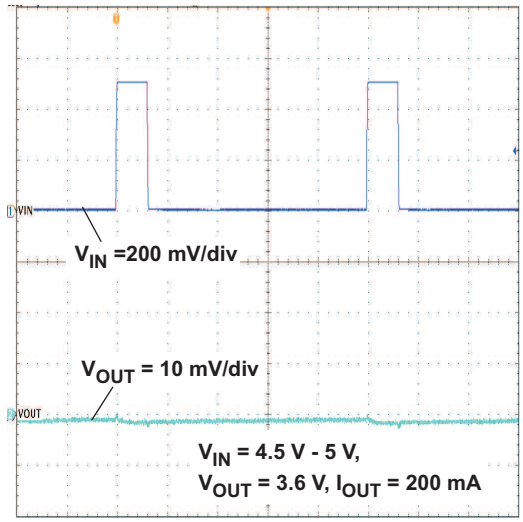


Figure 19. Line Transient

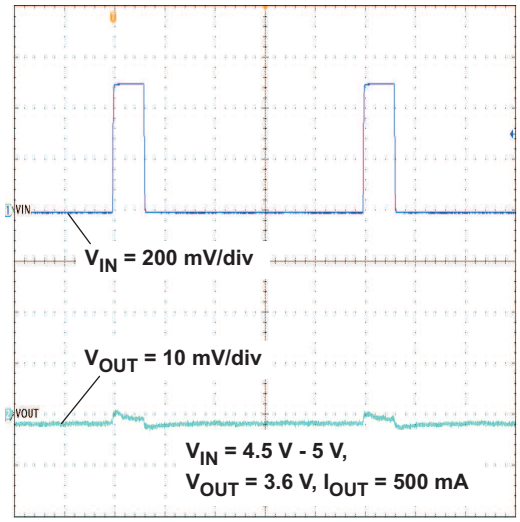


Figure 20. Line Transient

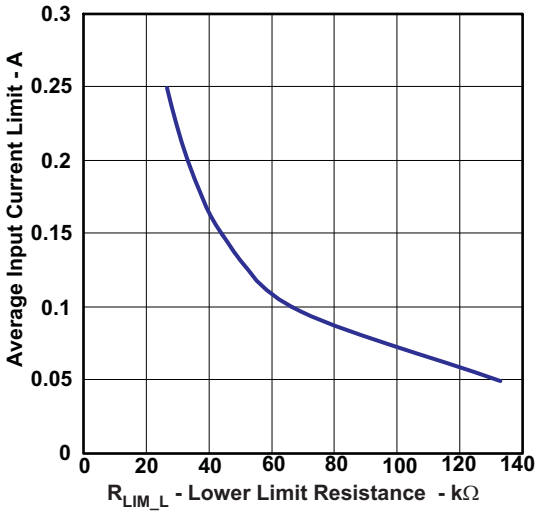


Figure 21. Average Input Current Limit

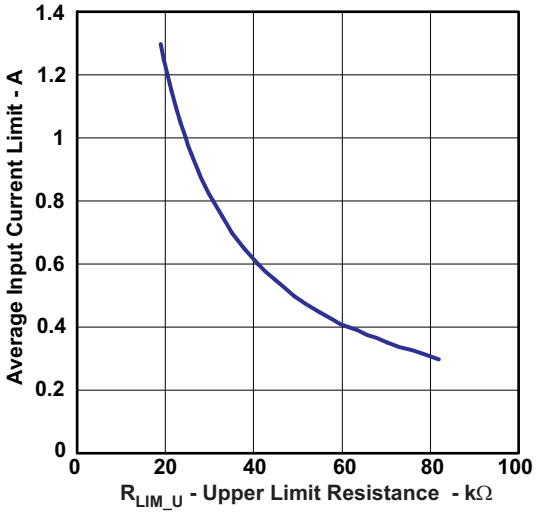


Figure 22. Average Input Current Limit

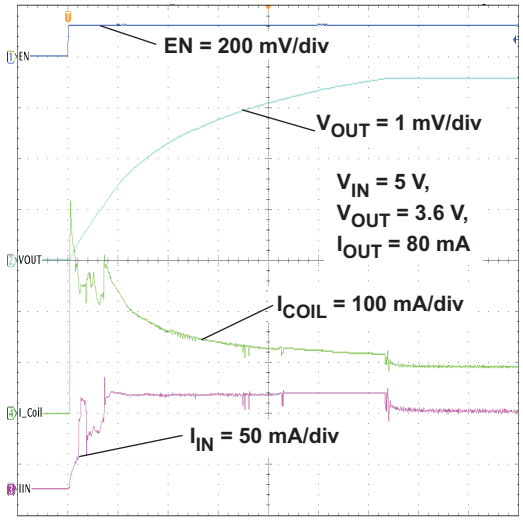


Figure 23. Startup After Enable

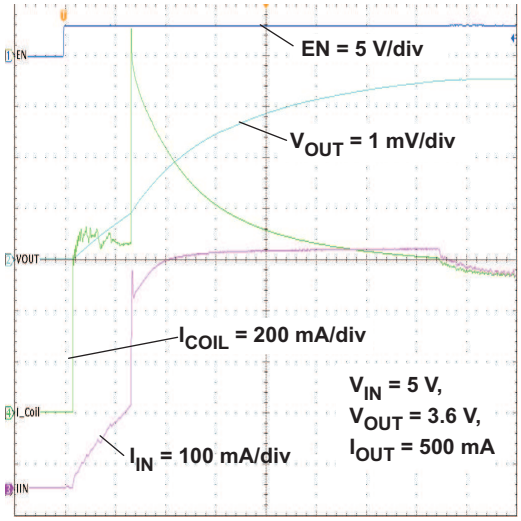
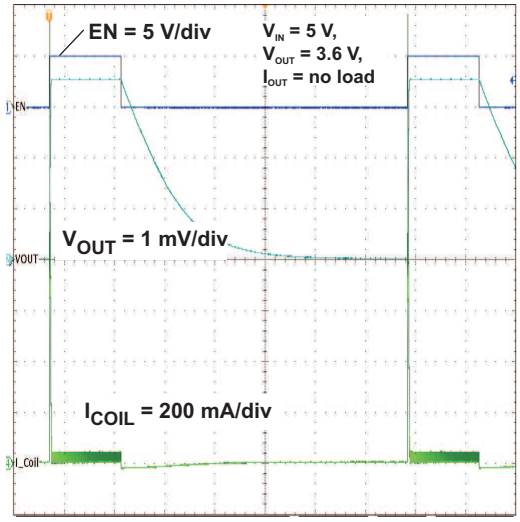


Figure 24. Startup After Enable



t - Time - 200 ms/div

Figure 25. Output Discharge

DETAILED DESCRIPTION

OPERATION

The TPS6275x step down converter operates with typically 2.25MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents the converter can automatically enter Power Save Mode and operates then in PFM (Pulse Frequency Mode) mode.

During PWM operation, the converter uses a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the High Side MOSFET switch is turned on. The current flows from the input capacitor via the High Side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic will turn off the switch.

The current limit comparator will also turn off the switch in case the current limit of the High Side MOSFET switch is exceeded. After a dead time preventing shoot through current, the Low Side MOSFET rectifier is turned on and the inductor current will ramp down. The current flows now from the inductor to the output capacitor and to the load. It returns back to the inductor through the Low Side MOSFET rectifier.

The next cycle will be initiated by the clock signal again turning off the Low Side MOSFET rectifier and turning on the on the High Side MOSFET switch.

POWER SAVE MODE

If the load current decreases, the converter will enter Power Save Mode operation automatically. During Power Save Mode the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency.

The transition from PWM mode to PFM mode occurs once the inductor current in the Low Side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During the Power Save Mode the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of V_{OUT} nominal +1%, the device starts a PFM current pulse. For this the High Side MOSFET switch will turn on and the inductor current ramps up. After the On-time expires the switch will be turned off and the Low Side MOSFET switch will be turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current the output voltage will rise. If the output voltage is equal or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode.

In case the output voltage is still below the PFM comparator threshold, further PFM current pulses will be generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold.

With a fast single threshold comparator, the output voltage ripple during PFM mode operation can be kept very small. The PFM Pulse is timing controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple depends in first order on the size of the output capacitor and the inductor value. Increasing output capacitor values and/or inductor values will minimize the output ripple.

The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode.

ENABLE

The device is enabled setting EN pin to high. During the start up time $t_{start-up}$ the internal circuits are settled. Afterwards the device activates the soft start circuit. The EN input can be used to control power sequencing in a system with various DC/DC converters.

The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN = GND, the device enters shutdown mode. In this mode, all circuits are disabled. In fixed output voltage versions, the internal resistor divider network is disconnected from FB pin.

OUTPUT CAPACITOR DISCHARGE

With EN = GND, the device enters shutdown mode and all internal circuits are disabled. The SW pin is connected to PGND via an internal resistor (typically 235Ω) to discharge the output capacitor.

SOFT START

The TPS62750 has an internal soft start circuit that controls the ramp up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value in a controlled manner. This limits the inrush of current in the converter during start-up and prevents possible voltage drops when a battery or high impedance power source is used.

During soft start, the target average input current limit is reduced to 1/3 of its nominal value (I_{LIM_L} or I_{LIM_U}) until the output voltage reaches 1/3 of its nominal value. Once the output voltage trips this threshold, the device operates with its set target average input current limit.

The Soft-Start circuit is enabled after the start-up time $t_{start-up}$ has expired.

HOT-PLUG PROTECTION

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on.

Due to the controlled rise times and fall times and input over-voltage clamping of the TPS62750, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS62750 also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.

REVERSE CURRENT PROTECTION

The USB specification does not allow an output device to source current back into the USB port. However, the TPS62750 is designed to safely power non-compliant devices. When disabled, each output is switched to a high-impedance state, blocking reverse current flow from the output back to the input.

SHORT-CIRCUIT PROTECTION

During normal operation the High Side and Low Side MOSFET switches are protected by its current limits I_{LIMF}. Once the High Side MOSFET switch reaches its current limit, it is turned off and the Low Side MOSFET switch is turned on. The High Side MOSFET switch can only turn on again, once the current in the Low Side MOSFET switch decreases below its current limit. The device is capable to provide peak inductor currents up to its internal current limit I_{LIMF}.

As soon as the output voltage falls below 1/3 of the nominal output voltage due to overload or short circuit condition, the converter current limit is reduced to 1/3 of the nominal value ILIMF. Due to the short-circuit protection is enabled during start-up, the device does not deliver more than 1/3 of its nominal current limit I_{LIMF} until the output voltage exceeds 1/3 of the nominal output voltage. This needs to be considered when a load is connected to the output of the converter, which acts as a current sink.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the High Side and Low Side MOSFETs are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

APPLICATION INFORMATION

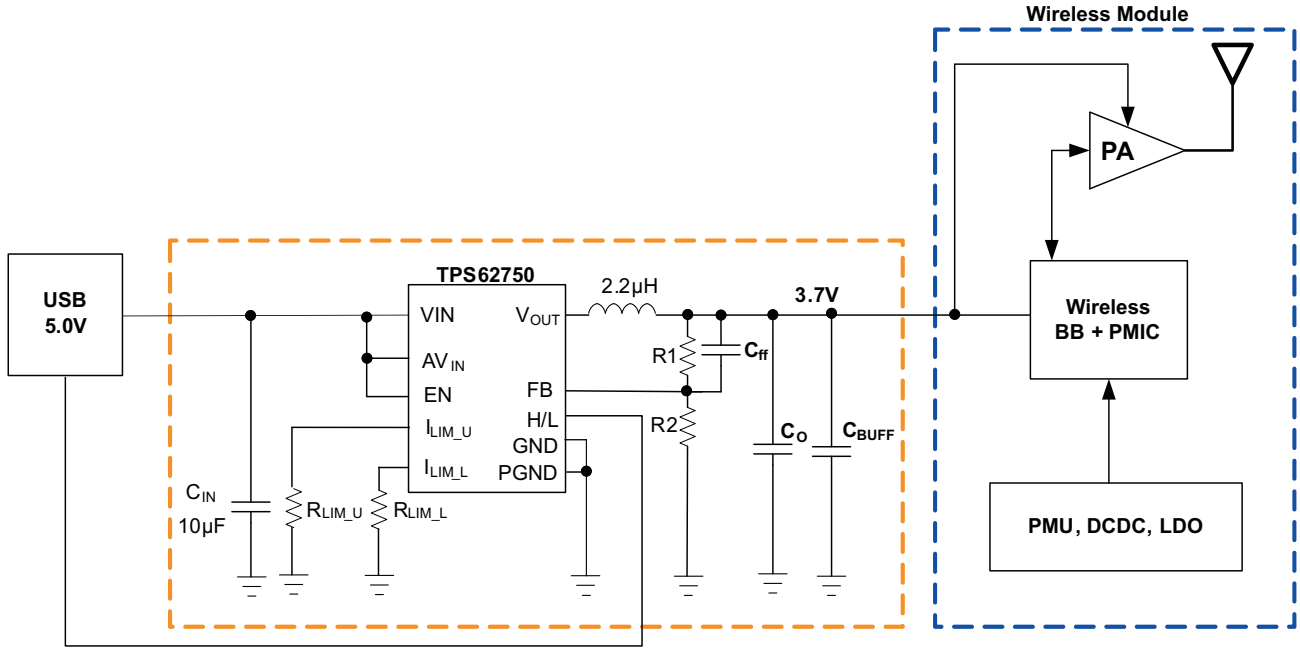


Figure 26. TPS62750DSK in a typical USB Datacard application

A growing variety of applications in notebooks, PCs and other mobile systems, TDMA data communication techniques, which require peak current (typically 2A) during the transmission of signals that can exceed the maximum current specified by the USB standard. Therefore, the application must be designed to limit the input power and draw on card-based storage for most of the energy requirement during a typical transmission cycle.

A typical GSM signal is transmitted over the carrier at a rate of 216 Hz (4.616ms pulse repetition interval). The transmission period is divided into eight time slots and depending on the power class being used, the duty cycle of this high current pulse can range anywhere between one-eighth of the cycle (577us) up to half of the transmission cycle (2.308ms).

The TPS62750 external current limit programming resistors can be easily used to adjust the required input current limit, thereby allowing the user to stay well within the specification requirement stipulated by USB. The TPS62750 is a high efficiency buck converter with programmable input average current limit that provides the needed flexibility when designing a GSM/GPRS power supply solution. The high efficiency of the converter maximizes the average output power without overloading the bus. A bulk output capacitor is used to supply the energy and maintain the output voltage during the high current pulses

OUTPUT VOLTAGE SETTING

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \text{ with an internal reference voltage VREF typical 0.6V} \quad (1)$$

To minimize the current through the feedback divider network, we recommend that the R2 resistor value be 180k. The sum of R1 and R2 should not exceed ~1.5MΩ, to keep the network robust against noise.

An external feed forward capacitor C_{ff} is required for optimum load transient response. The value of C_{ff} should be a minimum of 470pF (see table below). Route the FB line away from noise sources, such as the inductor or the SW line.

OUTPUT CAPACITOR	FEEDFORWARD CAPACITOR
1 mF – 2.5 mF	470 pF
> 2.5 mF	1 nF

INDUCTOR SELECTION

The inductor value has a direct effect on the ripple current. The selected inductor has to be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

The inductor selection has also impact on the output voltage ripple in PFM mode. Higher inductor values will lead to lower output voltage ripple and higher PFM frequency, lower inductor values will lead to a higher output voltage ripple but lower PFM frequency.

Equation 2 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 3. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (2)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (3)$$

With:

f = Switching Frequency (2.25MHz typical)
L = Inductor Value
ΔI_L= Peak to Peak inductor ripple current
I_{Lmax} = Maximum Inductor current

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. Accepting larger values of ripple current allows the use of low inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability. The device has been optimized to operate with inductance values between 1.0µH and 4.7µH. It is recommended that inductance values of at least 1.0µH is used, even if Equations 2 and 3 yield something lower.

The total losses of the coil have a strong impact on the efficiency of the DC/DC conversion and consist of both the losses in the dc resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Table 3. List of Inductors

MANUFACTURER	INDUCTOR TYPE	DIMENSIONS [mm]
Coilcraft	LPS3015-222ML	3.0 x 3.0 x 1.5
TOKO	1127AS-2R2M	3.5 x 3.7 x 1.8
Murata	LQH32PN1R0N0	3.2 x 2.5 x 1.7
TOKO	DB3015 Series	3.2 x 3.2 x 1.5

INPUT CAPACITOR SELECTION

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications a 4.7µF to 10µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or VIN step on the input can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

OUTPUT CAPACITOR SELECTION

The TPS62750 has been specifically internally compensated to operate with large capacitance values. But to maintain loop stability of the device, it is recommended to use a small ceramic capacitor placed as close as possible to the V_{OUT} and GND pins of the IC in parallel with the large holdup capacitor. To get an estimate of the small ceramic recommended minimum output capacitance, Equation 4 can be used.

$$C_{min} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f \times \Delta V \times V_{OUT}} \quad (4)$$

Parameter f is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 10 mV, a minimum effective capacitance of 2.7 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using $\Delta V_{ESR} = I_{OUT} \times R_{ESR}$.

A capacitor with a value in the range of the calculated minimum should be used. This is required to maintain control loop stability. There are no additional requirements regarding minimum ESR. There is no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

Note that ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance needed. Therefore the right capacitor value has to be chosen very carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and the effective capacitance.

To calculate the value of the effective capacitance required to buffer a GSM transmission pulse, the following equations can be used:

$$\text{Capacitance} = \frac{I \times \Delta t}{\Delta V} \quad (5)$$

Assuming the DCDC supplies ~700mA, the rest of the energy to supply the GSM transmission pulse must come from the capacitor.

$I_{CAP} = I_{GSM} - I_{DCDC}$

$I_{CAP} = 2A - 700mA = 1.3A$

Assuming a GSM transmission pulse width of 1.154ms and allowing a maximum voltage drop on the output of 350mV, the effective capacitance required is:

$$\text{Capacitance} = \frac{1.3A \times 1.154ms}{350mV} = 4.2mF \quad (6)$$

Table 4. List of Capacitors

COMPONENT REFERENCE	PART NUMBER	MANUFACTURER	VALUE
C_O	GRM188R60J106M69D	Murata	10µF
C_{BULK}	6TPG150M	Sanyo POSCAP	150µF
	592D158X06R3X2T25H	Vishay	1.5mF
	592D228X06R3X2T22H	Vishay	2.2mF

AVERAGE INPUT CURRENT LIMIT

The average input current is set by selecting the correct external resistor value correlating to the required current limit. The current limit can be selected between a high current limit (I_{LIM_U}) and a lower limit (I_{LIM_L}) by toggling the H/L pin high or low. This has the added benefit that of allowing a device first plugged into the USB port to enumerate at 100mA before switching over to the high power mode (500mA). The equations below are a guideline for selecting the correct resistor value:

$$\text{Upper range: } R_{LIM\_U} = \left(\frac{1.23}{I_{LIM\_U}}\right) \times 20000 \tag{7}$$

$$\text{Lower range: } R_{LIM\_L} = \left(\frac{1.23}{I_{LIM\_L}}\right) \times 5400 \tag{8}$$

Examples of different input current limit values selectable are given in the table below:

AVERAGE INPUT CURRENT REQUIRED	RESISTOR VALUE
50 mA	132.8 K
100 mA	66.5 K
400 mA	61.5 K
500 mA	49.2 K
600 mA	41 K
700 mA	35.1 K

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{O(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_O immediately shifts by an amount equal to $\Delta I_{(LOAD)} \times ESR$, where ESR is the effective series resistance of C_O. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_O to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_O can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET R_{DSon}) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

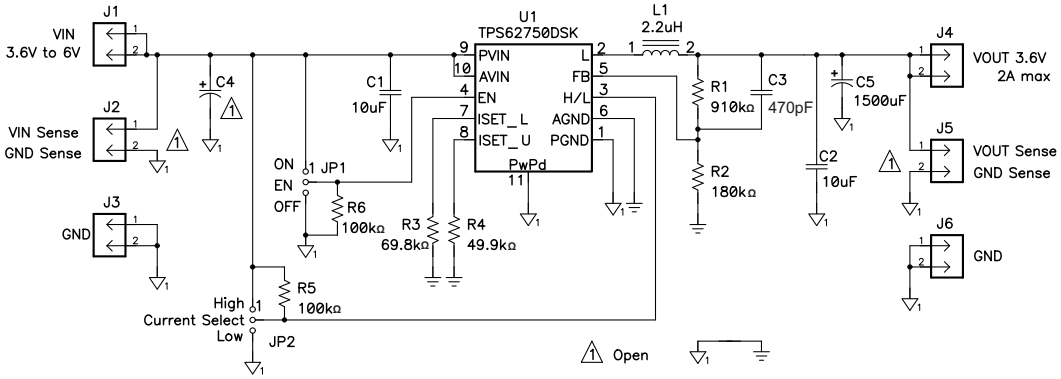


Figure 27. Checking Loop Stability

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Connect the GND Pin of the device to the Power Pad of the PCB and use this Pad as a star point. Use a common Power GND node and a different node for the Signal GND to minimize the effects of ground noise. Connect these ground nodes together to the Power Pad (star point) underneath the IC. Keep the common path to the GND PIN, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The FB line should be connected right to the output capacitor and routed away from noisy components and traces (e.g., SW line).

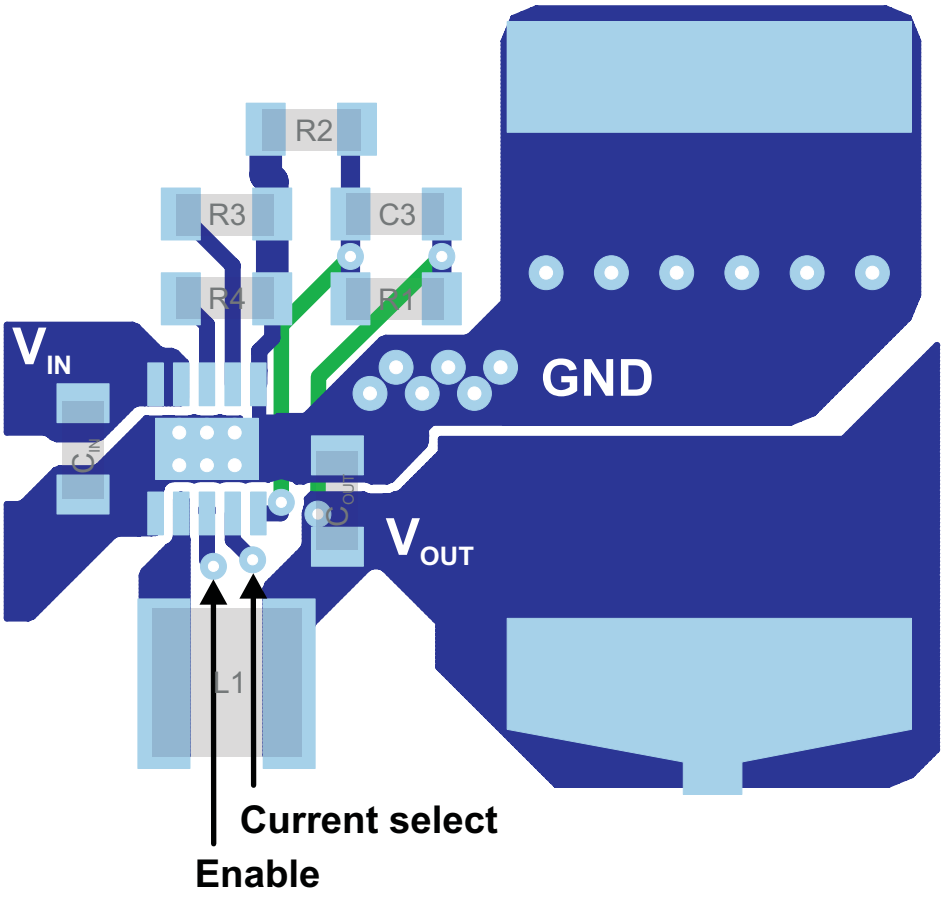


Figure 28. Suggested Layout

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component. Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow into the system

For more details on how to use the thermal parameters in the dissipation ratings table please check the Thermal Characteristics Application Note (SZZA017) and the IC Package Thermal Metrics Application Note (SPRA953).

Changes from Original (July 2009) to Revision A **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS62750DSKR	ACTIVE	SON	DSK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NXJ	Samples
TPS62750DSKT	ACTIVE	SON	DSK	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NXJ	Samples
TPS62751DSKR	ACTIVE	SON	DSK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DAL	Samples
TPS62751DSKT	ACTIVE	SON	DSK	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DAL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

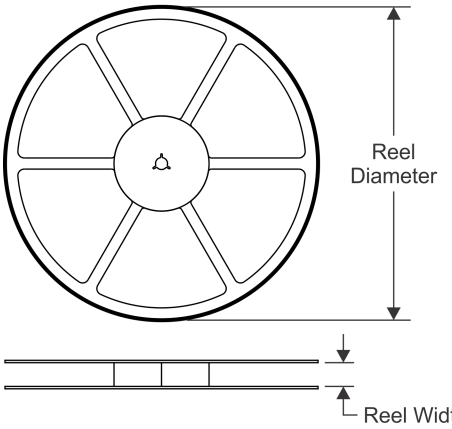
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

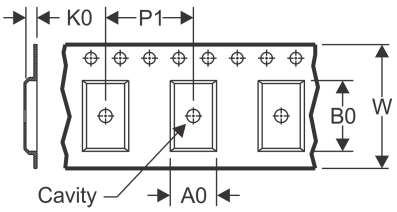
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

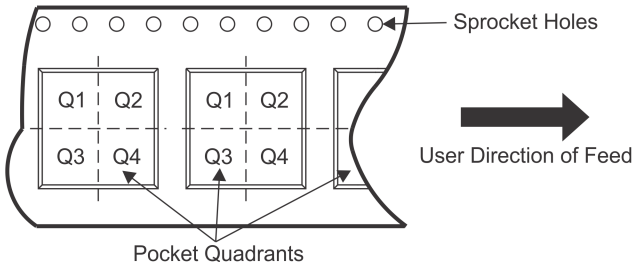


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

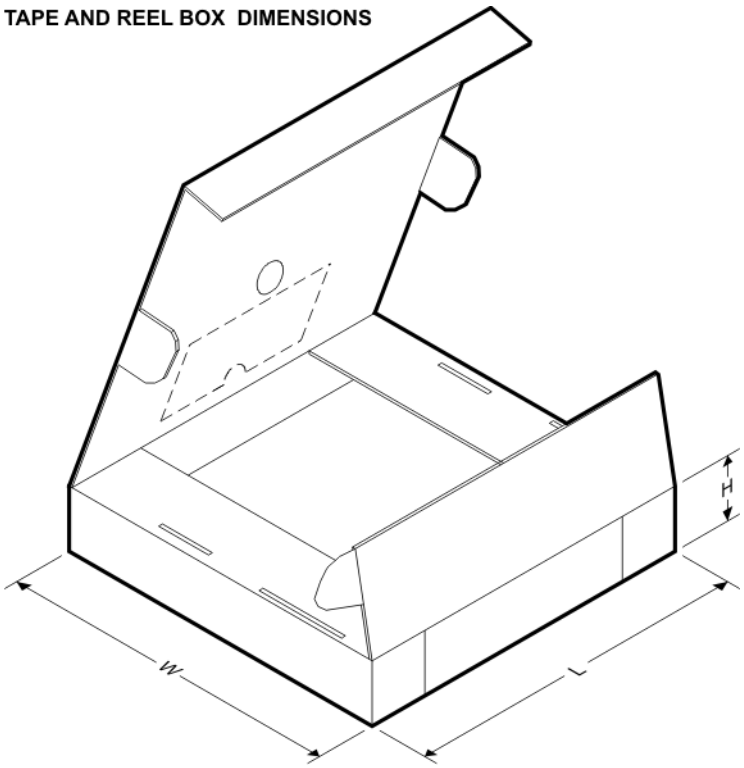
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62750DSKR	SON	DSK	10	3000	179.0	8.4	2.73	2.73	0.8	4.0	8.0	Q2
TPS62750DSKT	SON	DSK	10	250	179.0	8.4	2.73	2.73	0.8	4.0	8.0	Q2
TPS62751DSKR	SON	DSK	10	3000	179.0	8.4	2.73	2.73	0.8	4.0	8.0	Q2
TPS62751DSKT	SON	DSK	10	250	179.0	8.4	2.73	2.73	0.8	4.0	8.0	Q2

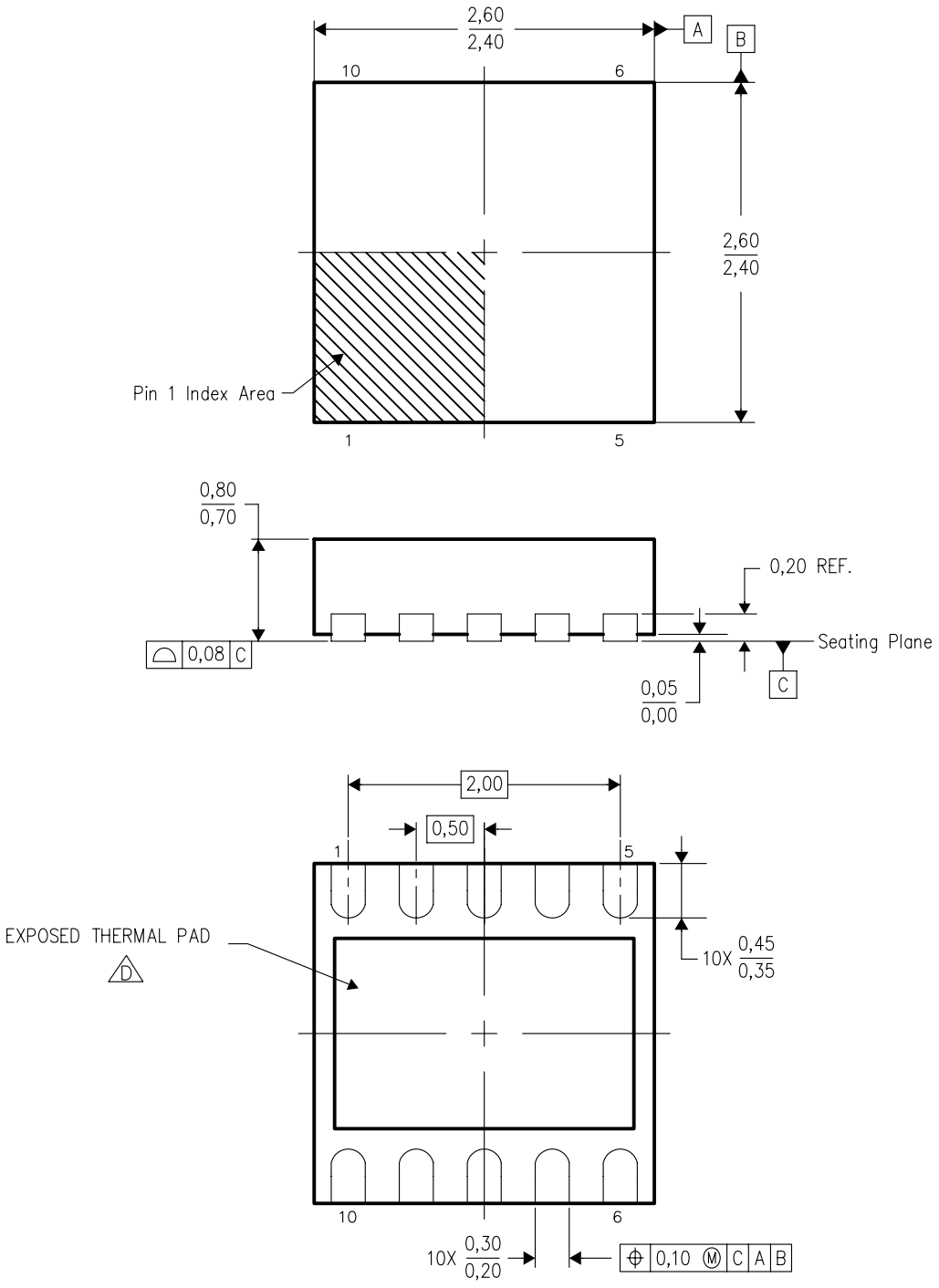
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62750DSKR	SON	DSK	10	3000	203.0	203.0	35.0
TPS62750DSKT	SON	DSK	10	250	203.0	203.0	35.0
TPS62751DSKR	SON	DSK	10	3000	203.0	203.0	35.0
TPS62751DSKT	SON	DSK	10	250	203.0	203.0	35.0

DSK (S–PDSO–N10) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

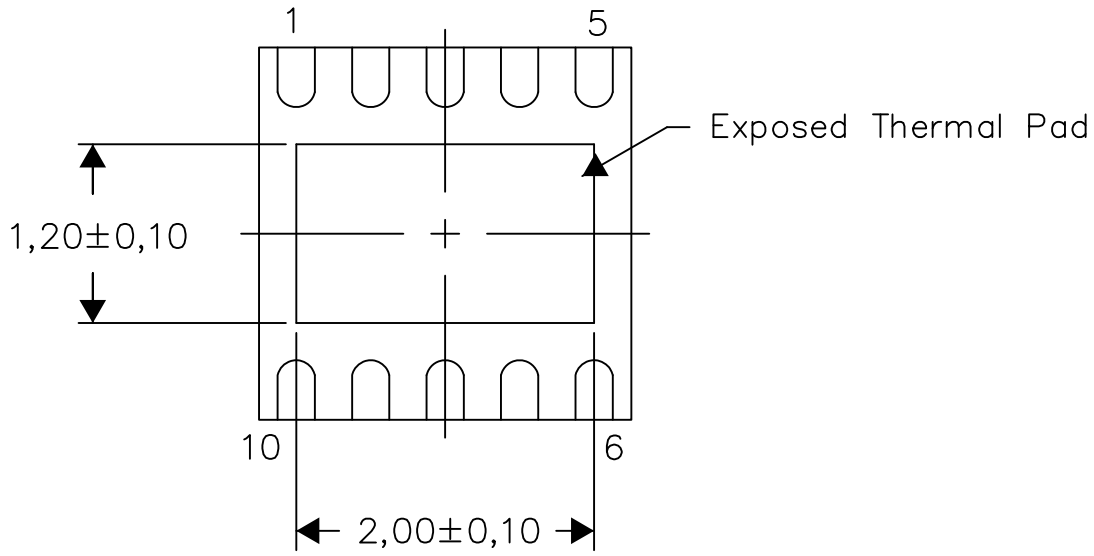
DSK (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



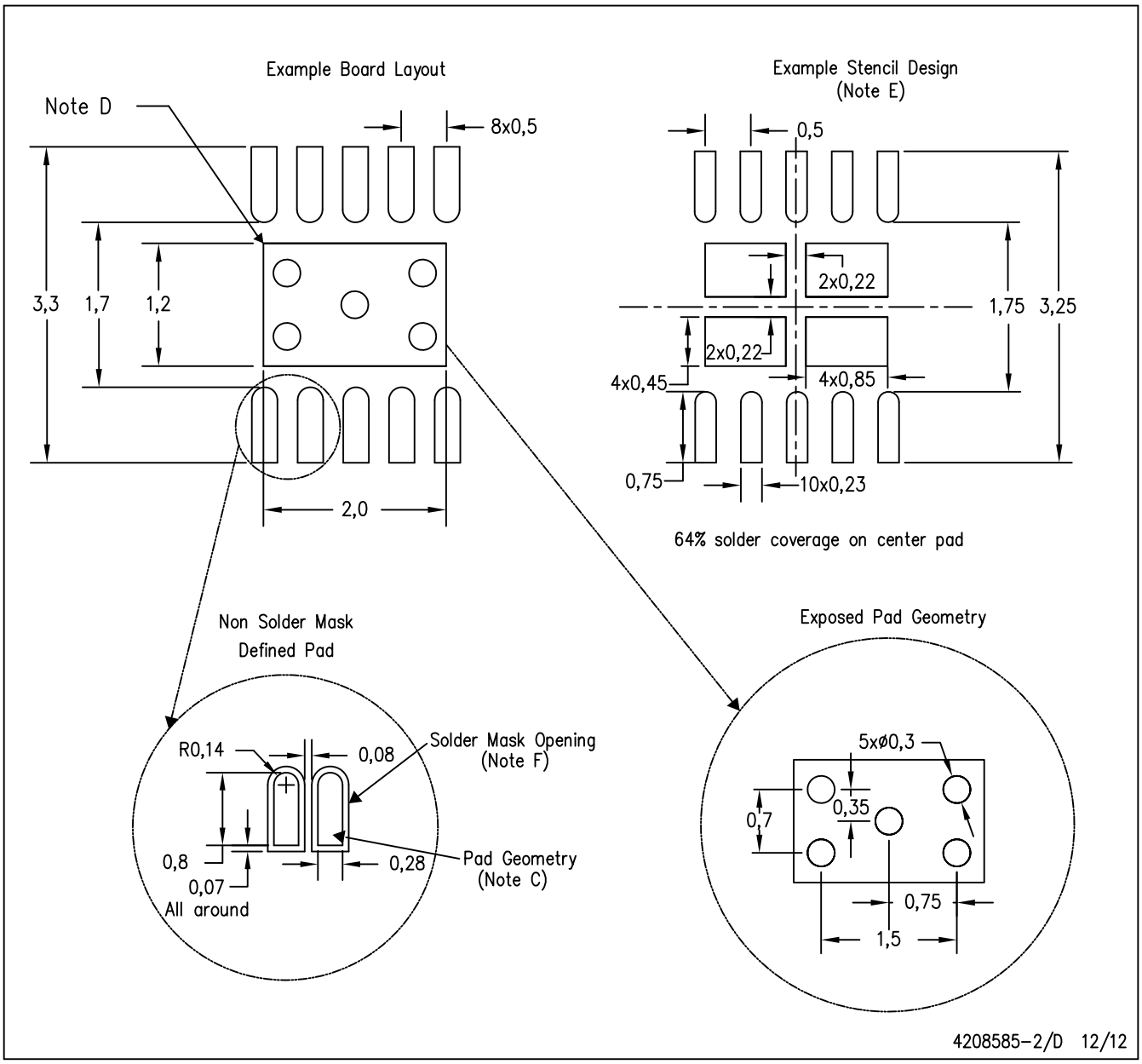
Bottom View

Exposed Thermal Pad Dimensions

4208579–2/E 12/12

NOTE: All linear dimensions are in millimeters

DSK (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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